Intel 80286/80386/80486
<table>
<thead>
<tr>
<th>Specifications</th>
<th>80286</th>
<th>80386</th>
<th>80486</th>
</tr>
</thead>
<tbody>
<tr>
<td>Date</td>
<td>1982</td>
<td>1985</td>
<td>1989</td>
</tr>
<tr>
<td>CPU speed</td>
<td>6 - 25 MHz</td>
<td>12 - 40 MHz</td>
<td>16 - 100 MHz</td>
</tr>
<tr>
<td>Cores</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Registers (Programmer)</td>
<td>8, 15 total</td>
<td>16, ?</td>
<td>16, ?</td>
</tr>
<tr>
<td>RAM</td>
<td>16 MB</td>
<td>4 GB</td>
<td>4 GB</td>
</tr>
<tr>
<td>Functional Units</td>
<td>4</td>
<td>6</td>
<td>9</td>
</tr>
<tr>
<td>Pipeline stages</td>
<td>3</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Cache off chip</td>
<td>0</td>
<td>Yes (support)</td>
<td>Yes (support)</td>
</tr>
<tr>
<td>Cache on chip</td>
<td>0</td>
<td>0</td>
<td>8 KB</td>
</tr>
<tr>
<td>Transistors</td>
<td>134,000</td>
<td>275,000</td>
<td>&gt; 1,000,000</td>
</tr>
</tbody>
</table>
i286 Features

- 16-bit registers & data bus, 24-bit address
- Addresses 1 GB of virtual memory
- MMU
- Task Management
- Protection Mechanism
- Built-in memory protection
- Operates in Real and Protected mode
i386 Features

- 32-bit registers, address, & data bus
- Backwards Compatibility with 80x86 CPUs
- Improved Protected Mode
- Paged Virtual Memory
- Virtual-86 Mode
i486 Features

- On-chip 8 KB Level 1 Cache
- Integrated FPU
- Improved MMU performance
  - Memory segmentation and paging are supported
  - Address management and memory-space protection mechanisms
- Tightly coupled pipelining
  - Fetching, decoding, address translation overlapped
  - Single Cycle Execution
Pipeline Stages

286 and 386 Pipeline stages
- Fetch
- Decode
- Execute

486 Pipeline stages
- Fetch:
  - Load 16 bytes of instructions into prefetch buffer
- Decode1:
  - Determine instruction length
  - Determine instruction type
- Decode2:
  - Compute memory address
  - Generate immediate operands
- Execute:
  - Read register operands
  - Compute ALU function
  - Read/write memory
- Write-Back:
  - Update register file
- Code Prefetch Unit  *Half IU
  - Program look ahead func.
  - 16-byte Code Queue
- Instruction Decode Unit  *Half IU
  - Takes from Prefetch Queue
  - Translates instructions into microcode
  - Stores in 3-deep instruction queue for EU
- Segmentation Unit  *AU
  - Translates logical address into linear addresses
  - Checks for bus-cycle segmentation violations
  - Linear addr. -> Paging unit
- Paging Unit  * NEW
  - Translates linear addr. to physical addr.
- Cache Unit  *NEW
  - 4-way set associative
  - Closely coupled with IPU
- Control Unit  *Half EU
  - Interprets instructions from IDU
  - Controls IU, FPU, SU
- Integer (datapath) Unit  *Half EU
  - Identifies where data is
  - Performs arithmetic & logic operations, in 386 instruction set
- Floating-point Unit  *NEW


References


Questions?