PIC12F629/675

Data Sheet

8-Pin FLASH-Based 8-Bit CMOS Microcontrollers
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8-Pin FLASH-Based 8-Bit CMOS Microcontroller

High Performance RISC CPU:
- Only 35 instructions to learn
  - All single cycle instructions except branches
- Operating speed:
  - DC - 20 MHz oscillator/clock input
  - DC - 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect, and Relative Addressing modes

Special Microcontroller Features:
- Internal and external oscillator options
  - Precision Internal 4 MHz oscillator factory calibrated to ±1%
  - External Oscillator support for crystals and resonators
  - 5 μs wake-up from SLEEP, 3.0V, typical
- Power saving SLEEP mode
- Wide operating voltage range - 2.0V to 5.5V
- Industrial and Extended temperature range
- Low power Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Detect (BOD)
- Watchdog Timer (WDT) with independent oscillator for reliable operation
- Multiplexed MCLR/Input-pin
- Interrupt-on-pin change
- Individual programmable weak pull-ups
- Programmable code protection
- High Endurance FLASH/EEPROM Cell
  - 100,000 write FLASH endurance
  - 1,000,000 write EEPROM endurance
  - FLASH/Data EEPROM Retention: > 40 years

Low Power Features:
- Standby Current:
  - 1 nA @ 2.0V, typical
- Operating Current:
  - 8.5 μA @ 32 kHz, 2.0V, typical
  - 100 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current
  - 300 nA @ 2.0V, typical
- Timer1 oscillator current:
  - 4 μA @ 32 kHz, 2.0V, typical

Peripheral Features:
- 6 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
  - One analog comparator
    - Programmable on-chip comparator voltage reference (CVREF) module
    - Programmable input multiplexing from device inputs
    - Comparator output is externally accessible
- Analog-to-Digital Converter module (PIC12F675):
  - 10-bit resolution
  - Programmable 4-channel input
  - Voltage reference input
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTOSC mode selected
- In-Circuit Serial Programming™ (ICSP™) via two pins

<table>
<thead>
<tr>
<th>Device</th>
<th>Program Memory</th>
<th>Data Memory</th>
<th>I/O</th>
<th>10-bit A/D (ch)</th>
<th>Comparators</th>
<th>Timers 8/16-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FLASH (words)</td>
<td>SRAM (bytes)</td>
<td>EEPROM (bytes)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC12F629</td>
<td>1024</td>
<td>64</td>
<td>128</td>
<td>6</td>
<td>1</td>
<td>1/1</td>
</tr>
<tr>
<td>PIC12F675</td>
<td>1024</td>
<td>64</td>
<td>128</td>
<td>6</td>
<td>4</td>
<td>1</td>
</tr>
</tbody>
</table>

* 8-bit, 8-pin devices protected by Microchip’s Low Pin Count Patent: U.S. Patent No. 5,847,450. Additional U.S. and foreign patents and applications may be issued or pending.
Pin Diagrams

8-pin PDIP, SOIC, DFN-S

PIC12F629

1  2  3  4  5  6  7  8
VDD   Vss
GP5/T1CKI/OSC1/CLKIN  GP0/CIN+/ICSPDAT
GP4/T1G/OSC2/CLKOUT  GP1/CIN-/ICSPCLK
GP3/MCLR/VPP  GP2/T0CKI/INT/COUT

PIC12F675

1  2  3  4  5  6  7  8
VDD   Vss
GP5/T1CKI/OSC1/CLKIN  GP0/AN0/CIN+/ICSPDAT
GP4/AN3/T1G/OSC2/CLKOUT  GP1/AN1/CIN-/VREF/ICSPCLK
GP3/MCLR/VPP  GP2/AN2/T0CKI/INT/COUT
Table of Contents

1.0 Device Overview ........................................................................................................... 5
2.0 Memory Organization .................................................................................................... 7
3.0 GPIO Port ....................................................................................................................... 19
4.0 Timer0 Module ............................................................................................................. 27
5.0 Timer1 Module with Gate Control ................................................................................. 30
6.0 Comparator Module ...................................................................................................... 35
7.0 Analog-to-Digital Converter (A/D) Module (PIC12F675 only) ..................................... 41
8.0 Data EEPROM Memory ............................................................................................... 47
9.0 Special Features of the CPU ....................................................................................... 51
10.0 Instruction Set Summary ............................................................................................. 69
11.0 Development Support ............................................................................................... 77
12.0 Electrical Specifications ............................................................................................. 83
13.0 DC and AC Characteristics Graphs and Tables ............................................................ 105
14.0 Packaging Information ............................................................................................... 115
Appendix A: Data Sheet Revision History ........................................................................ 121
Appendix B: Device Differences ....................................................................................... 121
Appendix C: Device Migrations ....................................................................................... 122
Appendix D: Migrating from other PICmicro® Devices ..................................................... 122
Index ................................................................................................................................. 123
On-Line Support .................................................................................................................. 127
Systems Information and Upgrade Hot Line ...................................................................... 127
Reader Response .............................................................................................................. 128
Product Identification System ............................................................................................ 129

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1.0 DEVICE OVERVIEW

This document contains device specific information for the PIC12F629/675. Additional information may be found in the PICmicro™ Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this Data Sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC12F629 and PIC12F675 devices are covered by this Data Sheet. They are identical, except the PIC12F675 has a 10-bit A/D converter. They come in 8-pin PDIP, SOIC, and MLF-S packages. Figure 1-1 shows a block diagram of the PIC12F629/675 devices. Table 1-1 shows the Pinout Description.

FIGURE 1-1: PIC12F629/675 BLOCK DIAGRAM

Note 1: Higher order bits are from STATUS register.
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP0/AN0/CIN+/ICSPDAT</td>
<td>GP0</td>
<td>TTL</td>
<td>CMOS</td>
<td>Bi-directional I/O w/ programmable pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>AN0</td>
<td>AN</td>
<td></td>
<td>A/D Channel 0 input</td>
</tr>
<tr>
<td></td>
<td>CIN+</td>
<td>AN</td>
<td></td>
<td>Comparator input</td>
</tr>
<tr>
<td></td>
<td>ICSPDAT</td>
<td>TTL</td>
<td>CMOS</td>
<td>Serial programming I/O</td>
</tr>
<tr>
<td>GP1/AN1/CIN-/VREF/ICSPCLK</td>
<td>GP1</td>
<td>TTL</td>
<td>CMOS</td>
<td>Bi-directional I/O w/ programmable pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>AN1</td>
<td>AN</td>
<td></td>
<td>A/D Channel 1 input</td>
</tr>
<tr>
<td></td>
<td>CIN-</td>
<td>AN</td>
<td></td>
<td>Comparator input</td>
</tr>
<tr>
<td></td>
<td>VREF</td>
<td>AN</td>
<td></td>
<td>External voltage reference</td>
</tr>
<tr>
<td></td>
<td>ICSPCLK</td>
<td>ST</td>
<td></td>
<td>Serial programming clock</td>
</tr>
<tr>
<td>GP2/AN2/T0CKI/INT/COUT</td>
<td>GP2</td>
<td>ST</td>
<td>CMOS</td>
<td>Bi-directional I/O w/ programmable pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>AN2</td>
<td>AN</td>
<td></td>
<td>A/D Channel 2 input</td>
</tr>
<tr>
<td></td>
<td>T0CKI</td>
<td>ST</td>
<td></td>
<td>TMR0 clock input</td>
</tr>
<tr>
<td></td>
<td>INT</td>
<td>ST</td>
<td></td>
<td>External interrupt</td>
</tr>
<tr>
<td></td>
<td>COUT</td>
<td>CMOS</td>
<td></td>
<td>Comparator output</td>
</tr>
<tr>
<td>GP3/MCLR/VPP</td>
<td>GP3</td>
<td>TTL</td>
<td></td>
<td>Input port w/ interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>MCLR</td>
<td>ST</td>
<td></td>
<td>Master Clear</td>
</tr>
<tr>
<td></td>
<td>VPP</td>
<td>HV</td>
<td></td>
<td>Programming voltage</td>
</tr>
<tr>
<td>GP4/AN3/T1G/OSC2/CLKOUT</td>
<td>GP4</td>
<td>TTL</td>
<td>CMOS</td>
<td>Bi-directional I/O w/ programmable pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>AN3</td>
<td>AN</td>
<td></td>
<td>A/D Channel 3 input</td>
</tr>
<tr>
<td></td>
<td>T1G</td>
<td>ST</td>
<td></td>
<td>TMR1 gate</td>
</tr>
<tr>
<td></td>
<td>OSC2</td>
<td>XTAL</td>
<td></td>
<td>Crystal/resonator</td>
</tr>
<tr>
<td></td>
<td>CLKOUT</td>
<td>CMOS</td>
<td></td>
<td>Fosc/4 output</td>
</tr>
<tr>
<td>GP5/T1CKI/OSC1/CLKIN</td>
<td>GP5</td>
<td>TTL</td>
<td>CMOS</td>
<td>Bi-directional I/O w/ programmable pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>T1CKI</td>
<td>ST</td>
<td></td>
<td>TMR1 clock</td>
</tr>
<tr>
<td></td>
<td>OSC1</td>
<td>XTAL</td>
<td></td>
<td>Crystal/resonator</td>
</tr>
<tr>
<td></td>
<td>CLKIN</td>
<td>ST</td>
<td></td>
<td>External clock input/RC oscillator connection</td>
</tr>
<tr>
<td>VSS</td>
<td>VSS</td>
<td>Power</td>
<td></td>
<td>Ground reference</td>
</tr>
<tr>
<td>VDD</td>
<td>VDD</td>
<td>Power</td>
<td></td>
<td>Positive supply</td>
</tr>
</tbody>
</table>

Legend: Shade = PIC12F675 only
TTL = TTL input buffer, ST = Schmitt Trigger input buffer
2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC12F629/675 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h - 03FFh) for the PIC12F629/675 devices is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 1K x 14 space. The RESET vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose registers and the Special Function registers. The Special Function registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when read. RP0 (STATUS<5>) is the bank select bit.

- RP0 = 0 Bank 0 is selected
- RP0 = 1 Bank 1 is selected

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the PIC12F629/675 devices. Each register is accessed, either directly or indirectly, through the File Select Register FSR (see Section 2.4).

Note: The IRP and RP1 bits STATUS<7:6> are reserved and should always be maintained as '0's.
2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

**FIGURE 2-2: DATA MEMORY MAP OF THE PIC12F629/675**

<table>
<thead>
<tr>
<th>File Address</th>
<th>File Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Indirect addr. (1) 00h</td>
<td>Indirect addr. (1) 80h</td>
</tr>
<tr>
<td>TMR0 01h</td>
<td>OPTION_REG 81h</td>
</tr>
<tr>
<td>PCL 02h</td>
<td>PCL 82h</td>
</tr>
<tr>
<td>STATUS 03h</td>
<td>STATUS 83h</td>
</tr>
<tr>
<td>FSR 04h</td>
<td>FSR 84h</td>
</tr>
<tr>
<td>GPIO 05h</td>
<td>TRISIO 85h</td>
</tr>
<tr>
<td>06h</td>
<td>06h</td>
</tr>
<tr>
<td>07h</td>
<td>07h</td>
</tr>
<tr>
<td>08h</td>
<td>08h</td>
</tr>
<tr>
<td>09h</td>
<td>09h</td>
</tr>
<tr>
<td>PCLATH 0Ah</td>
<td>PCLATH 8Ah</td>
</tr>
<tr>
<td>INTCN 0Bh</td>
<td>INTCN 8Bh</td>
</tr>
<tr>
<td>PIE1 0Ch</td>
<td>PIE1 8Ch</td>
</tr>
<tr>
<td>0Dh</td>
<td>0Dh</td>
</tr>
<tr>
<td>TMR1L 0Eh</td>
<td>PCON 8Eh</td>
</tr>
<tr>
<td>TMR1H 0Fh</td>
<td>8Fh</td>
</tr>
<tr>
<td>T1CON 08h</td>
<td>OSCCAL 90h</td>
</tr>
<tr>
<td>11h</td>
<td>11h</td>
</tr>
<tr>
<td>12h</td>
<td>12h</td>
</tr>
<tr>
<td>13h</td>
<td>13h</td>
</tr>
<tr>
<td>14h</td>
<td>14h</td>
</tr>
<tr>
<td>15h</td>
<td>WPU 95h</td>
</tr>
<tr>
<td>16h</td>
<td>IOC 96h</td>
</tr>
<tr>
<td>17h</td>
<td>97h</td>
</tr>
<tr>
<td>18h</td>
<td>98h</td>
</tr>
<tr>
<td>CMCON 19h</td>
<td>VRCON 99h</td>
</tr>
<tr>
<td>1Ah</td>
<td>Eedata 9Ah</td>
</tr>
<tr>
<td>1Bh</td>
<td>Eeadr 9Bh</td>
</tr>
<tr>
<td>1Ch</td>
<td>EECON1 9Ch</td>
</tr>
<tr>
<td>1Dh</td>
<td>EECON2 (2) 9Dh</td>
</tr>
<tr>
<td>ADRESH (2) 1Eh</td>
<td>ADRESL (2) 9Eh</td>
</tr>
<tr>
<td>ADCON (2) 1Fh</td>
<td>ANSEL (2) 9Fh</td>
</tr>
<tr>
<td>20h</td>
<td>accesses 20h-5Fh</td>
</tr>
<tr>
<td>5Fh</td>
<td>DFh</td>
</tr>
<tr>
<td>60h</td>
<td>E0h</td>
</tr>
<tr>
<td>7Fh</td>
<td>FFh</td>
</tr>
</tbody>
</table>

Bank 0

Bank 1

Unimplemented data memory locations, read as ‘0’.
1: Not a physical register.
2: PIC12F675 only.
TABLE 2-1: SPECIAL FUNCTION REGISTERS SUMMARY

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOD</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>INDF(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>18,59</td>
</tr>
<tr>
<td>01h</td>
<td>TMR0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx</td>
<td>27</td>
</tr>
<tr>
<td>02h</td>
<td>PCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>17</td>
</tr>
<tr>
<td>03h</td>
<td>STATUS</td>
<td>RP1(2)</td>
<td>RP1(2)</td>
<td>RP0</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>0001 1xxx</td>
<td>11</td>
</tr>
<tr>
<td>04h</td>
<td>FSR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx</td>
<td>18</td>
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<tr>
<td>05h</td>
<td>GPIO</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>06h</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<td>07h</td>
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<tr>
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<td></td>
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<tr>
<td>09h</td>
<td>—</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0Ah</td>
<td>PCLATH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Write Buffer for Upper 5 bits of Program Counter</td>
<td>---0 0000</td>
</tr>
<tr>
<td>0Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
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<td>ADRESH(3)</td>
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<td></td>
<td>Most Significant 8 bits of the Left Shifted A/D Result or 2 bits of the Right Shifted Result</td>
<td>xxxxx xxxxx</td>
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<tr>
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<td>ADCON0(3)</td>
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</table>

Legend: — = unimplemented locations read as '0'; u = unchanged; x = unknown; q = value depends on condition; shaded = unimplemented

Note 1: This is not a physical register.
2: These bits are reserved and should always be maintained as '0'.
3: PIC12F675 only.
### Table 2-1: Special Function Registers Summary (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOD</th>
<th>Page</th>
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<td></td>
<td></td>
<td>0000</td>
</tr>
</tbody>
</table>

Legend:  — = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: This is not a physical register.

2: These bits are reserved and should always be maintained as '0'.

3: PIC12F675 only.
2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:
- the arithmetic status of the ALU
- the RESET status
- the bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as 0000 u uuu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any STATUS bits. For other instructions not affecting any STATUS bits, see the “Instruction Set Summary”.

Note 1: Bits IRP and RP1 (STATUS<7:6>) are not used by the PIC12F629/675 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.

2: The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

### REGISTER 2-1: STATUS — STATUS REGISTER (ADDRESS: 03h OR 83h)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>IRP</td>
<td>This bit is reserved and should be maintained as ‘0’</td>
</tr>
<tr>
<td>6</td>
<td>RP1</td>
<td>This bit is reserved and should be maintained as ‘0’</td>
</tr>
<tr>
<td>5</td>
<td>RP0</td>
<td>Register Bank Select bit (used for direct addressing)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Bank 0 (00h - 7Fh)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Bank 1 (80h - FFh)</td>
</tr>
<tr>
<td>4</td>
<td>TO</td>
<td>Time-out bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = After power-up, CLRWDT instruction, or SLEEP instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = A WDT time-out occurred</td>
</tr>
<tr>
<td>3</td>
<td>PD</td>
<td>Power-down bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = After power-up or by the CLRWDT instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = By execution of the SLEEP instruction</td>
</tr>
<tr>
<td>2</td>
<td>Z</td>
<td>Zero bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = The result of an arithmetic or logic operation is zero</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = The result of an arithmetic or logic operation is not zero</td>
</tr>
<tr>
<td>1</td>
<td>DC</td>
<td>Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>For borrow, the polarity is reversed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = A carry-out from the 4th low order bit of the result occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = No carry-out from the 4th low order bit of the result</td>
</tr>
<tr>
<td>0</td>
<td>C</td>
<td>Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = A carry-out from the Most Significant bit of the result occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = No carry-out from the Most Significant bit of the result occurred</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown
2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- TMR0/WDT prescaler
- External GP2/INT interrupt
- TMR0
- Weak pull-ups on GPIO

REGISTER 2-2: OPTION_REG — OPTION REGISTER (ADDRESS: 81h)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2-0</th>
</tr>
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<tr>
<td>GPPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2:PS0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>TMR0 Rate</th>
<th>WDT Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1 : 2</td>
<td>1 : 1</td>
</tr>
<tr>
<td>001</td>
<td>1 : 4</td>
<td>1 : 2</td>
</tr>
<tr>
<td>010</td>
<td>1 : 8</td>
<td>1 : 4</td>
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<tr>
<td>011</td>
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<td>1 : 8</td>
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<tr>
<td>100</td>
<td>1 : 32</td>
<td>1 : 16</td>
</tr>
<tr>
<td>101</td>
<td>1 : 64</td>
<td>1 : 32</td>
</tr>
<tr>
<td>110</td>
<td>1 : 128</td>
<td>1 : 64</td>
</tr>
<tr>
<td>111</td>
<td>1 : 256</td>
<td>1 : 128</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

Note: To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT by setting PSA bit to ‘1’ (OPTION<3>). See Section 4.4.
### INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO port change and external GP2/INT pin interrupts.

#### Note

Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

#### REGISTER 2-3: INTCON — INTERRUPT CONTROL REGISTER (ADDRESS: 0Bh OR 8Bh)

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
</tr>
</tbody>
</table>

- **bit 7**  
  **GIE**: Global Interrupt Enable bit  
  1 = Enables all unmasked interrupts  
  0 = Disables all interrupts  

- **bit 6**  
  **PEIE**: Peripheral Interrupt Enable bit  
  1 = Enables all unmasked peripheral interrupts  
  0 = Disables all peripheral interrupts  

- **bit 5**  
  **T0IE**: TMR0 Overflow Interrupt Enable bit  
  1 = Enables the TMR0 interrupt  
  0 = Disables the TMR0 interrupt  

- **bit 4**  
  **INTE**: GP2/INT External Interrupt Enable bit  
  1 = Enables the GP2/INT external interrupt  
  0 = Disables the GP2/INT external interrupt  

- **bit 3**  
  **GPIE**: Port Change Interrupt Enable bit(1)  
  1 = Enables the GPIO port change interrupt  
  0 = Disables the GPIO port change interrupt  

- **bit 2**  
  **T0IF**: TMR0 Overflow Interrupt Flag bit(2)  
  1 = TMR0 register has overflowed (must be cleared in software)  
  0 = TMR0 register did not overflow  

- **bit 1**  
  **INTF**: GP2/INT External Interrupt Flag bit  
  1 = The GP2/INT external interrupt occurred (must be cleared in software)  
  0 = The GP2/INT external interrupt did not occur  

- **bit 0**  
  **GPIF**: Port Change Interrupt Flag bit  
  1 = When at least one of the GP5:GP0 pins changed state (must be cleared in software)  
  0 = None of the GP5:GP0 pins have changed state

#### Note 1

IOC register must also be enabled to enable an interrupt-on-change.

2: T0IF bit is set when TIMER0 rolls over. TIMER0 is unchanged on RESET and should be initialized before clearing T0IF bit.

#### Legend:

- **R** = Readable bit  
- **W** = Writable bit  
- **U** = Unimplemented bit, read as ‘0’  
- **n** = Value at POR  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared  
- **x** = Bit is unknown
### 2.2.2.4 PIE1 Register

The PIE1 register contains the interrupt enable bits, as shown in Register 2-4.

**REGISTER 2-4: PIE1 — PERIPHERAL INTERRUPT ENABLE REGISTER 1 (ADDRESS: 8Ch)**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEIE</td>
<td>ADIE</td>
<td>—</td>
<td>—</td>
<td>CMIE</td>
<td>—</td>
<td>—</td>
<td>TMR1IE</td>
</tr>
</tbody>
</table>

#### bit 7 EEIE: EE Write Complete Interrupt Enable bit
- 1 = Enables the EE write complete interrupt
- 0 = Disables the EE write complete interrupt

#### bit 6 ADIE: A/D Converter Interrupt Enable bit (PIC12F675 only)
- 1 = Enables the A/D converter interrupt
- 0 = Disables the A/D converter interrupt

#### bit 5-4 Unimplemented: Read as ‘0’

#### bit 3 CMIE: Comparator Interrupt Enable bit
- 1 = Enables the comparator interrupt
- 0 = Disables the comparator interrupt

#### bit 2-1 Unimplemented: Read as ‘0’

#### bit 0 TMR1IE: TMR1 Overflow Interrupt Enable bit
- 1 = Enables the TMR1 overflow interrupt
- 0 = Disables the TMR1 overflow interrupt

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**Note:** Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.
2.2.2.5 PIR1 Register

The PIR1 register contains the interrupt flag bits, as shown in Register 2-5.

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**REGISTER 2-5: PIR1 — PERIPHERAL INTERRUPT REGISTER 1 (ADDRESS: 0Ch)**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEIF</td>
<td>ADIF</td>
</tr>
<tr>
<td>CMIF</td>
<td>CMIF</td>
</tr>
<tr>
<td>TMR1IF</td>
<td>TMR1IF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5-4</th>
<th>Bit 3</th>
<th>Bit 2-1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EEIF:</strong> EEPROM Write Operation Interrupt Flag bit</td>
<td><strong>ADIF:</strong> A/D Converter Interrupt Flag bit (PIC12F675 only)</td>
<td><strong>Unimplemented:</strong> Read as ‘0’</td>
<td><strong>CMIF:</strong> Comparator Interrupt Flag bit</td>
<td><strong>Unimplemented:</strong> Read as ‘0’</td>
<td><strong>TMR1IF:</strong> TMR1 Overflow Interrupt Flag bit</td>
</tr>
<tr>
<td>1 = The write operation completed (must be cleared in software)</td>
<td>1 = The A/D conversion is complete (must be cleared in software)</td>
<td>0 = The write operation has not completed or has not been started</td>
<td>0 = Comparator input has not changed</td>
<td>0 = Comparator input has not changed</td>
<td>1 = TMR1 register overflowed (must be cleared in software)</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown
2.2.2.6 PCON Register
The Power Control (PCON) register contains flag bits to differentiate between a:

- Power-on Reset (POR)
- Brown-out Detect (BOD)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON Register bits are shown in Register 2-6.

REGISTER 2-6: PCON — POWER CONTROL REGISTER (ADDRESS: 8Eh)

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>POR</td>
<td>BOD</td>
</tr>
</tbody>
</table>

bit 7-2 **Unimplemented**: Read as ‘0’
bit 1 **POR**: Power-on Reset STATUS bit
  1 = No Power-on Reset occurred
  0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)
bit 0 **BOD**: Brown-out Detect STATUS bit
  1 = No Brown-out Detect occurred
  0 = A Brown-out Detect occurred (must be set in software after a Brown-out Detect occurs)

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

2.2.2.7 OSCCAL Register
The Oscillator Calibration register (OSCCAL) is used to calibrate the internal 4 MHz oscillator. It contains 6 bits to adjust the frequency up or down to achieve 4 MHz.

The OSCCAL register bits are shown in Register 2-7.

REGISTER 2-7: OSCCAL — OSCILLATOR CALIBRATION REGISTER (ADDRESS: 90h)

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAL5</td>
<td>CAL4</td>
<td>CAL3</td>
<td>CAL2</td>
<td>CAL1</td>
<td>CAL0</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

bit 7-2 **CAL5:CAL0**: 6-bit Signed Oscillator Calibration bits

- **111111** = Maximum frequency
- **100000** = Center frequency
- **000000** = Minimum frequency
bit 1-0 **Unimplemented**: Read as ‘0’

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown
2.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any RESET, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS

2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note “Implementing a Table Read” (AN556).

2.3.2 STACK

The PIC12F629/675 family has an 8-level deep x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed, or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no STATUS bits to indicate stack overflow or stack underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or the vectoring to an interrupt address.
2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly will result in a no operation (although STATUS bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

**EXAMPLE 2-1: INDIRECT ADDRESSING**

```assembly
movlw 0x20 ;initialize pointer
movwf FSR ;to RAM
NEXT clrf INDF ;clear INDF register
incf FSR ;inc pointer
btfss FSR,4 ;all done?
goto NEXT ;no clear next
CONTINUE ;yes continue
```

**FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC12F629/675**

For memory map detail see Figure 2-2.

**Note 1:** The RP1 and IRP bits are reserved; always maintain these bits clear.
3.0 GPIO PORT

There are as many as six general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

Note: Additional information on I/O ports may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023)

3.1 GPIO and the TRISIO Registers

GPIO is an 6-bit wide, bi-directional port. The corresponding data direction register is TRISIO. Setting a TRISIO bit (= 1) will make the corresponding GPIO pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISIO bit (= 0) will make the corresponding GPIO pin an output (i.e., put the contents of the output latch on the selected pin). The exception is GP3, which is input only and its TRISIO bit will always read as ‘1’. Example 3-1 shows how to initialize GPIO.

Reading the GPIO register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch. GP3 reads ‘0’ when MCLREN = 1.

The TRISIO register controls the direction of the GP pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISIO register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read ‘0’.

Note: The ANSEL (9Fh) and CMCON (19h) registers (9Fh) must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’. The ANSEL register is defined for the PIC12F675.

EXAMPLE 3-1: INITIALIZING GPIO

bcf STATUS, RP0 ; Bank 0
clrf GPIO ; Init GPIO
movlw 07h ; Set GP<2:0> to digital IO
movwf CMCON ;
clf ANSEL ; Digital I/O
movlw 0Ch ; Set GP<3:2> as inputs
movwf TRISIO ; and set GP<5:4,1:0> as outputs

3.2 Additional Pin Functions

Every GPIO pin on the PIC12F629/675 has an interrupt-on-change option and every GPIO pin, except GP3, has a weak pull-up option. The next two sections describe these functions.

3.2.1 WEAK PULL-UP

Each of the GPIO pins, except GP3, has an individually configurable weak internal pull-up. Control bits WPUX enable or disable each pull-up. Refer to Register 3-3. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are enabled on a Power-on Reset by the GPPU bit (OPTION<7>).

REGISTER 3-1: GPIO — GPIO REGISTER (ADDRESS: 05h)

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>GPIO5</td>
<td>GPIO4</td>
<td>GPIO3</td>
<td>GPIO2</td>
<td>GPIO1</td>
<td>GPIO0</td>
</tr>
</tbody>
</table>

bit 7

bit 7-6: Unimplemented: Read as ‘0’

bit 5-0: GPIO<5:0>: General Purpose I/O pin.
  1 = Port pin is >VH
  0 = Port pin is <VL

Legend:
R = Readable bit    W = Writable bit    U = Unimplemented bit, read as ‘0’
- n = Value at POR    ’1’ = Bit is set     ’0’ = Bit is cleared    x = Bit is unknown

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REGISTER 3-2: TRISIO — GPIO TRISTATE REGISTER (ADDRESS: 85h)

<table>
<thead>
<tr>
<th>bit 7-6:</th>
<th>bit 5-0:</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Unimplemented:</strong> Read as '0'</td>
<td>TRISIO&lt;5:0&gt;: General Purpose I/O Tri-State Control bit</td>
</tr>
<tr>
<td>1 = GPIO pin configured as an input (tri-stated)</td>
<td>0 = GPIO pin configured as an output.</td>
</tr>
<tr>
<td><strong>Note:</strong> TRISIO&lt;3&gt; always reads 1.</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- U = Unimplemented bit, read as '0'
- W = Writable bit
- - n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

REGISTER 3-3: WPU — WEAK PULL-UP REGISTER (ADDRESS: 95h)

<table>
<thead>
<tr>
<th>bit 7-6:</th>
<th>bit 5-4:</th>
<th>bit 3-0:</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Unimplemented:</strong> Read as '0'</td>
<td>WPU&lt;5:4&gt;: Weak Pull-up Register bit</td>
<td></td>
</tr>
<tr>
<td>1 = Pull-up enabled</td>
<td>0 = Pull-up disabled</td>
<td></td>
</tr>
<tr>
<td><strong>Note 1:</strong> Global GPPU must be enabled for individual pull-ups to be enabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Note 2:</strong> The weak pull-up device is automatically disabled if the pin is in Output mode (TRISIO = 0).</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- U = Unimplemented bit, read as '0'
- W = Writable bit
- - n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown
3.2.2 INTERRUPT-ON-CHANGE

Each of the GPIO pins is individually configurable as an interrupt-on-change pin. Control bits IOC enable or disable the interrupt function for each pin. Refer to Register 3-4. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of GPIO. The ‘mismatch’ outputs of the last read are OR'd together to set, the GP Port Change Interrupt flag bit (GPIF) in the INTCON register.

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of GPIO. This will end the mismatch condition.
b) Clear the flag bit GPIF.

A mismatch condition will continue to set flag bit GPIF. Reading GPIO will end the mismatch condition and allow flag bit GPIF to be cleared.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the GPIF interrupt flag may not get set.

REGISTER 3-4: IOC — INTERRUPT-ON-CHANGE GPIO REGISTER (ADDRESS: 96h)

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>IOC5</td>
<td>IOC4</td>
<td>IOC3</td>
<td>IOC2</td>
<td>IOC1</td>
<td>IOC0</td>
</tr>
</tbody>
</table>

bit 7  bit 0

bit 7-6 Unimplemented: Read as ‘0’
bit 5-0 IOC<5:0>: Interrupt-on-Change GPIO Control bit
1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

Note 1: Global interrupt enable (GIE) must be enabled for individual interrupts to be recognized.

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
- n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown
3.3 Pin Descriptions and Diagrams

Each GPIO pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the A/D, refer to the appropriate section in this Data Sheet.

3.3.1 GP0/AN0/CIN+

Figure 3-1 shows the diagram for this pin. The GP0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D (PIC12F675 only)
- an analog input to the comparator

3.3.2 GP1/AN1/CIN-/VREF

Figure 3-1 shows the diagram for this pin. The GP1 pin is configurable to function as one of the following:

- as a general purpose I/O
- an analog input for the A/D (PIC12F675 only)
- an analog input to the comparator
- a voltage reference input for the A/D (PIC12F675 only)
3.3.3 GP2/AN2/T0CKI/INT/COUT

Figure 3-2 shows the diagram for this pin. The GP2 pin is configurable to function as one of the following:
- a general purpose I/O
- an analog input for the A/D (PIC12F675 only)
- the clock input for TMR0
- an external edge triggered interrupt
- a digital output from the comparator

3.3.4 GP3/MCLR/VPP

Figure 3-3 shows the diagram for this pin. The GP3 pin is configurable to function as one of the following:
- a general purpose input
- as Master Clear Reset

FIGURE 3-2: BLOCK DIAGRAM OF GP2

FIGURE 3-3: BLOCK DIAGRAM OF GP3
3.3.5 GP4/AN3/T1G/OSC2/CLKOUT

Figure 3-4 shows the diagram for this pin. The GP4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D (PIC12F675 only)
- a TMR1 gate input
- a crystal/resonator connection
- a clock output

**FIGURE 3-4: BLOCK DIAGRAM OF GP4**

3.3.6 GP5/T1CKI/OSC1/CLKIN

Figure 3-5 shows the diagram for this pin. The GP5 pin is configurable to function as one of the following:

- a general purpose I/O
- a TMR1 clock input
- a crystal/resonator connection
- a clock input

**FIGURE 3-5: BLOCK DIAGRAM OF GP5**

Note 1: CLK modes are XT, HS, LP, LPTMR1 and CLKOUT Enable.
2: When using Timer1 with LP oscillator, the Schmitt Trigger is by-passed.
TABLE 3-1: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on:</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>05h</td>
<td>GPIO</td>
<td>—</td>
<td>—</td>
<td>GP5</td>
<td>GP4</td>
<td>GP3</td>
<td>GP2</td>
<td>GP1</td>
<td>GP0</td>
<td>——xx xxxx</td>
<td>——uu uuuu</td>
</tr>
<tr>
<td>0Bh/8Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPEIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000</td>
<td>0000 0000u</td>
</tr>
<tr>
<td>19h</td>
<td>CMCON</td>
<td>—</td>
<td>COUT</td>
<td>—</td>
<td>CINV</td>
<td>CIS</td>
<td>CM2</td>
<td>CM1</td>
<td>CM0</td>
<td>—0—0 0000</td>
<td>—0—0 0000</td>
</tr>
<tr>
<td>81h</td>
<td>OPTION_REG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>85h</td>
<td>TRISIO</td>
<td>—</td>
<td>—</td>
<td>TRISIO5</td>
<td>TRISIO4</td>
<td>TRISIO3</td>
<td>TRISIO2</td>
<td>TRISIO1</td>
<td>TRISIO0</td>
<td>——11 1111</td>
<td>——11 1111</td>
</tr>
<tr>
<td>95h</td>
<td>WPU</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WPU5</td>
<td>WPU4</td>
<td>—</td>
<td>WPU2</td>
<td>WPU1</td>
<td>——11 —111</td>
<td>——11 —111</td>
</tr>
<tr>
<td>96h</td>
<td>IOC</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOC5</td>
<td>IOC4</td>
<td>IOC3</td>
<td>IOC2</td>
<td>IOC1</td>
<td>——00 0000</td>
<td>——00 0000</td>
</tr>
<tr>
<td>9Fh</td>
<td>ANSEL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADCS2</td>
<td>ADCS1</td>
<td>ADCS0</td>
<td>ANS3</td>
<td>ANS2</td>
<td>—000 1111</td>
<td>—000 1111</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by GPIO.
4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:
- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 4-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

Note: Additional information on the Timer0 module is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION_REG<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin GP2/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION_REG<4>). Clearing the T0SE bit selects the rising edge.

Note: Counter mode has specific external clock requirements. Additional information on these requirements is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP since the timer is shut-off during SLEEP.

FIGURE 4-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

Note 1: T0SE, T0CS, PSA, PS0-PS2 are bits in the Option register.
4.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

Note: The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’. The ANSEL register is defined for the PIC12F675.

REGISTER 4-1: OPTION_REG — OPTION REGISTER (ADDRESS: 81h)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td><strong>GPPU</strong>: GPIO Pull-up Enable bit</td>
<td>1 = GPIO pull-ups are disabled 0 = GPIO pull-ups are enabled by individual port latch values</td>
</tr>
<tr>
<td>6</td>
<td><strong>INTEDG</strong>: Interrupt Edge Select bit</td>
<td>1 = Interrupt on rising edge of GP2/INT pin 0 = Interrupt on falling edge of GP2/INT pin</td>
</tr>
<tr>
<td>5</td>
<td><strong>T0CS</strong>: TMR0 Clock Source Select bit</td>
<td>1 = Transition on GP2/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT)</td>
</tr>
<tr>
<td>4</td>
<td><strong>T0SE</strong>: TMR0 Source Edge Select bit</td>
<td>1 = Increment on high-to-low transition on GP2/T0CKI pin 0 = Increment on low-to-high transition on GP2/T0CKI pin</td>
</tr>
<tr>
<td>3</td>
<td><strong>PSA</strong>: Prescaler Assignment bit</td>
<td>1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the TIMER0 module</td>
</tr>
<tr>
<td>2-0</td>
<td><strong>PS2:PS0</strong>: Prescaler Rate Select bits</td>
<td>Bit Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>001</td>
</tr>
<tr>
<td></td>
<td></td>
<td>010</td>
</tr>
<tr>
<td></td>
<td></td>
<td>011</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>101</td>
</tr>
<tr>
<td></td>
<td></td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>111</td>
</tr>
</tbody>
</table>

Legend:  
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’  
- n = Value at POR  
’1’ = Bit is set  
’0’ = Bit is cleared  
x = Bit is unknown
4.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as “prescaler” throughout this Data Sheet. The prescaler assignment is controlled in software by the control bit PSA (OPTION_REG<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS2:PS0 bits (OPTION_REG<2:0>).

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer.

4.4.1 Switching Prescaler Assignment

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 4-1) must be executed when changing the prescaler assignment from Timer0 to WDT.

**Example 4-1: Changing Prescaler (Timer0 → WDT)**

```assembly
bcf STATUS, RP0 ; Bank 0
clrwdt ; Clear WDT
clrf TMR0 ; Clear TMR0 and prescaler
bsf STATUS, RP0 ; Bank 1
movlw b'00101111'; Required if desired
movwf OPTION_REG ; PS2:PS0 is
clrwdt ; 000 or 001
movlw b'00101xxx'; Set postscaler to
movwf OPTION_REG ; desired WDT rate
bcf STATUS, RP0 ; Bank 0
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 4-2. This precaution must be taken even if the WDT is disabled.

**Example 4-2: Changing Prescaler (WDT → Timer0)**

```assembly
clrwdt ; Clear WDT and postscaler
bsf STATUS, RP0 ; Bank 1
movlw b'xxxx0xxx'; Select Timer0,
    ; prescale, and
    ; clock source
movwf OPTION_REG ;
bcf STATUS, RP0 ; Bank 0
```

<table>
<thead>
<tr>
<th>TABLE 4-1: REGISTERS ASSOCIATED WITH TIMER0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address</td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>01h</td>
</tr>
<tr>
<td>00h/08h</td>
</tr>
<tr>
<td>81h</td>
</tr>
<tr>
<td>85h</td>
</tr>
</tbody>
</table>

Legend: — = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.
5.0 TIMER1 MODULE WITH GATE CONTROL

The PIC12F629/675 devices have a 16-bit timer. Figure 5-1 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt on overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- Optional external enable input (T1G)
- Optional LP oscillator

The Timer1 Control register (T1CON), shown in Register 5-1, is used to enable/disable Timer1 and select the various features of the Timer1 module.

Note: Additional information on timer modules is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

FIGURE 5-1: TIMER1 BLOCK DIAGRAM
5.1 Timer1 Modes of Operation

Timer1 can operate in one of three modes:
- 16-bit timer with prescaler
- 16-bit synchronous counter
- 16-bit asynchronous counter

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

In Counter and Timer modules, the counter/timer clock can be gated by the T1G input.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC w/o CLKOUT), Timer1 can use the LP oscillator as a clock source.

5.2 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit (PIR1<0>) is set. To enable the interrupt on rollover, you must set these bits:
- Timer1 interrupt Enable bit (PIE1<0>)
- PEIE bit (INTCON<6>)
- GIE bit (INTCON<7>).

The interrupt is cleared by clearing the TMR1IF in the Interrupt Service Routine.

5.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4, or 8 divisions of the clock input. The T1CKPS bits (T1CON<5:4>) control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

FIGURE 5-2: TIMER1 INCREMENTING EDGE

- T1CKI = 1 when TMR1 Enabled
- T1CKI = 0 when TMR1 Enabled

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge.
## REGISTER 5-1: T1CON — TIMER1 CONTROL REGISTER (ADDRESS: 10h)

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>TMR1GE</td>
<td>T1CKPS1</td>
<td>T1CKPS0</td>
<td>T1OSCEN</td>
<td>T1SYNC</td>
<td>TMR1CS</td>
<td>TMR1ON</td>
</tr>
</tbody>
</table>

- **bit 7**  
  **Unimplemented**: Read as ‘0’

- **bit 6**  
  **TMR1GE**: Timer1 Gate Enable bit  
  If TMR1ON = 0:  
  This bit is ignored  
  If TMR1ON = 1:  
  1 = Timer1 is on if T1G pin is low  
  0 = Timer1 is on

- **bit 5-4**  
  **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits  
  11 = 1:8 Prescale Value  
  10 = 1:4 Prescale Value  
  01 = 1:2 Prescale Value  
  00 = 1:1 Prescale Value

- **bit 3**  
  **T1OSCEN**: LP Oscillator Enable Control bit  
  If INTOSC without CLKOUT oscillator is active:  
  1 = LP oscillator is enabled for Timer1 clock  
  0 = LP oscillator is off  
  **Else**:  
  This bit is ignored

- **bit 2**  
  **T1SYNC**: Timer1 External Clock Input Synchronization Control bit  
  TMR1CS = 1:  
  1 = Do not synchronize external clock input  
  0 = Synchronize external clock input  
  TMR1CS = 0:  
  This bit is ignored. Timer1 uses the internal clock.

- **bit 1**  
  **TMR1CS**: Timer1 Clock Source Select bit  
  1 = External clock from T1OSO/T1CKI pin (on the rising edge)  
  0 = Internal clock (Fosc/4)

- **bit 0**  
  **TMR1ON**: Timer1 On bit  
  1 = Enables Timer1  
  0 = Stops Timer1

---

Legend:  
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’  
- n = Value at POR  
'1' = Bit is set  
'0' = Bit is cleared  
x = Bit is unknown
5.4 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronously to the internal phase clocks. The timer will continue to run during SLEEP and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 5.4.1).

Note: The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’. The ANSEL register is defined for the PIC12F675.

5.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Examples 12-2 and 12-3 in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023) show how to read and write Timer1 when it is running in Asynchronous mode.

5.5 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 37 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 9-2 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the system clock is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up

While enabled, TRISIO4 and TRISIO5 are set. GP4 and GP5 read ‘0’ and TRISIO4 and TRISIO5 are read ‘1’.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

5.6 Timer1 Operation During SLEEP

Timer1 can only operate during SLEEP when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To setup the timer to wake the device:

- Timer1 must be on (T1CON<0>)
- TMR1IE bit (PIE1<0>) must be set
- PEIE bit (INTCON<6>) must be set

The device will wake-up on an overflow. If the GIE bit (INTCON<7>) is set, the device will wake-up and jump to the Interrupt Service Routine on an overflow.

### TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOD</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Bh/8Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPEIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000</td>
<td>0000 0000u</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>—</td>
<td>—</td>
<td>CMIE</td>
<td>—</td>
<td>—</td>
<td>TMR1IF</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
</tr>
<tr>
<td>0Eh</td>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>—</td>
<td>—</td>
<td>CMIF</td>
<td>—</td>
<td>—</td>
<td>TMR1IE</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
</tr>
<tr>
<td>0Fh</td>
<td>TMR1H</td>
<td>Holding Register for the Least Significant Byte of the 16-bit TMR1 Register</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TMR1H</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>10h</td>
<td>T1CON</td>
<td>—</td>
<td>TMR1GE</td>
<td>T1CKPS1</td>
<td>T1CKPS0</td>
<td>T1OSCEN</td>
<td>T1SYNC</td>
<td>TMR1CS</td>
<td>TMR10N</td>
<td>—000 0000</td>
<td>—uuu uuuu</td>
</tr>
<tr>
<td>8Ch</td>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>—</td>
<td>—</td>
<td>CMIE</td>
<td>—</td>
<td>—</td>
<td>TMR1IE</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
</tr>
</tbody>
</table>

Legend: *x* = unknown, *u* = unchanged, *-* = unimplemented, read as ‘0’. Shaded cells are not used by the Timer1 module.
6.0 COMPARATOR MODULE

The PIC12F629/675 devices have one analog comparator. The inputs to the comparator are multiplexed with the GP0 and GP1 pins. There is an on-chip Comparator Voltage Reference that can also be applied to an input of the comparator. In addition, GP2 can be configured as the comparator output. The Comparator Control Register (CMCON), shown in Register 6-1, contains the bits to control the comparator.

REGISTER 6-1: CMCON — COMPARATOR CONTROL REGISTER (ADDRESS: 19h)

<table>
<thead>
<tr>
<th>bit 7</th>
<th>COUT</th>
<th>CINV</th>
<th>CIS</th>
<th>CM2</th>
<th>CM1</th>
<th>CM0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7 Unimplemented: Read as ‘0’

bit 6 COUT: Comparator Output bit

When CINV = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-

When CINV = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 5 Unimplemented: Read as ‘0’

bit 4 CINV: Comparator Output Inversion bit
1 = Output inverted
0 = Output not inverted

bit 3 CIS: Comparator Input Switch bit
When CM2:CM0 = 110 or 101:
1 = VIN- connects to CIN+
0 = VIN- connects to CIN-

bit 2-0 CM2:CM0: Comparator Mode bits
Figure 6-2 shows the Comparator modes and CM2:CM0 bit settings

Legend:
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as ‘0’
- n = Value at POR     ’1’ = Bit is set     ’0’ = Bit is cleared     x = Bit is unknown
6.1 Comparator Operation

A single comparator is shown in Figure 6-1, along with the relationship between the analog input levels and the digital output. When the analog input at $V_{IN}+$ is less than the analog input $V_{IN}-$, the output of the comparator is a digital low level. When the analog input at $V_{IN}+$ is greater than the analog input $V_{IN}-$, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 6-1 represent the uncertainty due to input offsets and response time.

Note: To use CIN+ and CIN- pins as analog inputs, the appropriate bits must be programmed in the CMCON (19h) register.

The polarity of the comparator output can be inverted by setting the CINV bit (CMCON<4>). Clearing CINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 6-1.

<table>
<thead>
<tr>
<th>Input Conditions</th>
<th>CINV</th>
<th>COUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}- &gt; V_{IN}+$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_{IN}- &lt; V_{IN}+$</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$V_{IN}- &gt; V_{IN}+$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$V_{IN}- &lt; V_{IN}+$</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: CINV bit (CMCON<4>) is clear.
6.2 Comparator Configuration

There are eight modes of operation for the comparator. The CMCON register, shown in Register 6-1, is used to select the mode. Figure 6-2 shows the eight possible modes. The TRISIO register controls the data direction of the comparator pins for each mode. If the comparator mode is changed, the comparator output level may not be valid for a specified period of time. Refer to the specifications in Section 12.0.

**Note:** Comparator interrupts should be disabled during a Comparator mode change. Otherwise, a false interrupt may occur.

**Figure 6-2: Comparator I/O Operating Modes**

<table>
<thead>
<tr>
<th>Comparator Reset (POR Default Value - low power)</th>
<th>Comparator Off (Lowest power)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM2:CM0 = 000</td>
<td>CM2:CM0 = 111</td>
</tr>
<tr>
<td>GP1/CIN-</td>
<td>GP1/CIN-</td>
</tr>
<tr>
<td>GP0/CIN+</td>
<td>GP0/CIN+</td>
</tr>
<tr>
<td>GP2/COUT</td>
<td>GP2/COUT</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Comparator without Output</th>
<th>Comparator w/o Output and with Internal Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM2:CM0 = 010</td>
<td>CM2:CM0 = 100</td>
</tr>
<tr>
<td>GP1/CIN-</td>
<td>GP1/CIN-</td>
</tr>
<tr>
<td>GP0/CIN+</td>
<td>GP0/CIN+</td>
</tr>
<tr>
<td>GP2/COUT</td>
<td>GP2/COUT</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Comparator with Output and Internal Reference</th>
<th>Multiplexed Input with Internal Reference and Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM2:CM0 = 011</td>
<td>CM2:CM0 = 101</td>
</tr>
<tr>
<td>GP1/CIN-</td>
<td>GP1/CIN-</td>
</tr>
<tr>
<td>GP0/CIN+</td>
<td>GP0/CIN+</td>
</tr>
<tr>
<td>GP2/COUT</td>
<td>GP2/COUT</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Comparator with Output</th>
<th>Multiplexed Input with Internal Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM2:CM0 = 001</td>
<td>CM2:CM0 = 110</td>
</tr>
<tr>
<td>GP1/CIN-</td>
<td>GP1/CIN-</td>
</tr>
<tr>
<td>GP0/CIN+</td>
<td>GP0/CIN+</td>
</tr>
<tr>
<td>GP2/COUT</td>
<td>GP2/COUT</td>
</tr>
</tbody>
</table>

A = Analog Input, ports always reads '0'
D = Digital Input
CIS = Comparator Input Switch (CMCON<3>)
6.3 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 6-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latchup may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 6-3: ANALOG INPUT MODE

![Diagram of Analog Input Mode]

Legend:
- CPIN = Input Capacitance
- VT = Threshold Voltage
- ILEAKAGE = Leakage Current at the pin due to Various Junctions
- RIC = Interconnect Resistance
- RS = Source Impedance
- VA = Analog Voltage

6.4 Comparator Output

The comparator output, COUT, is read through the CMCON register. This bit is read only. The comparator output may also be directly output to the GP2 pin in three of the eight possible modes, as shown in Figure 6-2. When in one of these modes, the output on GP2 is asynchronous to the internal clock. Figure 6-4 shows the comparator output block diagram.

The TRISIO<2> bit functions as an output enable/disable for the GP2 pin while the comparator is in an Output mode.

Note 1: When reading the GPIO register, all pins configured as analog inputs will read as a ‘0’. Pins configured as digital inputs will convert an analog input according to the TTL input specification.

Note 2: Analog levels on any pin that is defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 6-4: MODIFIED COMPARATOR OUTPUT BLOCK DIAGRAM

![Diagram of Modified Comparator Output Block Diagram]
6.5 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The internal reference signal is used for four of the eight Comparator modes. The VRCON register, Register 6-2, controls the voltage reference module shown in Figure 6-5.

6.5.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equations determine the output voltages:

\[
\begin{align*}
VRR = 1 \text{ (low range)}: CVREF &= \left(\frac{VR3:VR0}{24}\right) \times VDD \\
VRR = 0 \text{ (high range)}: CVREF &= \left(\frac{VDD}{4}\right) + \left(\frac{VR3:VR0 \times VDD}{32}\right)
\end{align*}
\]

6.5.2 VOLTAGE REFERENCE ACCURACY/ERROR

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 6-5) keep CVREF from approaching VSS or VDD. The Voltage Reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in Section 12.0.

FIGURE 6-5: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

6.6 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is ensured to have a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (Table 12-7).

6.7 Operation During SLEEP

Both the comparator and voltage reference, if enabled before entering SLEEP mode, remain active during SLEEP. This results in higher SLEEP currents than shown in the power-down specifications. The additional current consumed by the comparator and the voltage reference is shown separately in the specifications. To minimize power consumption while in SLEEP mode, turn off the comparator, CM2:CM0 = 111, and voltage reference, VRCON<7> = 0.

While the comparator is enabled during SLEEP, an interrupt will wake-up the device. If the device wakes up from SLEEP, the contents of the CMCON and VRCON registers are not affected.

6.8 Effects of a RESET

A device RESET forces the CMCON and VRCON registers to their RESET states. This forces the comparator module to be in the Comparator Reset mode, CM2:CM0 = 000 and the voltage reference to its off state. Thus, all potential inputs are analog inputs with the comparator and voltage reference disabled to consume the smallest current possible.
6.9 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of the comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<6>, to determine the actual change that has occurred. The CMIF bit, PIR1<3>, is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<3>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON. This will end the mismatch condition.

b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition, and allow flag bit CMIF to be cleared.

Table 6-2: Registers Associated with Comparator Module

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOD</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Bh/8Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>—</td>
<td>—</td>
<td>CMIF</td>
<td>—</td>
<td>—</td>
<td>TMR1IF</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
</tr>
<tr>
<td>19h</td>
<td>CMCON</td>
<td>—</td>
<td>COUT</td>
<td>—</td>
<td>CIN</td>
<td>CM2</td>
<td>CM1</td>
<td>—</td>
<td>CM0</td>
<td>—0-- 0000</td>
<td>0--0 0000</td>
</tr>
<tr>
<td>8Ch</td>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>—</td>
<td>—</td>
<td>CMIE</td>
<td>—</td>
<td>—</td>
<td>TMR1IE</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
</tr>
<tr>
<td>85h</td>
<td>TRISIO</td>
<td>—</td>
<td>—</td>
<td>TRISIO5</td>
<td>TRISIO4</td>
<td>TRISIO3</td>
<td>TRISIO2</td>
<td>TRISIO1</td>
<td>TRISIO0</td>
<td>--11 1111</td>
<td>--11 1111</td>
</tr>
<tr>
<td>99h</td>
<td>VRCON</td>
<td>VREN</td>
<td>VRR</td>
<td>—</td>
<td>VR3</td>
<td>VR2</td>
<td>VR1</td>
<td>VR0</td>
<td>—</td>
<td>0--0 0000</td>
<td>0--0 0000</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the comparator module.
7.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE (PIC12F675 ONLY)

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a 10-bit binary representation of that signal. The PIC12F675 has four analog inputs, multiplexed into one sample and hold circuit.

FIGURE 7-1: A/D BLOCK DIAGRAM

The output of the sample and hold is connected to the input of the converter. The converter generates a binary result via successive approximation and stores the result in a 10-bit register. The voltage reference used in the conversion is software selectable to either VDD or a voltage applied by the VREF pin. Figure 7-1 shows the block diagram of the A/D on the PIC12F675.

7.1 A/D Configuration and Operation

There are two registers available to control the functionality of the A/D module:

1. ADCON0 (Register 7-1)
2. ANSEL (Register 7-2)

7.1.1 ANALOG PORT PINS

The ANS3:ANS0 bits (ANSEL<3:0>) and the TRISO bits control the operation of the A/D port pins. Set the corresponding TRISO bits to set the pin output driver to its high impedance state. Likewise, set the corresponding ANS bit to disable the digital input buffer.

Note: Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

7.1.2 CHANNEL SELECTION

There are four analog channels on the PIC12F675, AN0 through AN3. The CHS1:CHS0 bits (ADCON0<3:2>) control which channel is connected to the sample and hold circuit.

7.1.3 VOLTAGE REFERENCE

There are two options for the voltage reference to the A/D converter: either VDD is used, or an analog voltage applied to VREF is used. The VCFG bit (ADCON0<6>) controls the voltage reference selection. If VCFG is set, then the voltage on the VREF pin is the reference; otherwise, VDD is the reference.

7.1.4 CONVERSION CLOCK

The A/D conversion cycle requires 11 TAD. The source of the conversion clock is software selectable via the ADCS bits (ANSEL<6:4>). There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal RC oscillator)

For correct conversion, the A/D conversion clock (1/TAD) must be selected to ensure a minimum TAD of 1.6 µs. Table 7-1 shows a few TAD calculations for selected frequencies.
TABLE 7-1: \( \text{TAD} \) vs. DEVICE OPERATING FREQUENCIES

<table>
<thead>
<tr>
<th>A/D Clock Source (TAD)</th>
<th>Device Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation</td>
<td>ADCS2:ADCS0</td>
</tr>
<tr>
<td>2 Tosc</td>
<td>000</td>
</tr>
<tr>
<td>4 Tosc</td>
<td>100</td>
</tr>
<tr>
<td>8 Tosc</td>
<td>001</td>
</tr>
<tr>
<td>16 Tosc</td>
<td>101</td>
</tr>
<tr>
<td>32 Tosc</td>
<td>010</td>
</tr>
<tr>
<td>64 Tosc</td>
<td>110</td>
</tr>
<tr>
<td>A/D RC</td>
<td>x11</td>
</tr>
</tbody>
</table>

Legend: Shaded cells are outside of recommended range.

Note 1: The A/D RC source has a typical \( \text{TAD} \) time of 4 \(\mu\)s for \(V_{DD}>3.0\text{V}\).

2: These values violate the minimum required \( \text{TAD} \) time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during SLEEP.

7.1.5 STARTING A CONVERSION

The A/D conversion is initiated by setting the GO/DONE bit (ADCON0<1>). When the conversion is complete, the A/D module:

- Clears the GO/DONE bit
- Sets the ADIF flag (PIR1<6>)
- Generates an interrupt (if enabled).

If the conversion must be aborted, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete A/D conversion sample. Instead, the ADRESH:ADRESL registers will retain the value of the previous conversion. After an aborted conversion, a 2 \( \text{TAD} \) delay is required before another acquisition can be initiated. Following the delay, an input acquisition is automatically started on the selected channel.

Note: The GO/DONE bit should not be set in the same instruction that turns on the A/D.

7.1.6 CONVERSION OUTPUT

The A/D conversion can be supplied in two formats: left or right shifted. The ADFM bit (ADCON0<7>) controls the output format. Figure 7-2 shows the output formats.

FIGURE 7-2: 10-BIT A/D RESULT FORMAT
## REGISTER 7-1: ADCON0 — A/D CONTROL REGISTER (ADDRESS: 1Fh)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value 0</th>
<th>Value 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ADFM: A/D Result Formed Select bit</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1 = Right justified</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Left justified</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>VCFG: Voltage Reference bit</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1 = VREF pin</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = VDD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5-4</td>
<td>Unimplemented: Read as zero</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-2</td>
<td>CHS1:CHS0: Analog Channel Select bits</td>
<td>00</td>
<td>01</td>
</tr>
<tr>
<td></td>
<td>00 = Channel 00 (AN0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01 = Channel 01 (AN1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 = Channel 02 (AN2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>11 = Channel 03 (AN3)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>GO/DONE: A/D Conversion Status bit</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>This bit is automatically cleared by hardware when the A/D conversion has completed.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = A/D conversion completed/not in progress</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>ADON: A/D Conversion STATUS bit</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1 = A/D converter module is operating</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = A/D converter is shut-off and consumes no operating current</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- n = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - x = Bit is unknown

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### REGISTER 7-2: ANSEL — ANALOG SELECT REGISTER (ADDRESS: 9Fh)

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>—</td>
<td>ADCS2</td>
<td>ADCS1</td>
<td>ADCS0</td>
<td>ANS3</td>
<td>ANS2</td>
<td>ANS1</td>
<td>ANS0</td>
</tr>
</tbody>
</table>

- **bit 7**: *Unimplemented*: Read as ‘0’.
- **bit 6-4**: **ADCS<2:0>**: A/D Conversion Clock Select bits
  - 000 = Fosc/2
  - 001 = Fosc/8
  - 010 = Fosc/32
  - 011 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)
  - 100 = Fosc/4
  - 101 = Fosc/16
  - 110 = Fosc/64

- **bit 3-0**: **ANS3:ANS0**: Analog Select bits
  (Between analog or digital function on pins AN<3:0>, respectively.)
  - 1 = Analog input; pin is assigned as analog input\(^{(1)}\)
  - 0 = Digital I/O; pin is assigned to port or special function

\(\text{Note 1}: \) Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change. The corresponding TRISIO bit must be set to Input mode in order to allow external control of the voltage on the pin.

---

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown
7.2 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (C\text{HOLD}) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 7-3. The source impedance (R\text{S}) and the internal sampling switch (R\text{SS}) impedance directly affect the time required to charge the capacitor C\text{HOLD}. The sampling switch (R\text{SS}) impedance varies over the device voltage (V\text{DD}), see Figure 7-3. The maximum recommended impedance for analog sources is 10 k\text{\Omega}. As the impedance is decreased, the acquisition time may be decreased.

After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, \( T_{\text{ACQ}} \), see the PICmicro™ Mid-Range Reference Manual (DS33023).

\[ EQUATION 7-1: \ \text{ACQUISITION TIME} \]

\[
T_{\text{ACQ}} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}
\]

\[
= T_{\text{AMP}} + T_{\text{C}} + T_{\text{COFF}}
\]

\[
= 2\mu s + T_{\text{C}} + \frac{[(\text{Temperature} - 25^\circ \text{C})(0.05\mu s/\circ \text{C})]}{(120pF (1\text{\k}\Omega + 7\text{\k}\Omega + 10\text{\k}\Omega) \ln(1/2047))}
\]

\[
= 16.47\mu s
\]

\[
T_{\text{ACQ}} = 2\mu s + 16.47\mu s + [(50^\circ \text{C} - 25^\circ \text{C})(0.05\mu s/\circ \text{C})]
\]

\[
= 19.72\mu s
\]

\text{Note 1:} \ The reference voltage (V\text{REF}) has no effect on the equation, since it cancels itself out.

\text{Note 2:} \ The charge holding capacitor (C\text{HOLD}) is not discharged after each conversion.

\text{Note 3:} \ The maximum recommended impedance for analog sources is 10 k\text{\Omega}. This is required to meet the pin leakage specification.

\text{Legend:} \ C_{\text{PIN}} = \text{input capacitance} \quad V_T = \text{threshold voltage} \quad I_{\text{LEAKAGE}} = \text{leakage current at the pin due to various junctions} \quad R_{\text{IC}} = \text{interconnect resistance} \quad R_{\text{SS}} = \text{sampling switch} \quad C_{\text{HOLD}} = \text{sample/hold capacitance (from DAC)}
7.3 A/D Operation During SLEEP

The A/D converter module can operate during SLEEP. This requires the A/D clock source to be set to the internal RC oscillator. When the RC clock source is selected, the A/D waits one instruction before starting the conversion. This allows the SLEEP instruction to be executed, thus eliminating much of the switching noise from the conversion. When the conversion is complete, the GO/DONE bit is cleared, and the result is loaded into the ADRESH:ADRESL registers. If the A/D interrupt is enabled, the device awakens from SLEEP. If the A/D interrupt is not enabled, the A/D module is turned off, although the ADON bit remains set.

When the A/D clock source is something other than RC, a SLEEP instruction causes the present conversion to be aborted, and the A/D module is turned off. The ADON bit remains set.

7.4 Effects of RESET

A device RESET forces all registers to their RESET state. Thus the A/D module is turned off and any pending conversion is aborted. The ADRESH:ADRESL registers are unchanged.

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOD</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>05h</td>
<td>GPIO</td>
<td>—</td>
<td>—</td>
<td>GPIO5</td>
<td>GPIO4</td>
<td>GPIO3</td>
<td>GPIO2</td>
<td>GPIO1</td>
<td>GPIO0</td>
<td>— — — — — — — —</td>
<td>— — — — — — — —</td>
</tr>
<tr>
<td>0Bh, 8Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPF</td>
<td>0000 0000</td>
<td>0000 000u</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>—</td>
<td>—</td>
<td>CMIF</td>
<td>—</td>
<td>—</td>
<td>TMRI1F</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
</tr>
<tr>
<td>1Eh</td>
<td>ADRESH</td>
<td>ADRESH</td>
<td>Most Significant 8 bits of the Left Shifted A/D result or 2 bits of the Right Shifted Result</td>
<td>xxxx xxxx</td>
<td>xxxx xxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1Fh</td>
<td>ADCON0</td>
<td>ADFM</td>
<td>VCFG</td>
<td>—</td>
<td>—</td>
<td>CHS1</td>
<td>CHS0</td>
<td>GO</td>
<td>ADON</td>
<td>00-- 0000</td>
<td>00-- 0000</td>
</tr>
<tr>
<td>85h</td>
<td>TRISIO</td>
<td>—</td>
<td>—</td>
<td>TRISIO5</td>
<td>TRISIO4</td>
<td>TRISIO3</td>
<td>TRISIO2</td>
<td>TRISIO1</td>
<td>TRISIO0</td>
<td>— — — —</td>
<td>— — — —</td>
</tr>
<tr>
<td>8Ch</td>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>—</td>
<td>—</td>
<td>CMIE</td>
<td>—</td>
<td>—</td>
<td>TMRI1E</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
</tr>
<tr>
<td>9Eh</td>
<td>ADRESL</td>
<td>ADRESL</td>
<td>Least Significant 2 bits of the Left Shifted A/D Result or 8 bits of the Right Shifted Result</td>
<td>xxxx xxxx</td>
<td>xxxx xxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9Fh</td>
<td>ANSEL</td>
<td>—</td>
<td>—</td>
<td>ADCS2</td>
<td>ADCS1</td>
<td>ADCS0</td>
<td>ANS3</td>
<td>ANS2</td>
<td>ANS1</td>
<td>ANS0</td>
<td>— — — —</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D converter module.
8.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC12F629/675 devices have 128 bytes of data EEPROM with an address range from 0h to 7Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip to chip. Please refer to AC Specifications for exact limits.

When the data memory is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

Additional information on the Data EEPROM is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

---

**REGISTER 8-1: EEDAT — EEPROM DATA REGISTER (ADDRESS: 9Ah)**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEDAT7</td>
<td>EEDAT6</td>
<td>EEDAT5</td>
<td>EEDAT4</td>
<td>EEDAT3</td>
<td>EEDAT2</td>
<td>EEDAT1</td>
<td>EEDAT0</td>
</tr>
</tbody>
</table>

bit 7-0 **EEDATn**: Byte value to write to or read from Data EEPROM

---

Legend:

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’  
- n = Value at POR  
’1’ = Bit is set  
’0’ = Bit is cleared  
x = Bit is unknown

---

**REGISTER 8-2: EEADR — EEPROM ADDRESS REGISTER (ADDRESS: 9Bh)**

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>EADR6</td>
<td>EADR5</td>
<td>EADR4</td>
<td>EADR3</td>
<td>EADR2</td>
<td>EADR1</td>
<td>EADR0</td>
</tr>
</tbody>
</table>

bit 7-0  
**Unimplemented**: Should be set to ‘0’

---

**EEADR**: Specifies one of 128 locations for EEPROM Read/Write Operation

---

Legend:

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’  
- n = Value at POR  
’1’ = Bit is set  
’0’ = Bit is cleared  
x = Bit is unknown
8.1  EEA DR

The EEA DR register can address up to a maximum of 128 bytes of data EEPROM. Only seven of the eight bits in the register (EEADR<6:0>) are required. The MSb (bit 7) is ignored.

The upper bit should always be ‘0’ to remain upward compatible with devices that have more data EEPROM memory.

8.2  EECO N1 AND EECO N2 REGISTERS

EECON1 is the control register with four low order bits physically implemented. The upper four bits are non-implemented and read as ‘0’s.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset, or a WDT Time-out Reset during normal operation. In these situations, following RESET, the user can check the WRERR bit, clear it, and rewrite the location.

The data and address will be cleared, therefore, the EEDATA and EEA DR registers will need to be re-initialized.

Interrupt flag bit EEIF in the PIR1 register is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all ‘0’s. The EECON2 register is used exclusively in the Data EEPROM write sequence.

REGISTER 8-3:  EECO N1 — EEPROM CONTROL REGISTER (ADDRESS: 9Ch)

<table>
<thead>
<tr>
<th>U-0 U-0 U-0</th>
<th>R/W-x</th>
<th>R/W-0</th>
<th>R/S-0</th>
<th>R/S-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7-4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WRERR: EEPROM Error Flag bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = A write operation is prematurely terminated (any MCLR Reset, any WDT Reset during normal operation or BOD detect)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = The write operation completed</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WREN: EEPROM Write Enable bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = Allows write cycles</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Inhibits write to the data EEPROM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WR: Write Control bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Write cycle to the data EEPROM is complete</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD: Read Control bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Does not initiate an EEPROM read</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
S = Bit can only be set
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown
8.3 READING THE EEPROM DATA MEMORY

To read a data memory location, the user must write the address to the EEARDR register and then set control bit RD (EECON1<0>), as shown in Example 8-1. The data is available, in the very next cycle, in the EEDATA register. Therefore, it can be read in the next instruction. EEDATA holds this value until another read, or until it is written to by the user (during a write operation).

**EXAMPLE 8-1: DATA EEPROM READ**

```plaintext
bsf STATUS,RP0 ;Bank 1
movlw CONFIG_ADDR ;
movwf EEARDR ;Address to read
bsf EECON1,RD ;EE Read
movf EEDATA,W ;Move data to W
```

8.4 WRITING TO THE EEPROM DATA MEMORY

To write an EEPROM data location, the user must first write the address to the EEARDR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 8-2.

**EXAMPLE 8-2: DATA EEPROM WRITE**

```plaintext
bsf STATUS,RP0 ;Bank 1
bsf EECON1,WREN ;Enable write
bcf INTCON,W ;Disable INTs
movlw 55h ;Unlock write
movwf EECON2 ;
movlw AAh ;
movwf EECON1 ;
bsf EECON1,WR ;Start the write
bsf INTCON,GIE ;Enable INTs
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit (PIR<7>) register must be cleared by software.

8.5 WRITE VERIFY

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (see Example 8-3) to the desired value to be written.

**EXAMPLE 8-3: WRITE VERIFY**

```plaintext
bcf STATUS,RP0 ;Bank 0 
:"Any code
bsf STATUS,RP0 ;Bank 1 READ
movf EEDATA,W ;EEDATA not changed
:"from previous write
bsf EECON1,RD ;YES, Read the
:"value written
xorwf EEDATA,W ;Is data the same
btfss STATUS,Z ;Is data the same
goto WRITE_ERR ;No, handle error
:"Yes, continue
```

8.6 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the device may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On-power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

- brown-out
- power glitch
- software malfunction
8.7 DATA EEPROM OPERATION DURING CODE PROTECT

Data memory can be code protected by programming the CPD bit to ‘0’.

When the data memory is code protected, the CPU is able to read and write data to the Data EEPROM. It is recommended to code protect the program memory when code protecting data memory. This prevents anyone from programming zeroes over the existing code (which will execute as NOPs) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations to ‘0’ will also help prevent data memory code protection from becoming breached.

TABLE 8-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOD</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>—</td>
<td>—</td>
<td>CMIF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>00—0</td>
<td>00—0</td>
</tr>
<tr>
<td>9Ah</td>
<td>EEDATA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>00000000</td>
<td>00000000</td>
</tr>
<tr>
<td>9Bh</td>
<td>EEADR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
<td>—000</td>
<td>—000</td>
</tr>
<tr>
<td>9Ch</td>
<td>EECON1(1)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WR</td>
<td>RD</td>
<td>—</td>
<td>—000</td>
<td>—000</td>
</tr>
<tr>
<td>9Dh</td>
<td>EECON2(1)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—000</td>
<td>—000</td>
</tr>
</tbody>
</table>

Legend:  x = unknown,  u = unchanged,  - = unimplemented read as ‘0’,  q = value depends upon condition.

Shaded cells are not used by Data EEPROM module.

Note 1: EECON2 is not a physical register.
9.0  SPECIAL FEATURES OF THE CPU

Certain special circuits that deal with the needs of real time applications are what sets a microcontroller apart from other processors. The PIC12F629/675 family has a host of such features intended to:

- maximize system reliability
- minimize cost through elimination of external components
- provide power saving operating modes and offer code protection.

These features are:

- Oscillator selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Detect (BOD)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID Locations
- In-Circuit Serial Programming

The PIC12F629/675 has a Watchdog Timer that is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can provide at least a 72 ms RESET. With these three functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through:

- External RESET
- Watchdog Timer wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options (see Register 9-1).
9.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations, as shown in Register 9-1. These bits are mapped in program memory location 2007h.

REGISTER 9-1: CONFIG — CONFIGURATION WORD (ADDRESS: 2007h)

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>U-0</th>
<th>U-0</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>BG1</td>
<td>BG0</td>
<td></td>
<td></td>
<td>CPD</td>
<td>CP</td>
<td>BODEN</td>
<td>MCLRE</td>
<td>PWRT</td>
<td>WDE</td>
<td>FOSC2</td>
<td>FOSC1</td>
</tr>
</tbody>
</table>

**bit 13-12**  **BG1:BG0**: Bandgap Calibration bits for BOD and POR voltage(1)
- 00 = Lowest bandgap voltage
- 11 = Highest bandgap voltage

**bit 11-9**  **Unimplemented**: Read as ‘0’

**bit 8**  **CPD**: Data Code Protection bit(2)
- 1 = Data memory code protection is disabled
- 0 = Data memory code protection is enabled

**bit 7**  **CP**: Code Protection bit(3)
- 1 = Program Memory code protection is disabled
- 0 = Program Memory code protection is enabled

**bit 6**  **BODEN**: Brown-out Detect Enable bit(4)
- 1 = BOD enabled
- 0 = BOD disabled

**bit 5**  **MCLRE**: GP3/MCLR pin function select(5)
- 1 = GP3/MCLR pin function is MCLR
- 0 = GP3/MCLR pin function is digital I/O, MCLR internally tied to VDD

**bit 4**  **PWRT**: Power-up Timer Enable bit
- 1 = PWRT disabled
- 0 = PWRT enabled

**bit 3**  **WDTE**: Watchdog Timer Enable bit
- 1 = WDT enabled
- 0 = WDT disabled

**bit 2-0**  **FOSC2:FOSC0**: Oscillator Selection bits
- 111 = RC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
- 110 = RC oscillator: I/O function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
- 101 = INTOSC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
- 100 = INTOSC oscillator: I/O function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
- 011 = EC: I/O function on GP4/OSC2/CLKOUT pin, CLkin on GP5/OSC1/CLKIN
- 010 = HS oscillator: High speed crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
- 001 = XT oscillator: Crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
- 000 = LP oscillator: Low power crystal on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

**Note 1**: The Bandgap Calibration bits are factory programmed and must be read and saved prior to erasing the device as specified in the PIC12F629/675 Programming Specification. These bits are reflected in an export of the configuration word. Microchip Development Tools maintain all calibration bits to factory settings.

**2**: The entire data EEPROM will be erased when the code protection is turned off.

**3**: The entire program memory will be erased, including OSCCAL value, when the code protection is turned off.

**4**: Enabling Brown-out Detect does not automatically enable Power-up Timer.

**5**: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

Legend:
P = Programmed using ICSP  
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’  
-n = Value at POR  
1 = bit is set  
0 = bit is cleared  
x = bit is unknown

Note: Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h - 3FFFh), which can be accessed only during programming. See PIC12F629/675 Programming Specification for more information.
9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC12F629/675 can be operated in eight different oscillator option modes. The user can program three configuration bits (FOSC2 through FOSC0) to select one of these eight modes:

- **LP** Low Power Crystal
- **XT** Crystal/Resonator
- **HS** High Speed Crystal/Resonator
- **RC** External Resistor/Capacitor (2 modes)
- **INTOSC** Internal Oscillator (2 modes)
- **EC** External Clock In

### Note:
Additional information on oscillator configurations is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (see Figure 9-1). The PIC12F629/675 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may yield a frequency outside of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (see Figure 9-2).

### FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) HS, XT OR LP OSC CONFIGURATION

![Crystal Oscillator Diagram](image)

**Note:**
1. See Table 9-1 and Table 9-2 for recommended values of C1 and C2.
2. A series resistor may be required for AT strip cut crystals.
3. RF varies with the Oscillator mode selected (Approx. value = 10 MΩ).

### FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT, EC, OR LP OSC CONFIGURATION)

![External Clock Input Diagram](image)

**Note 1:** Functions as GP4 in EC Osc mode.

### TABLE 9-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

<table>
<thead>
<tr>
<th>Mode</th>
<th>Freq</th>
<th>OSC1(C1)</th>
<th>OSC2(C2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XT</td>
<td>455 kHz</td>
<td>68 - 100 pF</td>
<td>68 - 100 pF</td>
</tr>
<tr>
<td></td>
<td>2.0 MHz</td>
<td>15 - 68 pF</td>
<td>15 - 68 pF</td>
</tr>
<tr>
<td></td>
<td>4.0 MHz</td>
<td>15 - 68 pF</td>
<td>15 - 68 pF</td>
</tr>
<tr>
<td>HS</td>
<td>8.0 MHz</td>
<td>10 - 68 pF</td>
<td>10 - 68 pF</td>
</tr>
<tr>
<td></td>
<td>16.0 MHz</td>
<td>10 - 22 pF</td>
<td>10 - 22 pF</td>
</tr>
</tbody>
</table>

**Note 1:** Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

### TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

<table>
<thead>
<tr>
<th>Mode</th>
<th>Freq</th>
<th>OSC1(C1)</th>
<th>OSC2(C2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP</td>
<td>32 kHz</td>
<td>68 - 100 pF</td>
<td>68 - 100 pF</td>
</tr>
<tr>
<td>XT</td>
<td>100 kHz</td>
<td>68 - 150 pF</td>
<td>150 - 200 pF</td>
</tr>
<tr>
<td></td>
<td>2 MHz</td>
<td>15 - 30 pF</td>
<td>15 - 30 pF</td>
</tr>
<tr>
<td></td>
<td>4 MHz</td>
<td>15 - 30 pF</td>
<td>15 - 30 pF</td>
</tr>
<tr>
<td>HS</td>
<td>8 MHz</td>
<td>15 - 30 pF</td>
<td>15 - 30 pF</td>
</tr>
<tr>
<td></td>
<td>10 MHz</td>
<td>15 - 30 pF</td>
<td>15 - 30 pF</td>
</tr>
<tr>
<td></td>
<td>20 MHz</td>
<td>15 - 30 pF</td>
<td>15 - 30 pF</td>
</tr>
</tbody>
</table>

**Note 1:** Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
9.2.3 EXTERNAL CLOCK IN

For applications where a clock is already available elsewhere, users may directly drive the PIC12F629/675 provided that this external clock source meets the AC/DC timing requirements listed in Section 12.0. Figure 9-2 shows how an external clock circuit should be configured.

9.2.4 RC OSCILLATOR

For applications where precise timing is not a requirement, the RC oscillator option is available. The operation and functionality of the RC oscillator is dependent upon a number of variables. The RC oscillator frequency is a function of:

- Supply voltage
- Resistor (R<sub>EXT</sub>) and capacitor (C<sub>EXT</sub>) values
- Operating temperature.

The oscillator frequency will vary from unit to unit due to normal process parameter variation. The difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C<sub>EXT</sub> values. The user also needs to account for the tolerance of the external R and C components.

Two options are available for this Oscillator mode which allow GP4 to be used as a general purpose I/O or to output Fosc/4.

9.2.5 INTERNAL 4 MHz OSCILLATOR

When calibrated, the internal oscillator provides a fixed 4 MHz (nominal) system clock. See Electrical Specifications, Section 12.0, for information on variation over voltage and temperature.

Two options are available for this Oscillator mode which allow GP4 to be used as a general purpose I/O or to output Fosc/4.

9.2.5.1 Calibrating the Internal Oscillator

A calibration instruction is programmed into the last location of program memory. This instruction is a RETLW XX, where the literal is the calibration value. The literal is placed in the OSCCAL register to set the calibration of the internal oscillator. Example 9-1 demonstrates how to calibrate the internal oscillator. For best operation, decouple (with capacitance) V<sub>DD</sub> and V<sub>SS</sub> as close to the device as possible.

**Note:** Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be saved prior to erasing part as specified in the PIC12F629/675 Programming specification. Microchip Development Tools maintain all calibration bits to factory settings.

**EXAMPLE 9-1: CALIBRATING THE INTERNAL OSCILLATOR**

bsf STATUS, RP0 ;Bank 1
call 3FFh ;Get the cal value
movwf OSCCAL ;Calibrate
bcf STATUS, RP0 ;Bank 0

9.2.6 CLKOUT

The PIC12F629/675 devices can be configured to provide a clock out signal in the INTOSC and RC oscillator modes. When configured, the oscillator frequency divided by four (Fosc/4) is output on the GP4/OSC2/CLKOUT pin. Fosc/4 can be used for test purposes or to synchronize other logic.
9.3 **RESET**

The PIC12F629/675 differentiates between various kinds of RESET:

a) Power-on Reset (POR)
b) WDT Reset during normal operation
c) WDT Reset during SLEEP
d) MCLR Reset during normal operation
e) MCLR Reset during SLEEP
f) Brown-out Detect (BOD)

Some registers are not affected in any RESET condition; their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a “RESET state” on:

- Power-on Reset
- MCLR Reset
- WDT Reset
- WDT Reset during SLEEP
- Brown-out Detect (BOD) Reset

They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. To and PD bits are set or cleared differently in different RESET situations as indicated in Table 9-4. These bits are used in software to determine the nature of the RESET. See Table 9-7 for a full description of RESET states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 9-4.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See Table 12-4 in Electrical Specifications Section for pulse width specification.

**FIGURE 9-4: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**

---

**Note 1:** This is a separate oscillator from the INTOSC/EC oscillator.
9.3.1 MCLR

PIC12F629/675 devices have a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

The behavior of the ESD protection on the MCLR pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event.

For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 9-5, is suggested.

An internal MCLR option is enabled by setting the MCLRE bit in the configuration word. When enabled, MCLR is internally tied to VDD. No internal pull-up option is available for the MCLR pin.

**FIGURE 9-5: RECOMMENDED MCLR CIRCUIT**

![MCLR Circuit Diagram]

9.3.2 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in RESET until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply tie the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details (see Section 12.0). If the BOD is enabled, the maximum rise time specification does not apply. The BOD circuitry will keep the device in RESET until VDD reaches VBOD (see Section 9.3.5).

**Note:** The POR circuit does not produce an internal RESET when VDD declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

9.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Detect. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, PWRT can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Detect is enabled.

The Power-up Time delay will vary from chip to chip and due to:

- VDD variation
- Temperature variation
- Process variation.

See DC parameters for details (Section 12.0).

9.3.4 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

For additional information, refer to Application Note AN607 “Power-up Trouble Shooting”.

Note: The POR circuit does not produce an internal RESET when VDD declines.
9.3.5 BROWN-OUT DETECT (BOD)

The PIC12F629/675 members have on-chip Brown-out Detect circuitry. A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Detect circuitry. If V\textsubscript{DD} falls below V\textsubscript{BOD} for greater than parameter (T\textsubscript{BOD}) in Table 12-4 (see Section 12.0), the Brown-out situation will reset the device. This will occur regardless of V\textsubscript{DD} slew-rate. A RESET is not guaranteed to occur if V\textsubscript{DD} falls below V\textsubscript{BOD} for less than parameter (T\textsubscript{BOD}).

On any RESET (Power-on, Brown-out, Watchdog, etc.), the chip will remain in RESET until V\textsubscript{DD} rises above BV\textsubscript{DD} (see Figure 9-6). The Power-up Timer will now be invoked, if enabled, and will keep the chip in RESET an additional 72 ms.

**Note:** A Brown-out Detect does not enable the Power-up Timer if the PWRTE bit in the configuration word is set.

If V\textsubscript{DD} drops below BV\textsubscript{DD} while the Power-up Timer is running, the chip will go back into a Brown-out Detect and the Power-up Timer will be re-initialized. Once V\textsubscript{DD} rises above BV\textsubscript{DD}, the Power-up Timer will execute a 72 ms RESET.

**FIGURE 9-6: BROWN-OUT SITUATIONS**

![Brown-out Situations Diagram]

**Note 1:** 72 ms delay only if PWRTE bit is programmed to ‘0’.

9.3.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired. Then, OST is activated. The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 9-7, Figure 9-8 and Figure 9-9 depict time-out sequences.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately (see Figure 9-8). This is useful for testing purposes or to synchronize more than one PIC12F629/675 device operating in parallel.

Table 9-6 shows the RESET conditions for some special registers, while Table 9-7 shows the RESET conditions for all the registers.

9.3.7 POWER CONTROL (PCON) STATUS REGISTER

The power CONTROL/STATUS register, PCON (address 8Eh) has two bits.

Bit0 is BOD (Brown-out). BOD is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if BOD = 0, indicating that a brown-out has occurred. The BOD STATUS bit is a don’t care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a ‘0’ on Power-on Reset and unaffected otherwise. The user must write a ‘1’ to this bit following a Power-on Reset. On a subsequent RESET, if POR is ‘0’, it will indicate that a Power-on Reset must have occurred (i.e., V\textsubscript{DD} may have gone too low).
### TABLE 9-3: TIME-OUT IN VARIOUS SITUATIONS

<table>
<thead>
<tr>
<th>Oscillator Configuration</th>
<th>Power-up</th>
<th>Brown-out Detect</th>
<th>Wake-up from SLEEP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PWRTE = 0</td>
<td>PWRTE = 1</td>
<td></td>
</tr>
<tr>
<td>XT, HS, LP</td>
<td>TPWRT + 1024*TOSC</td>
<td>1024*TOSC</td>
<td>1024*Tosc</td>
</tr>
<tr>
<td>RC, EC, INTOSC</td>
<td>TPWRT</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

### TABLE 9-4: STATUS/PCON BITS AND THEIR SIGNIFICANCE

<table>
<thead>
<tr>
<th>POR</th>
<th>BOD</th>
<th>TO</th>
<th>PD</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>u</td>
<td>1</td>
<td>1</td>
<td>Power-on Reset</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Brown-out Detect</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>u</td>
<td>WDT Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>0</td>
<td>WDT Wake-up</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>MCLR Reset during normal operation</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>1</td>
<td>0</td>
<td>MCLR Reset during SLEEP</td>
</tr>
</tbody>
</table>

Legend: u = unchanged, x = unknown

### TABLE 9-5: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOD</th>
<th>Value on all other RESETS(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>03h</td>
<td>STATUS</td>
<td>IRP</td>
<td>RP1</td>
<td>RPO</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>0001 1xxx</td>
<td>000q quuuu</td>
</tr>
<tr>
<td>8 Eh</td>
<td>PCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>POR</td>
<td>BOD</td>
<td>---- --0x ---- --q</td>
</tr>
</tbody>
</table>

Legend: u = unchanged, x = unknown, _ = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** Other (non Power-up) Resets include MCLR Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

### TABLE 9-6: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

<table>
<thead>
<tr>
<th>Condition</th>
<th>Program Counter</th>
<th>STATUS Register</th>
<th>PCON Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-on Reset</td>
<td>000h</td>
<td>0001 1xxx</td>
<td>---- --0x</td>
</tr>
<tr>
<td>MCLR Reset during normal operation</td>
<td>000h</td>
<td>000u uuuu</td>
<td>---- --uu</td>
</tr>
<tr>
<td>MCLR Reset during SLEEP</td>
<td>000h</td>
<td>0001 0uuu</td>
<td>---- --uu</td>
</tr>
<tr>
<td>WDT Reset</td>
<td>000h</td>
<td>0000 uuuu</td>
<td>---- --uu</td>
</tr>
<tr>
<td>WDT Wake-up</td>
<td>PC + 1</td>
<td>uuu0 0uuu</td>
<td>---- --uu</td>
</tr>
<tr>
<td>Brown-out Detect</td>
<td>000h</td>
<td>0001 1uuu</td>
<td>---- --10</td>
</tr>
<tr>
<td>Interrupt Wake-up from SLEEP</td>
<td>PC + 1(1)</td>
<td>uuul 0uuu</td>
<td>---- --uu</td>
</tr>
</tbody>
</table>

Legend: u = unchanged, x = unknown, _ = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and global enable bit GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

---

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## TABLE 9-7: INITIALIZATION CONDITION FOR REGISTERS

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
<th>Power-on Reset</th>
<th>MCLR Reset during normal operation</th>
<th>MCLR Reset during SLEEP</th>
<th>WDT Reset</th>
<th>Brown-out Detect(1)</th>
<th>Wake-up from SLEEP through interrupt</th>
<th>Wake-up from SLEEP through WDT time-out</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>—</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>INDF</td>
<td>00h/80h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>TMR0</td>
<td>01h</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PCL</td>
<td>02h/82h</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td>PC + 1(3)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>STATUS</td>
<td>03h/83h</td>
<td>0001 1xxx</td>
<td>000q quuu</td>
<td>yyyy quuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>FSR</td>
<td>04h/84h</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>GPIO</td>
<td>05h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PCLATH</td>
<td>0Ah/8Ah</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>INTCON</td>
<td>08h/88h</td>
<td>0000 0000</td>
<td>0000 000u</td>
<td>yyyy quqq</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PIR1</td>
<td>0Ch</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
<td>qq-- q--q</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>T1CON</td>
<td>10h</td>
<td>-000 0000</td>
<td>-uuu uuuu</td>
<td>-uuu uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>CMCON</td>
<td>19h</td>
<td>-0-0 0000</td>
<td>-0-0 0000</td>
<td>-u-u uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>ADRESH</td>
<td>1Eh</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>ADCON0</td>
<td>1Fh</td>
<td>00-- 0000</td>
<td>00-- 0000</td>
<td>uu-- uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>81h</td>
<td>1111 1111</td>
<td>1111 1111</td>
<td>yyyy uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>TRISIO</td>
<td>85h</td>
<td>--11 1111</td>
<td>--11 1111</td>
<td>--uu uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PIE1</td>
<td>8Ch</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
<td>uu-- u--u</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PCON</td>
<td>8Eh</td>
<td>----- --0x</td>
<td>----- --uu(1,6)</td>
<td>----- --uu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>OSCCAL</td>
<td>90h</td>
<td>1000 00--</td>
<td>1000 00--</td>
<td>yyyy uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>WPU</td>
<td>95h</td>
<td>--11 --111</td>
<td>--11 --111</td>
<td>yyyy uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>IOC</td>
<td>96h</td>
<td>--00 0000</td>
<td>--00 0000</td>
<td>--uu uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>VRCON</td>
<td>99h</td>
<td>0-0- 0000</td>
<td>0-0- 0000</td>
<td>u-u- uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>EEDATA</td>
<td>9Ah</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td>yyyy uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>EEADR</td>
<td>9Bh</td>
<td>-000 0000</td>
<td>-000 0000</td>
<td>-uuu uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>EECON1</td>
<td>9Ch</td>
<td>----- x000</td>
<td>----- q000</td>
<td>---- uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>EECON2</td>
<td>9Dh</td>
<td>----- -----</td>
<td>----- -----</td>
<td>---- ----</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>ADRESL</td>
<td>9Eh</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>yyyy yyyy</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>ANSEL</td>
<td>9Fh</td>
<td>-000 1111</td>
<td>-000 1111</td>
<td>-uuu uuuu</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:  
- u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 9-6 for RESET value for specific condition.

5: If wake-up was due to data EEPROM write completing, Bit 7 = 1; A/D conversion completing, Bit 6 = 1; Comparator input changing, bit 3 = 1; or Timer1 rolling over, bit 0 = 1. All other interrupts generating a wake-up will cause these bits to = u.

6: If RESET was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.
FIGURE 9-7: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

VDD
MCLR
Internal POR

PWRT Time-out

OST Time-out

Internal RESET

FIGURE 9-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2

VDD
MCLR
Internal POR

PWRT Time-out

OST Time-out

Internal RESET

FIGURE 9-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

VDD
MCLR
Internal POR

PWRT Time-out

OST Time-out

Internal RESET
9.4 Interrupts

The PIC12F629/675 has 7 sources of interrupt:

- External Interrupt GP2/INT
- TMR0 Overflow Interrupt
- GPIO Change Interrupts
- Comparator Interrupt
- A/D Interrupt (PIC12F675 only)
- TMR1 Overflow Interrupt
- EEPROM Data Write Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt register (PIR) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register and PIE register. GIE is cleared on RESET.

The return from interrupt instruction, RETFIE, exits interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT pin interrupt
- GP port change interrupt
- TMR0 overflow interrupt

The peripheral interrupt flags are contained in the special register PIR1. The corresponding interrupt enable bit is contained in Special Register PIE1.

The following interrupt flags are contained in the PIR register:

- EEPROM data write interrupt
- A/D interrupt
- Comparator interrupt
- Timer1 overflow interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt
- The return address is pushed onto the stack
- The PC is loaded with 0004h

Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

**Note 1:** Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

**Note 2:** When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts which were ignored are still pending to be serviced when the GIE bit is set again.
FIGURE 9-10: INTERRUPT LOGIC

Note 1: PIC12F675 only.
9.4.1 GP2/INT INTERRUPT

External interrupt on GP2/INT pin is edge-triggered; either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The GP2/INT interrupt can wake-up the processor from SLEEP if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.7 for details on SLEEP and Figure 9-13 for timing of wake-up from SLEEP through GP2/INT interrupt.

Note: The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’. The ANSEL register is defined for the PIC12F675.

9.4.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set the TOIF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 4.0.

9.4.3 GPIO INTERRUPT

An input change on GPIO change sets the GPIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the GPIE (INTCON<3>) bit. Plus individual pins can be configured through the IOC register.

9.4.4 COMPARATOR INTERRUPT

See Section 6.9 for description of comparator interrupt.

9.4.5 A/D CONVERTER INTERRUPT

After a conversion is complete, the ADIF flag (PIR<6>) is set. The interrupt can be enabled/disabled by setting/clearing the ADIE (PIE<6>) bit. See Section 7.0 for operation of the A/D converter interrupt.

FIGURE 9-11: INT PIN INTERRUPT TIMING

Note 1: INTF flag is sampled here (every Q1).
2: Asynchronous interrupt latency = 3-4 Tcy. Synchronous latency = 3 Tcy, where Tcy = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in RC Oscillator mode.
4: For minimum width of INT pulse, refer to AC specs.
5: INTF is enabled to be set any time during the Q4-Q1 cycles.
TABLE 9-8: SUMMARY OF INTERRUPT REGISTERS

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOD</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Bh, 8Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TOIE</td>
<td>INTE</td>
<td>GPIE</td>
<td>TOIF</td>
<td>INTF</td>
<td>GIFF</td>
<td>0000 0000</td>
<td>0000 000u</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>—</td>
<td>—</td>
<td>CMIF</td>
<td>—</td>
<td>—</td>
<td>TMR1IF</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
</tr>
<tr>
<td>8Ch</td>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>—</td>
<td>—</td>
<td>CMIE</td>
<td>—</td>
<td>—</td>
<td>TMR1IE</td>
<td>00-- 0--0</td>
<td>00-- 0--0</td>
</tr>
</tbody>
</table>

Legend:  x = unknown,  u = unchanged,  - = unimplemented read as '0',  q = value depends upon condition.  
Shaded cells are not used by the Interrupt module.

9.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt, e.g., W register and STATUS register. This must be implemented in software.

Example 9-2 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 9-2:

- Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- Restores the W register

EXAMPLE 9-2: SAVING THE STATUS AND W REGISTERS IN RAM

```assembly
MOVWF W_TEMP ; copy W to temp register, could be in either bank
SWAPF STATUS,W ; swap status to be saved into W
BCF STATUS,RP0 ; change to bank 0 regardless of current bank
MOVWF STATUS_TEMP ; save status to bank 0 register
: ; (ISR)
: SWAPF STATUS_TEMP,W; swap STATUS_TEMP register into W, sets bank to original state
MOVWF STATUS ; move W into STATUS register
SWAPF W_TEMP,F ; swap W_TEMP
SWAPF W_TEMP,W ; swap W_TEMP into W
```

9.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which requires no external components. This RC oscillator is separate from the external RC oscillator of the CLKIN pin and INTOSC. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped (for example, by execution of a SLEEP instruction). During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

9.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWD and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET. The T0 bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

9.6.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (i.e., VDD = Min., Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time-out occurs.
**FIGURE 9-12: WATCHDOG TIMER BLOCK DIAGRAM**

```
CLKOUT (= Fosc/4)

T0CKI
pin
T0SE
T0CS

0
1

0
1

PS0 - PS2

8-bit
Prescaler

PSA

0
1

PSA

SYNC 2
8 Cycles

Set Flag bit T0IF
on Overflow

TMR0

Data Bus

Watchdog
Timer

WDTE

Note 1: T0SE, T0CS, PSA, PS0-PS2 are bits in the Option register.
```

**TABLE 9-9: SUMMARY OF WATCHDOG TIMER REGISTERS**

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOD</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>81h</td>
<td>OPTION_REG</td>
<td>GPPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>2007h</td>
<td>Config. bits</td>
<td>CP</td>
<td>BODEN</td>
<td>MCLRE</td>
<td>PWRTE</td>
<td>WDTE</td>
<td>F0SC2</td>
<td>F0SC1</td>
<td>F0SC0</td>
<td>uuuu uuuu</td>
<td>uuuu uuuu</td>
</tr>
</tbody>
</table>

Legend: u = Unchanged, shaded cells are not used by the Watchdog Timer.
9.7 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If the Watchdog Timer is enabled:
- WDT will be cleared but keeps running
- PD bit in the STATUS register is cleared
- TO bit is set
- Oscillator driver is turned off
- I/O ports maintain the status they had before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin and the comparators and CVREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on GPIO should be considered.

The MCLR pin must be at a logic high level (VIHMC).

**Note:** It should be noted that a RESET generated by a WDT time-out does not drive MCLR pin low.

9.7.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External RESET input on MCLR pin
2. Watchdog Timer Wake-up (if WDT was enabled)
3. Interrupt from GP2/INT pin, GPIO change, or a peripheral interrupt.

**Figure 9-13:** WAKE-UP FROM SLEEP THROUGH INTERRUPT

- Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4
- OSC1
- CLKOUT
- INT pin
- INTF flag (INTCON<1>)
- GIE bit (INTCON<7>)
- INSTRUCTION FLOW
- PC
- Instruction Fetched
- Instruction Executed

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device RESET. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. TO bit is cleared if WDT Wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

**Note:** If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The SLEEP instruction is completely executed.

The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

**Note 1:** XT, HS or LP Oscillator mode assumed.
**Note 2:** TOST = 1024TOSC (drawing not to scale). Approximately 1 µs delay will be there for RC Osc mode. See Section 12 for wake-up from SLEEP delay in INTOSC mode.
**Note 3:** GIE = '1' assumed. In this case after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
**Note 4:** CLKOUT is not available in XT, HS, LP or EC Osc modes, but shown here for timing reference.
9.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

**Note:** The entire data EEPROM and FLASH program memory will be erased when the code protection is turned off. The INTOSC calibration data is also erased. See PIC12F629/675 Programming Specification for more information.

9.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify. Only the Least Significant 7 bits of the ID locations are used.

9.10 In-Circuit Serial Programming

The PIC12F629/675 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for:

- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the GP0 and GP1 pins low, while raising the MCLR (Vpp) pin from VIL to VIHI (see Programming Specification). GP0 becomes the programming data and GP1 becomes the programming clock. Both GP0 and GP1 are Schmitt Trigger inputs in this mode.

After RESET, to place the device into Programming/Verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 9-14.

9.11 In-Circuit Debugger

Since in-circuit debugging requires the loss of clock, data and MCLR pins, MPLAB® ICD 2 development with an 8-pin device is not practical. A special 14-pin PIC12F675-ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

This special ICD device is mounted on the top of the header and its signals are routed to the MPLAB ICD 2 connector. On the bottom of the header is an 8-pin socket that plugs into the user’s target via the 8-pin stand-off connector.

When the ICD pin on the PIC12F675-ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 9-10 shows which features are consumed by the background debugger:

<table>
<thead>
<tr>
<th>TABLE 9-10: DEBUGGER RESOURCES</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O pins</td>
</tr>
<tr>
<td>Stack</td>
</tr>
<tr>
<td>Program Memory</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

For more information, see 8-Pin MPLAB ICD 2 Header Information Sheet (DS51292) available on Microchip’s website (www.microchip.com).
10.0 INSTRUCTION SET SUMMARY

The PIC12F629/675 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC12F629/675 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 10-1, while the various opcode fields are summarized in Table 10-1.

Table 10-2 lists the instructions recognized by the MPASM™ assembler. A complete description of each instruction is also available in the PICmicro™ Mid-Range Reference Manual (DS33023).

For **byte-oriented** instructions, ‘f’ represents a file register designator and ‘d’ represents a destination designator. The file register designator specifies which file register is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If ‘d’ is zero, the result is placed in the W register. If ‘d’ is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, ‘b’ represents a bit field designator, which selects the bit affected by the operation, while ‘f’ represents the address of the file in which the bit is located.

For **literal and control** operations, ‘k’ represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 \( \mu s \). All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

All instruction examples use the format ‘0xhh’ to represent a hexadecimal number, where ‘h’ signifies a hexadecimal digit.

### 10.1 READ-MODIFY-WRITE OPERATIONS

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator ‘d’. A read operation is performed on a register even if the instruction writes to that register.

For example, a **CLRF GPIO** instruction will read GPIO, clear all the data bits, then write the result back to GPIO. This example would have the unintended result that the condition that sets the GPIF flag would be cleared.

### TABLE 10-1: OPCODE FIELD DESCRIPTIONS

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>f</td>
<td>Register file address (0x00 to 0x7F)</td>
</tr>
<tr>
<td>W</td>
<td>Working register (accumulator)</td>
</tr>
<tr>
<td>b</td>
<td>Bit address within an 8-bit file register</td>
</tr>
<tr>
<td>k</td>
<td>Literal field, constant data or label</td>
</tr>
<tr>
<td>x</td>
<td>Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.</td>
</tr>
<tr>
<td>d</td>
<td>Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.</td>
</tr>
<tr>
<td>PC</td>
<td>Program Counter</td>
</tr>
<tr>
<td>TO</td>
<td>Time-out bit</td>
</tr>
<tr>
<td>PD</td>
<td>Power-down bit</td>
</tr>
</tbody>
</table>

### FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS

<table>
<thead>
<tr>
<th>Byte-oriented file register operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 8 7 6 0</td>
</tr>
<tr>
<td>OPCODE   d f (FILE #)</td>
</tr>
<tr>
<td>d = 0 for destination W</td>
</tr>
<tr>
<td>d = 1 for destination f</td>
</tr>
<tr>
<td>f = 7-bit file register address</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit-oriented file register operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 10 9 7 6 0</td>
</tr>
<tr>
<td>OPCODE b (BIT #) f (FILE #)</td>
</tr>
<tr>
<td>b = 3-bit bit address</td>
</tr>
<tr>
<td>f = 7-bit file register address</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Literal and control operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>General</td>
</tr>
<tr>
<td>13 8 7 0</td>
</tr>
<tr>
<td>OPCODE k (literal)</td>
</tr>
<tr>
<td>k = 8-bit immediate value</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CALL and GOTO instructions only</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 11 10 0</td>
</tr>
<tr>
<td>OPCODE k (literal)</td>
</tr>
<tr>
<td>k = 11-bit immediate value</td>
</tr>
</tbody>
</table>
## TABLE 10-2: PIC12F629/675 INSTRUCTION SET

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>14-Bit Opcode</th>
<th>Status</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td>Affected</td>
</tr>
<tr>
<td><strong>BYTE-ORIENTED FILE REGISTER OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDWF f, d</td>
<td>Add W and f</td>
<td>1</td>
<td>00</td>
<td>0111</td>
<td>dfff</td>
</tr>
<tr>
<td>ANDWF f, d</td>
<td>AND W with f</td>
<td>1</td>
<td>00</td>
<td>0101</td>
<td>dfff</td>
</tr>
<tr>
<td>CLRF f</td>
<td>Clear f</td>
<td>1</td>
<td>00</td>
<td>0000</td>
<td>1fff</td>
</tr>
<tr>
<td>CLR f</td>
<td>Clear W</td>
<td>1</td>
<td>00</td>
<td>0001</td>
<td>0xxx</td>
</tr>
<tr>
<td>COMF f, d</td>
<td>Complement f</td>
<td>1</td>
<td>00</td>
<td>1001</td>
<td>dfff</td>
</tr>
<tr>
<td>DEC f, d</td>
<td>Decrement f</td>
<td>1</td>
<td>00</td>
<td>0011</td>
<td>dfff</td>
</tr>
<tr>
<td>DECFSZ f, d</td>
<td>Decrement f, Skip if 0</td>
<td>1(2)</td>
<td>00</td>
<td>1011</td>
<td>dfff</td>
</tr>
<tr>
<td>INC f, d</td>
<td>Increment f</td>
<td>1</td>
<td>00</td>
<td>1010</td>
<td>dfff</td>
</tr>
<tr>
<td>INCFSZ f, d</td>
<td>Increment f, Skip if 0</td>
<td>1(2)</td>
<td>00</td>
<td>1111</td>
<td>dfff</td>
</tr>
<tr>
<td>IORWF f, d</td>
<td>Inclusive OR W with f</td>
<td>1</td>
<td>00</td>
<td>0100</td>
<td>dfff</td>
</tr>
<tr>
<td>MOVF f, d</td>
<td>Move f</td>
<td>1</td>
<td>00</td>
<td>1000</td>
<td>dfff</td>
</tr>
<tr>
<td>MOVWF f, d</td>
<td>Move W to f</td>
<td>1</td>
<td>00</td>
<td>0000</td>
<td>lfff</td>
</tr>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td>-</td>
<td>00</td>
<td>0000</td>
<td>0x00</td>
</tr>
<tr>
<td>RLF f, d</td>
<td>Rotate Left f through Carry</td>
<td>1</td>
<td>00</td>
<td>1101</td>
<td>dfff</td>
</tr>
<tr>
<td>RRF f, d</td>
<td>Rotate Right f through Carry</td>
<td>1</td>
<td>00</td>
<td>1100</td>
<td>dfff</td>
</tr>
<tr>
<td>SUBWF f, d</td>
<td>Subtract W from f</td>
<td>1</td>
<td>00</td>
<td>0010</td>
<td>dfff</td>
</tr>
<tr>
<td>SWAPF f, d</td>
<td>Swap nibbles in f</td>
<td>1</td>
<td>00</td>
<td>1110</td>
<td>dfff</td>
</tr>
<tr>
<td>XORWF f, d</td>
<td>Exclusive OR W with f</td>
<td>1</td>
<td>00</td>
<td>0110</td>
<td>dfff</td>
</tr>
<tr>
<td><strong>BIT-ORIENTED FILE REGISTER OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BCF f, b</td>
<td>Bit Clear f</td>
<td>1</td>
<td>01</td>
<td>00bb</td>
<td>bfff</td>
</tr>
<tr>
<td>BSF f, b</td>
<td>Bit Set f</td>
<td>1</td>
<td>01</td>
<td>01bb</td>
<td>bfff</td>
</tr>
<tr>
<td>BTFSC f, b</td>
<td>Bit Test f, Skip if Clear</td>
<td>1(2)</td>
<td>01</td>
<td>10bb</td>
<td>bfff</td>
</tr>
<tr>
<td>BTFSS f, b</td>
<td>Bit Test f, Skip if Set</td>
<td>1(2)</td>
<td>01</td>
<td>11bb</td>
<td>bfff</td>
</tr>
<tr>
<td><strong>LITERAL AND CONTROL OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDLW k</td>
<td>Add literal and W</td>
<td>1</td>
<td>11</td>
<td>111x</td>
<td>kkkk</td>
</tr>
<tr>
<td>ANDLW k</td>
<td>AND literal with W</td>
<td>1</td>
<td>11</td>
<td>1001</td>
<td>kkkk</td>
</tr>
<tr>
<td>CALL k</td>
<td>Call subroutine</td>
<td>2</td>
<td>10</td>
<td>0kkk</td>
<td>kkkk</td>
</tr>
<tr>
<td>CLRWDT</td>
<td>-</td>
<td>Clear Watchdog Timer</td>
<td>1</td>
<td>00</td>
<td>0000</td>
</tr>
<tr>
<td>GOTO k</td>
<td>Go to address</td>
<td>2</td>
<td>10</td>
<td>1kkk</td>
<td>kkkk</td>
</tr>
<tr>
<td>IORLW k</td>
<td>Inclusive OR literal with W</td>
<td>1</td>
<td>11</td>
<td>1000</td>
<td>kkkk</td>
</tr>
<tr>
<td>MOVVLW k</td>
<td>Move literal to W</td>
<td>1</td>
<td>11</td>
<td>00xx</td>
<td>kkkk</td>
</tr>
<tr>
<td>RETFIE</td>
<td>-</td>
<td>Return from interrupt</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RETLW k</td>
<td>Return with literal in W</td>
<td>2</td>
<td>11</td>
<td>01xx</td>
<td>kkkk</td>
</tr>
<tr>
<td>RETURN</td>
<td>-</td>
<td>Return from Subroutine</td>
<td>2</td>
<td>00</td>
<td>0000</td>
</tr>
<tr>
<td>SLEEP</td>
<td>-</td>
<td>Go into Standby mode</td>
<td>1</td>
<td>00</td>
<td>0000</td>
</tr>
<tr>
<td>SUBLW k</td>
<td>Subtract W from literal</td>
<td>1</td>
<td>11</td>
<td>110x</td>
<td>kkkk</td>
</tr>
<tr>
<td>XORLW k</td>
<td>Exclusive OR literal with W</td>
<td>1</td>
<td>11</td>
<td>1010</td>
<td>kkkk</td>
</tr>
</tbody>
</table>

**Note 1:** When an I/O register is modified as a function of itself (e.g., MOVF GPIO, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

**Note 2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

**Note 3:** If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

**Note:** Additional information on the mid-range instruction set is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).
### 10.2 Instruction Descriptions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
</table>
| **ADDLW** Add Literal and W  
Syntax: \([\text{label}]\) ADDLW \(k\)  
Operands: \(0 \leq k \leq 255\)  
Operation: \((W) + k \rightarrow (W)\)  
Status Affected: C, DC, Z  
Description: The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register. |
| **BCF** Bit Clear f  
Syntax: \([\text{label}]\) BCF \(f, b\)  
Operands: \(0 \leq f \leq 127\)  
\(0 \leq b \leq 7\)  
Operation: \(0 \rightarrow (f <b>)\)  
Status Affected: None  
Description: Bit 'b' in register 'f' is cleared. |
| **ADDWF** Add W and f  
Syntax: \([\text{label}]\) ADDWF \(f, d\)  
Operands: \(0 \leq f \leq 127\)  
\(d \in [0,1]\)  
Operation: \((W) + (f) \rightarrow \text{(destination)}\)  
Status Affected: C, DC, Z  
Description: Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'. |
| **BSF** Bit Set f  
Syntax: \([\text{label}]\) BSF \(f, b\)  
Operands: \(0 \leq f \leq 127\)  
\(0 \leq b \leq 7\)  
Operation: \(1 \rightarrow (f <b>)\)  
Status Affected: None  
Description: Bit 'b' in register 'f' is set. |
| **ANDLW** AND Literal with W  
Syntax: \([\text{label}]\) ANDLW \(k\)  
Operands: \(0 \leq k \leq 255\)  
Operation: \((W) \ . \ AND. (k) \rightarrow (W)\)  
Status Affected: Z  
Description: The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register. |
| **BTFSS** Bit Test f, Skip if Set  
Syntax: \([\text{label}]\) BTFSS \(f, b\)  
Operands: \(0 \leq f \leq 127\)  
\(0 \leq b < 7\)  
Operation: skip if \((f <b>) = 1\)  
Status Affected: None  
Description: If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2T\text{CY} instruction. |
| **ANDWF** AND W with f  
Syntax: \([\text{label}]\) ANDWF \(f, d\)  
Operands: \(0 \leq f \leq 127\)  
\(d \in [0,1]\)  
Operation: \((W) \ . \ AND. (f) \rightarrow \text{(destination)}\)  
Status Affected: Z  
Description: AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'. |
| **BTFSC** Bit Test, Skip if Clear  
Syntax: \([\text{label}]\) BTFSC \(f, b\)  
Operands: \(0 \leq f \leq 127\)  
\(0 \leq b \leq 7\)  
Operation: skip if \((f <b>) = 0\)  
Status Affected: None  
Description: If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2T\text{CY} instruction. |
### CALL Call Subroutine

**Syntax:**

```
[label] CALL k
```

**Operands:**

\(0 \leq k \leq 2047\)

**Operation:**

- \((PC)+1 \rightarrow \text{TOS},\)
- \(k \rightarrow \text{PC}<10:0>,\)
- \((\text{PCLATH}<4:3>) \rightarrow \text{PC}<12:11>\)

**Status Affected:** None

**Description:**

Call Subroutine. First, return address \((PC+1)\) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

### CLRWDT Clear Watchdog Timer

**Syntax:**

```
[label] CLRWDT
```

**Operands:** None

**Operation:**

- \(00h \rightarrow \text{WDT}\)
- \(0 \rightarrow \text{WDT prescaler},\)
- \(1 \rightarrow \text{T0}\)
- \(1 \rightarrow \text{PD}\)

**Status Affected:** \(\text{T0}, \text{PD}\)

**Description:**

CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits \(\text{T0}\) and \(\text{PD}\) are set.

### CLRF Clear f

**Syntax:**

```
[label] CLRF f
```

**Operands:**

\(0 \leq f \leq 127\)

**Operation:**

- \(00h \rightarrow (f)\)
- \(1 \rightarrow Z\)

**Status Affected:** Z

**Description:**

The contents of register \(f\) are cleared and the Z bit is set.

### COMF Complement f

**Syntax:**

```
[label] COMF f,d
```

**Operands:**

- \(0 \leq f \leq 127\)
- \(d \in [0,1]\)

**Operation:**

- \((f) \rightarrow (\text{destination})\)

**Status Affected:** Z

**Description:**

The contents of register \(f\) are complemented. If \(d\) is 0, the result is stored in W. If \(d\) is 1, the result is stored back in register \(f\).

### CLRW Clear W

**Syntax:**

```
[label] CLRW
```

**Operands:** None

**Operation:**

- \(00h \rightarrow (W)\)
- \(1 \rightarrow Z\)

**Status Affected:** Z

**Description:**

W register is cleared. Zero bit \(Z\) is set.

### DECF Decrement f

**Syntax:**

```
[label] DECF f,d
```

**Operands:**

- \(0 \leq f \leq 127\)
- \(d \in [0,1]\)

**Operation:**

- \((f) - 1 \rightarrow (\text{destination})\)

**Status Affected:** Z

**Description:**

Decrement register \(f\). If \(d\) is 0, the result is stored in the W register. If \(d\) is 1, the result is stored back in register \(f\).
### DECFSZ  Decrement f, Skip if 0

**Syntax:**  
\[
[\text{label}] \quad \text{DECFSZ} \quad f,d
\]

**Operands:**  
\[
0 \leq f \leq 127  
\quad d \in [0,1]
\]

**Operation:**  
\[
(f) - 1 \to (\text{destination}); \quad \text{skip if result} = 0
\]

**Status Affected:** None

**Description:**  
The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead, making it a 2Tcy instruction.

### INCFSZ Increment f, Skip if 0

**Syntax:**  
\[
[\text{label}] \quad \text{INCFSZ} \quad f,d
\]

**Operands:**  
\[
0 \leq f \leq 127  
\quad d \in [0,1]
\]

**Operation:**  
\[
(f) + 1 \to (\text{destination}), \quad \text{skip if result} = 0
\]

**Status Affected:** None

**Description:**  
The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead, making it a 2Tcy instruction.

### GOTO Unconditional Branch

**Syntax:**  
\[
[\text{label}] \quad \text{GOTO} \quad k
\]

**Operands:**  
\[
0 \leq k \leq 2047
\]

**Operation:**  
\[
k \to \text{PC}<10:0>  
\quad \text{PCLATH}<4:3> \to \text{PC}<12:11>
\]

**Status Affected:** None

**Description:**  
GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

### IORLW Inclusive OR Literal with W

**Syntax:**  
\[
[\text{label}] \quad \text{IORLW} \quad k
\]

**Operands:**  
\[
0 \leq k \leq 255
\]

**Operation:**  
\[
(W) .OR. k \to (W)
\]

**Status Affected:** Z

**Description:**  
The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

### INCF Increment f

**Syntax:**  
\[
[\text{label}] \quad \text{INCF} \quad f,d
\]

**Operands:**  
\[
0 \leq f \leq 127  
\quad d \in [0,1]
\]

**Operation:**  
\[
(f) + 1 \to (\text{destination})
\]

**Status Affected:** Z

**Description:**  
The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

### IORWF Inclusive OR W with f

**Syntax:**  
\[
[\text{label}] \quad \text{IORWF} \quad f,d
\]

**Operands:**  
\[
0 \leq f \leq 127  
\quad d \in [0,1]
\]

**Operation:**  
\[
(W) .OR. (f) \to (\text{destination})
\]

**Status Affected:** Z

**Description:**  
Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.
<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
</table>
| **MOVF** | Move f  
*Syntax:* 
\[
\text{[ label ] MOVF } f,d 
\]  
*Operands:* 
\[ 0 \leq f \leq 127 \]  
\[ d \in [0,1] \]  
*Operation:* 
\[(f) \rightarrow (\text{destination})\]  
*Status Affected:* 
\[ Z \]  
*Description:* The contents of register f are moved to a destination dependant upon the status of d. If \(d = 0\), destination is W register. If \(d = 1\), the destination is file register f itself. \(d = 1\) is useful to test a file register, since status flag Z is affected. |
| **MOVLW** | Move Literal to W  
*Syntax:* 
\[
\text{[ label ] MOVLW } k 
\]  
*Operands:* 
\[ 0 \leq k \leq 255 \]  
*Operation:* 
\[ k \rightarrow (W) \]  
*Status Affected:* None  
*Description:* The eight-bit literal 'k' is loaded into W register. The don't cares will assemble as 0's. |
| **MOVWF** | Move W to f  
*Syntax:* 
\[
\text{[ label ] MOVWF } f 
\]  
*Operands:* 
\[ 0 \leq f \leq 127 \]  
*Operation:* 
\[ (W) \rightarrow (f) \]  
*Status Affected:* None  
*Description:* Move data from W register to register 'f'. |
| **NOP** | No Operation  
*Syntax:* 
\[
\text{[ label ] NOP} 
\]  
*Operands:* None  
*Operation:* No operation  
*Status Affected:* None  
*Description:* No operation. |
| **RETFIE** | Return from Interrupt  
*Syntax:* 
\[
\text{[ label ] RETFIE} 
\]  
*Operands:* None  
*Operation:* \[ \text{TOS} \rightarrow \text{PC}, \text{1} \rightarrow \text{GIE} \]  
*Status Affected:* None  
*Description:* |
| **RETLW** | Return with Literal in W  
*Syntax:* 
\[
\text{[ label ] RETLW } k 
\]  
*Operands:* 
\[ 0 \leq k \leq 255 \]  
*Operation:* \[ k \rightarrow (W); \text{TOS} \rightarrow \text{PC} \]  
*Status Affected:* None  
*Description:* The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction. |
**RLF**

**Rotate Left f through Carry**

**Syntax:**  \([ \text{label} ]\) RLF \(f,d\)

**Operands:**  \(0 \leq f \leq 127\)
\(d \in [0,1]\)

**Operation:**  See description below

**Status Affected:**  \(C\)

**Description:**  The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.

**RETURN**

**Return from Subroutine**

**Syntax:**  \([ \text{label} ]\) RETURN

**Operands:**  None

**Operation:**  TOS \(\rightarrow\) PC

**Status Affected:**  None

**Description:**  Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

**SLEEP**

**Syntax:**  \([ \text{label} ]\) SLEEP

**Operands:**  None

**Operation:**  
\(00h \rightarrow WDT,\)
\(0 \rightarrow WDT\) prescaler,
\(1 \rightarrow TO,\)
\(0 \rightarrow PD\)

**Status Affected:**  \(TO, PD\)

**Description:**  The power-down STATUS bit, \(PD\) is cleared. Time-out STATUS bit, \(TO\) is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped.

**RRF**

**Rotate Right f through Carry**

**Syntax:**  \([ \text{label} ]\) RRF \(f,d\)

**Operands:**  \(0 \leq f \leq 127\)
\(d \in [0,1]\)

**Operation:**  See description below

**Status Affected:**  \(C\)

**Description:**  The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

**SUBLW**

**Subtract W from Literal**

**Syntax:**  \([ \text{label} ]\) SUBLW \(k\)

**Operands:**  \(0 \leq k \leq 255\)

**Operation:**  \(k - (W) \rightarrow (W)\)

**Status Affected:**  \(C, DC, Z\)

**Description:**  The W register is subtracted (2's complement method) from the eight-bit literal \(k\). The result is placed in the W register.

**SUBLW**

**Subtract W from f**

**Syntax:**  \([ \text{label} ]\) SUBWF \(f,d\)

**Operands:**  \(0 \leq f \leq 127\)
\(d \in [0,1]\)

**Operation:**  \((f) - (W) \rightarrow \text{destination}\)

**Status Affected:**  \(C, DC, Z\)

**Description:**  Subtract (2’s complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
### SWAPF

**Swap Nibbles in f**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ] SWAPF f,d</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>( 0 \leq f \leq 127 )  ( d \in [0,1] )</td>
</tr>
<tr>
<td>Operation:</td>
<td>((f&lt;3:0&gt;) \rightarrow (destination&lt;7:4&gt;),)  ((f&lt;7:4&gt;) \rightarrow (destination&lt;3:0&gt;))</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Description:</td>
<td>The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in register 'f'.</td>
</tr>
</tbody>
</table>

### XORWF

**Exclusive OR W with f**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ] XORWF f,d</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>( 0 \leq f \leq 127 )  ( d \in [0,1] )</td>
</tr>
<tr>
<td>Operation:</td>
<td>((W) \text{ XOR } (f) \rightarrow (destination))</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.</td>
</tr>
</tbody>
</table>

### XORLW

**Exclusive OR Literal with W**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ] XORLW k</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>( 0 \leq k \leq 255 )</td>
</tr>
<tr>
<td>Operation:</td>
<td>((W) \text{ XOR } k \rightarrow (W))</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.</td>
</tr>
</tbody>
</table>
11.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB C30 C Compiler
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
  - MPLAB dsPIC30 Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM.net™ Demonstration Board
  - PICDEM 2 Plus Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - PICDEM 18R Demonstration Board
  - PICDEM LIN Demonstration Board
  - PICDEM USB Demonstration Board
- Evaluation Kits
  - KeELOQ®
  - PICDEM MSC
  - microID®
  - CAN
  - PowerSmart®
  - Analog

11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High level source code debugging
- Mouse over variable inspection
- Extensive on-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files (assembly or C)
  - absolute listing file (mixed assembly and C)
  - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

11.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contains source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process
11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI C compilers for Microchip’s PIC17CXXX and PIC18CXXX family of microcontrollers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

11.4 MPLINK Object Linker/
MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian manages the creation and modification of library files of pre-compiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:
- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

11.5 MPLAB C30 C Compiler

The MPLAB C30 C compiler is a full-featured, ANSI compliant, optimizing compiler that translates standard ANSI C programs into dsPIC30F assembly language source. The compiler also supports many command-line options and language extensions to take full advantage of the dsPIC30F device hardware capabilities, and afford fine control of the compiler code generator.

MPLAB C30 is distributed with a complete ANSI C standard library. All library functions have been validated and conform to the ANSI C library standard. The library includes functions for string manipulation, dynamic memory allocation, data conversion, time-keeping, and math functions (trigonometric, exponential and hyperbolic). The compiler provides symbolic information for high level source debugging with the MPLAB IDE.

11.6 MPLAB ASM30 Assembler, Linker, and Librarian

MPLAB ASM30 assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 compiler uses the assembler to produce it’s object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:
- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

11.7 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any pin. The execution can be performed in Single-Step, Execute Until Break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and MPLAB C18 C Compilers, as well as the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

11.8 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator allows code development in a PC hosted environment by simulating the dsPIC30F series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any of the pins.

The MPLAB SIM30 simulator fully supports symbolic debugging using the MPLAB C30 C Compiler and MPLAB ASM30 assembler. The simulator runs in either a Command Line mode for automated tasks, or from MPLAB IDE. This high speed simulator is designed to debug, analyze and optimize time intensive DSP routines.
11.9 MPLAB ICE 2000
High Performance Universal
In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.10 MPLAB ICE 4000
High Performance Universal
In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory, and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.11 MPLAB ICD 2 In-Circuit Debugger

Microchip’s In-Circuit Debugger, MPLAB ICD 2, is a powerful, low cost, run-time development tool, connecting to the host PC via an RS-232 or high speed USB interface. This tool is based on the FLASH PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip’s In-Circuit Serial Programming™ (ICSP™) protocol, offers cost effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

11.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, and program PICmicro devices without a PC connection. It can also set code protection in this mode.

11.13 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PICmicro devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.
11.14 PICDEM 1 PICmicro Demonstration Board

The PICDEM 1 demonstration board demonstrates the capabilities of the PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The sample microcontrollers provided with the PICDEM 1 demonstration board can be programmed with a PRO MATE II device programmer, or a PICSTART Plus development programmer. The PICDEM 1 demonstration board can be connected to the MPLAB ICE in-circuit emulator for testing. A prototype area extends the circuitry for additional application components. Features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs.

11.15 PICDEM.net Internet/Ethernet Demonstration Board

The PICDEM.net demonstration board is an Internet/Ethernet demonstration board using the PIC18F452 microcontroller and TCP/IP firmware. The board supports any 40-pin DIP device that conforms to the standard pinout used by the PIC16F877 or PIC18C452. This kit features a user friendly TCP/IP stack, web server with HTML, a 24L256 Serial EEPROM for Xmodem download to web pages into Serial EEPROM, ICSP/MPLAB ICD 2 interface connector, an Ethernet interface, RS-232 interface, and a 16 x 2 LCD display. Also included is the book and CD-ROM “TCP/IP Lean, Web Servers for Embedded Systems,” by Jeremy Bentham

11.16 PICDEM 2 Plus Demonstration Board

The PICDEM 2 Plus demonstration board supports many 18-, 28-, and 40-pin microcontrollers, including PIC16F87X and PIC18FXX2 devices. All the necessary hardware and software is included to run the demonstration programs. The sample microcontrollers provided with the PICDEM 2 demonstration board can be programmed with a PRO MATE II device programmer, PICSTART Plus development programmer, or MPLAB ICD 2 with a Universal Programmer Adapter. The MPLAB ICD 2 and MPLAB ICE in-circuit emulators may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area extends the circuitry for additional application components. Some of the features include an RS-232 interface, a 2 x 16 LCD display, a piezo speaker, an on-board temperature sensor, four LEDs, and sample PIC18F452 and PIC16F877 FLASH microcontrollers.

11.17 PICDEM 3 PIC16C92X Demonstration Board

The PICDEM 3 demonstration board supports the PIC16C923 and PIC16C924 in the PLCC package. All the necessary hardware and software is included to run the demonstration programs.

11.18 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. A programmed sample is included. The PRO MATE II device programmer, or the PICSTART Plus development programmer, can be used to reprogram the device for user tailored application development. The PICDEM 17 demonstration board supports program download and execution from external on-board FLASH memory. A generous prototype area is available for user hardware expansion.
11.19 **PICDEM 18R PIC18C601/801 Demonstration Board**

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/De-multiplexed and 16-bit Memory modes. The board includes 2 Mb external FLASH memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

11.20 **PICDEM LIN PIC16C43X Demonstration Board**

The powerful LIN hardware and software kit includes a series of boards and three PICmicro microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIIN communication and feature on-board LIIN transceivers. A PIC16F874 FLASH microcontroller serves as the master. All three microcontrollers are programmed with firmware to provide LIN bus communication.

11.21 **PICkit™ 1 FLASH Starter Kit**

A complete "development system in a box", the PICkit FLASH Starter Kit includes a convenient multi-section board for programming, evaluation, and development of 8/14-pin FLASH PIC® microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the user's guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB® IDE (Integrated Development Environment) software, software and hardware "Tips 'n Tricks for 8-pin FLASH PIC® Microcontrollers" Handbook and a USB Interface Cable. Supports all current 8/14-pin FLASH PIC microcontrollers, as well as many future planned devices.

11.22 **PICDEM USB PIC16C7X5 Demonstration Board**

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

11.23 **Evaluation and Programming Tools**

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELoo evaluation and programming tools for Microchip’s HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/calibration kits
- IrDA® development kit
- microID development and rfLabTM development software
- SEEVAL® designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high power IR driver, delta sigma ADC, and flow rate sensor

Check the Microchip web page and the latest Product Line Card for the complete list of demonstration and evaluation kits.
12.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient temperature under bias</td>
<td>-40 to +125°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Voltage on VDD with respect to VSS</td>
<td>-0.3 to +6.5V</td>
</tr>
<tr>
<td>Voltage on MCLR with respect to Vss</td>
<td>-0.3 to +13.5V</td>
</tr>
<tr>
<td>Voltage on all other pins with respect to Vss</td>
<td>-0.3V to (VDD + 0.3V)</td>
</tr>
<tr>
<td>Total power dissipation</td>
<td>800 mW</td>
</tr>
<tr>
<td>Maximum current out of VSS pin</td>
<td>300 mA</td>
</tr>
<tr>
<td>Maximum current into VDD pin</td>
<td>250 mA</td>
</tr>
<tr>
<td>Input clamp current, I&lt;sub&gt;IK&lt;/sub&gt; (Vi &lt; 0 or Vi &gt; VDD)</td>
<td>± 20 mA</td>
</tr>
<tr>
<td>Output clamp current, I&lt;sub&gt;OK&lt;/sub&gt; (Vo &lt; 0 or Vo &gt; VDD)</td>
<td>± 20 mA</td>
</tr>
<tr>
<td>Maximum output current sunk by any I/O pin</td>
<td>25 mA</td>
</tr>
<tr>
<td>Maximum output current sourced by any I/O pin</td>
<td>25 mA</td>
</tr>
<tr>
<td>Maximum current sunk by all GPIO</td>
<td>125 mA</td>
</tr>
<tr>
<td>Maximum current sourced all GPIO</td>
<td>125 mA</td>
</tr>
</tbody>
</table>

Note 1: Power dissipation is calculated as follows: 
\[ P_{DIS} = V_{DD} \times (I_{DD} - \sum I_{OH}) + \sum ((V_{DD} - V_{OH}) \times I_{OH}) + \sum (V_{OL} \times I_{OL}) \].

† NOTICE: Stresses above those listed under ‘Absolute Maximum Ratings’ may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latchup. Thus, a series resistor of 50-100 Ω should be used when applying a “low” level to the MCLR pin, rather than pulling this pin directly to Vss.
FIGURE 12-1: PIC12F629/675 WITH A/D DISABLED VOLTAGE-FREQUENCY GRAPH, 
-40°C ≤ TA ≤ +125°C

![Graph showing voltage vs. frequency for PIC12F629/675 with A/D disabled.]

**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 12-2: PIC12F675 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH, 
-40°C ≤ TA ≤ +125°C

![Graph showing voltage vs. frequency for PIC12F675 with A/D enabled.]

**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.
FIGURE 12-3: PIC12F675 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH, 
0°C ≤ TA ≤ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
12.1 DC Characteristics: PIC12F629/675-I (Industrial), PIC12F629/675-E (Extended)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D001</td>
<td>VDD</td>
<td>Supply Voltage</td>
<td>2.0</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>Fosc ≤ 4 MHz:</td>
</tr>
<tr>
<td>D001A</td>
<td></td>
<td></td>
<td>2.2</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>PIC12F629/675 with A/D off</td>
</tr>
<tr>
<td>D001B</td>
<td></td>
<td></td>
<td>2.5</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>PIC12F675 with A/D on, 0°C to +125°C</td>
</tr>
<tr>
<td>D001C</td>
<td></td>
<td></td>
<td>3.0</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>PIC12F675 with A/D on, -40°C to +125°C</td>
</tr>
<tr>
<td>D001D</td>
<td></td>
<td></td>
<td>4.5</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>4 MHz &lt; Fosc ≤ 10 MHz</td>
</tr>
<tr>
<td>D002</td>
<td>VDR</td>
<td>RAM Data Retention Voltage(1)</td>
<td>1.5*</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>Device in SLEEP mode</td>
</tr>
<tr>
<td>D003</td>
<td>VPOR</td>
<td>VDD Start Voltage to ensure internal Power-on Reset signal</td>
<td>—</td>
<td>Vss</td>
<td>—</td>
<td>V</td>
<td>See section on Power-on Reset for details</td>
</tr>
<tr>
<td>D004</td>
<td>SVDD</td>
<td>VDD Rise Rate to ensure internal Power-on Reset signal</td>
<td>0.05*</td>
<td>—</td>
<td>—</td>
<td>V/ms</td>
<td>See section on Power-on Reset for details</td>
</tr>
<tr>
<td>D005</td>
<td>VBDD</td>
<td></td>
<td>—</td>
<td>2.1</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
### 12.2 DC Characteristics: PIC12F629/675-I (Industrial)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VDD</td>
</tr>
<tr>
<td>D010</td>
<td>Supply Current (I\text{DD})</td>
<td>—</td>
<td>9</td>
<td>16</td>
<td>µA</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>18</td>
<td>28</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>35</td>
<td>54</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D011</td>
<td></td>
<td>—</td>
<td>110</td>
<td>150</td>
<td>µA</td>
<td>2.0</td>
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<tr>
<td></td>
<td></td>
<td>—</td>
<td>190</td>
<td>280</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>330</td>
<td>450</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D012</td>
<td></td>
<td>—</td>
<td>220</td>
<td>280</td>
<td>µA</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>370</td>
<td>650</td>
<td>µA</td>
<td>3.0</td>
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<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.6</td>
<td>1.4</td>
<td>mA</td>
<td>5.0</td>
</tr>
<tr>
<td>D013</td>
<td></td>
<td>—</td>
<td>70</td>
<td>110</td>
<td>µA</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>140</td>
<td>250</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>260</td>
<td>390</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D014</td>
<td></td>
<td>—</td>
<td>180</td>
<td>250</td>
<td>µA</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>320</td>
<td>470</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>580</td>
<td>850</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D015</td>
<td></td>
<td>—</td>
<td>340</td>
<td>450</td>
<td>µA</td>
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<td></td>
<td></td>
<td>—</td>
<td>500</td>
<td>700</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.8</td>
<td>1.1</td>
<td>mA</td>
<td>5.0</td>
</tr>
<tr>
<td>D016</td>
<td></td>
<td>—</td>
<td>180</td>
<td>250</td>
<td>µA</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
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<td>—</td>
<td>320</td>
<td>450</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>580</td>
<td>800</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D017</td>
<td></td>
<td>—</td>
<td>2.1</td>
<td>2.95</td>
<td>mA</td>
<td>4.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>2.4</td>
<td>3.0</td>
<td>mA</td>
<td>5.0</td>
</tr>
</tbody>
</table>

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The test conditions for all I\text{DD} measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to V\text{DD}; MCLR = V\text{DD}; WDT disabled.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
### DC Characteristics: PIC12F629/675-I (Industrial)

**Standard Operating Conditions (unless otherwise stated)**

Operating temperature: 
\[-40°C ≤ TA ≤ +85°C\] for industrial

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VDD</td>
</tr>
<tr>
<td>D020</td>
<td>Power-down Base Current</td>
<td>—</td>
<td>0.99</td>
<td>700</td>
<td>nA</td>
<td>2.0 WDT, BOD, Comparators, VREF, and T1OSC disabled</td>
</tr>
<tr>
<td></td>
<td>(IPD)</td>
<td>—</td>
<td>1.2</td>
<td>770</td>
<td>nA</td>
<td>3.0</td>
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<tr>
<td></td>
<td></td>
<td>—</td>
<td>2.9</td>
<td>995</td>
<td>nA</td>
<td>5.0</td>
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<tr>
<td>D021</td>
<td>—</td>
<td>—</td>
<td>0.3</td>
<td>1.5</td>
<td>µA</td>
<td>2.0 WDT Current(1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>1.8</td>
<td>3.5</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>8.4</td>
<td>17</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D022</td>
<td>—</td>
<td>—</td>
<td>58</td>
<td>70</td>
<td>µA</td>
<td>3.0 BOD Current(1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>109</td>
<td>130</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D023</td>
<td>—</td>
<td>—</td>
<td>3.3</td>
<td>6.5</td>
<td>µA</td>
<td>2.0 Comparator Current(1)</td>
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<td></td>
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<td>—</td>
<td>6.1</td>
<td>8.5</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>11.5</td>
<td>16</td>
<td>µA</td>
<td>5.0</td>
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<tr>
<td>D024</td>
<td>—</td>
<td>—</td>
<td>58</td>
<td>70</td>
<td>µA</td>
<td>2.0 CVREF Current(1)</td>
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<tr>
<td></td>
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<td>—</td>
<td>85</td>
<td>100</td>
<td>µA</td>
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<tr>
<td></td>
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<td>—</td>
<td>138</td>
<td>160</td>
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<tr>
<td>D025</td>
<td>—</td>
<td>—</td>
<td>4.0</td>
<td>6.5</td>
<td>µA</td>
<td>2.0 T1 Osc Current(1)</td>
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<tr>
<td></td>
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<td>4.6</td>
<td>7.0</td>
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<td>D026</td>
<td>—</td>
<td>—</td>
<td>1.2</td>
<td>775</td>
<td>nA</td>
<td>3.0 A/D Current(1)</td>
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<td>0.0022</td>
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† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral ∆ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**Note 2:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD.
### 12.4 DC Characteristics: PIC12F629/675-E (Extended)

**Standard Operating Conditions (unless otherwise stated)**

Operating temperature $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for extended

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
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<tbody>
<tr>
<td>D010E</td>
<td>Supply Current (IDD)</td>
<td>9</td>
<td>16</td>
<td>µA</td>
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<td>FOSC = 32 kHz</td>
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<tr>
<td></td>
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<td>18</td>
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<td>µA</td>
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<td></td>
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<td>54</td>
<td>µA</td>
<td>5.0</td>
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<td>D011E</td>
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<td>110</td>
<td>150</td>
<td>µA</td>
<td>2.0</td>
<td>FOSC = 1 MHz</td>
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<tr>
<td></td>
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<td>190</td>
<td>280</td>
<td>µA</td>
<td>3.0</td>
<td>XT Oscillator Mode</td>
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<td></td>
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<td>450</td>
<td>µA</td>
<td>5.0</td>
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<td>D012E</td>
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<td>220</td>
<td>280</td>
<td>µA</td>
<td>2.0</td>
<td>FOSC = 4 MHz</td>
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<td>370</td>
<td>650</td>
<td>µA</td>
<td>3.0</td>
<td>XT Oscillator Mode</td>
</tr>
<tr>
<td></td>
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<td>0.6</td>
<td>1.4</td>
<td>mA</td>
<td>5.0</td>
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</tr>
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<td>D013E</td>
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<td>µA</td>
<td>2.0</td>
<td>FOSC = 1 MHz</td>
</tr>
<tr>
<td></td>
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<td>250</td>
<td>µA</td>
<td>3.0</td>
<td>EC Oscillator Mode</td>
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<td>260</td>
<td>390</td>
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<td>D014E</td>
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<td>µA</td>
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<td>FOSC = 4 MHz</td>
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<td>850</td>
<td>µA</td>
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<td>mA</td>
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<td>FOSC = 4 MHz</td>
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<td>µA</td>
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<tr>
<td>D017E</td>
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<td>2.95</td>
<td>mA</td>
<td>4.5</td>
<td>FOSC = 20 MHz</td>
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<tr>
<td></td>
<td></td>
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<td>3.0</td>
<td>mA</td>
<td>5.0</td>
<td>HS Oscillator Mode</td>
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</table>

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
### DC Characteristics: PIC12F629/675-E (Extended)

#### Standard Operating Conditions (unless otherwise stated)
Operating temperature $-40^\circ C \leq T_A \leq +125^\circ C$ for extended

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
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<tr>
<td>D021E</td>
<td>Power-down Base Current (I_PD)</td>
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<td>µA</td>
<td>WDT Current(1)</td>
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<tr>
<td></td>
<td></td>
<td>—</td>
<td>1.8</td>
<td>9.0</td>
<td>µA</td>
<td>WDT Current(1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>8.4</td>
<td>20</td>
<td>µA</td>
<td>WDT Current(1)</td>
</tr>
<tr>
<td>D022E</td>
<td></td>
<td>—</td>
<td>58</td>
<td>70</td>
<td>µA</td>
<td>BOD Current(1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>109</td>
<td>130</td>
<td>µA</td>
<td>BOD Current(1)</td>
</tr>
<tr>
<td>D023E</td>
<td></td>
<td>—</td>
<td>3.3</td>
<td>10</td>
<td>µA</td>
<td>Comparator Current(1)</td>
</tr>
<tr>
<td></td>
<td></td>
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<td>6.1</td>
<td>13</td>
<td>µA</td>
<td>Comparator Current(1)</td>
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<td></td>
<td>—</td>
<td>11.5</td>
<td>24</td>
<td>µA</td>
<td>Comparator Current(1)</td>
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<td>D024E</td>
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<td>58</td>
<td>70</td>
<td>µA</td>
<td>CVREF Current(1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>85</td>
<td>100</td>
<td>µA</td>
<td>CVREF Current(1)</td>
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<tr>
<td></td>
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<td>—</td>
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<td>165</td>
<td>µA</td>
<td>CVREF Current(1)</td>
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<td>D025E</td>
<td></td>
<td>—</td>
<td>4.0</td>
<td>10</td>
<td>µA</td>
<td>T1 Osc Current(1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>4.6</td>
<td>12</td>
<td>µA</td>
<td>T1 Osc Current(1)</td>
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<td></td>
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<td>—</td>
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<td>20</td>
<td>µA</td>
<td>T1 Osc Current(1)</td>
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<td>D026E</td>
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<td>0.0012</td>
<td>6.0</td>
<td>µA</td>
<td>A/D Current(1)</td>
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<td></td>
<td>—</td>
<td>0.0022</td>
<td>8.5</td>
<td>µA</td>
<td>A/D Current(1)</td>
</tr>
</tbody>
</table>

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base I_DD or I_PD and the additional current consumed when this peripheral is enabled. The peripheral $\Delta$ current can be determined by subtracting the base I_DD or I_PD current from this limit. Max values should be used when calculating total current consumption.

**2:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD.
12.6 DC Characteristics: PIC12F629/675-I (Industrial), PIC12F629/675-E (Extended)

<table>
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<th>DC CHARACTERISTICS</th>
<th>Standard Operating Conditions (unless otherwise stated)</th>
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<tr>
<td></td>
<td>Operating temperature -40°C ≤ TA ≤ +85°C for industrial</td>
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<tr>
<td></td>
<td>-40°C ≤ TA ≤ +125°C for extended</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VIL</td>
<td>Input Low Voltage</td>
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<td></td>
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<td></td>
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<tr>
<td>D030</td>
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<td>I/O ports with TTL buffer</td>
<td>VSS</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>4.5V ≤ VDD ≤ 5.5V</td>
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<tr>
<td>D030A</td>
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<td>VSS</td>
<td>—</td>
<td>0.15VDD</td>
<td>V</td>
<td>Otherwise</td>
</tr>
<tr>
<td>D031</td>
<td></td>
<td>with Schmitt Trigger buffer</td>
<td>VSS</td>
<td>—</td>
<td>0.2VDD</td>
<td>V</td>
<td>Entire range</td>
</tr>
<tr>
<td>D032</td>
<td></td>
<td>MCLR, OSC1 (RC mode)</td>
<td>VSS</td>
<td>—</td>
<td>0.2VDD</td>
<td>V</td>
<td></td>
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<tr>
<td>D033</td>
<td></td>
<td>OSC1 (XT and LP modes)</td>
<td>VSS</td>
<td>—</td>
<td>0.3</td>
<td>V</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>D033A</td>
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<td></td>
<td>VSS</td>
<td>—</td>
<td>0.3VDD</td>
<td>V</td>
<td>(Note 1)</td>
</tr>
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<td></td>
<td>VIH</td>
<td>Input High Voltage</td>
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<td>D040</td>
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<td>I/O ports with TTL buffer</td>
<td>2.0</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td>4.5V ≤ VDD ≤ 5.5V</td>
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<tr>
<td>D040A</td>
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<td>(0.25VDD+0.8)</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td>otherwise</td>
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<tr>
<td>D041</td>
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<td>with Schmitt Trigger buffer</td>
<td>0.8VDD</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td>entire range</td>
</tr>
<tr>
<td>D042</td>
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<td>MCLR</td>
<td>0.8VDD</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
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<td>OSC1 (XT and LP modes)</td>
<td>1.6</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td>(Note 1)</td>
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<td>OSC1 (HS mode)</td>
<td>0.7VDD</td>
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<td>VDD</td>
<td>V</td>
<td>(Note 1)</td>
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<td>OSC1 (RC mode)</td>
<td>0.9VDD</td>
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<td>VDD</td>
<td>V</td>
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<tr>
<td>D070</td>
<td>IPUR</td>
<td>GPIO Weak Pull-up Current</td>
<td>50*</td>
<td>250</td>
<td>400*</td>
<td>μA</td>
<td>VDD = 5.0V, VIN = VSS</td>
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<tr>
<td>D060</td>
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<td>Input Leakage Current(3)</td>
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<td>D060A</td>
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<td>I/O ports</td>
<td>—</td>
<td>±0.1</td>
<td>±1</td>
<td>μA</td>
<td>VSS ≤ VIN ≤ VDD, Pin at hi-impedance</td>
</tr>
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<td>D060B</td>
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<td>Analog inputs</td>
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<td>±1</td>
<td>μA</td>
<td>VSS ≤ VIN ≤ VDD</td>
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<td>VREF</td>
<td>—</td>
<td>±0.1</td>
<td>±1</td>
<td>μA</td>
<td>VSS ≤ VIN ≤ VDD</td>
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<td>MCLR(2)</td>
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<td>±5</td>
<td>μA</td>
<td>VSS ≤ VIN ≤ VDD</td>
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<td>I/O ports</td>
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<td>—</td>
<td>0.6</td>
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<td>Output High Voltage</td>
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<td>I/O ports</td>
<td>VDD - 0.7</td>
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<td>—</td>
<td>V</td>
<td>IOH = -3.0 mA, VDD = 4.5V (Ind.)</td>
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<td>—</td>
<td>V</td>
<td>IOH = -1.3 mA, VDD = 4.5V (Ind.)</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

**Note 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**Note 3:** Negative current is defined as current sourced by the pin.
12.7 DC Characteristics: PIC12F629/675-I (Industrial), PIC12F629/675-E (Extended) (Cont.)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Standard Operating Conditions (unless otherwise stated)</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td>Operating temperature: -40°C ≤ TA ≤ +85°C for industrial</td>
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<td>-40°C ≤ TA ≤ +125°C for extended</td>
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<td>D100</td>
<td>C</td>
<td>Osc2 Capacitive Loading Specs on Output Pins</td>
<td>Min</td>
<td>Typ†</td>
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<td>C</td>
<td>IO All I/O pins</td>
<td>Min</td>
<td>Typ†</td>
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<td>Byte Endurance</td>
<td>10K</td>
<td>100K</td>
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<tr>
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<td>V</td>
<td>DRW VDD for Read/Write</td>
<td>VMIN</td>
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<td>DEW Erase/Write cycle time</td>
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<td>RETD Characteristic Retention</td>
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<td>10M</td>
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<td>10K</td>
</tr>
<tr>
<td>D131</td>
<td>V</td>
<td>PR VDD for Read</td>
<td>VMIN</td>
<td>—</td>
</tr>
<tr>
<td>D132</td>
<td>V</td>
<td>PEW VDD for Erase/Write</td>
<td>4.5</td>
<td>—</td>
</tr>
<tr>
<td>D133</td>
<td>T</td>
<td>PEW Erase/Write cycle time</td>
<td>—</td>
<td>2</td>
</tr>
<tr>
<td>D134</td>
<td>T</td>
<td>RETD Characteristic Retention</td>
<td>40</td>
<td>—</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: See Section 8.5.1 for additional information.
12.8 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created with one of the following formats:

1. $T_{ppS2ppS}$
2. $T_{ppS}$

<table>
<thead>
<tr>
<th>$T$</th>
<th>$F$</th>
<th>Frequency</th>
<th>$T$</th>
<th>Time</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>$pp$</th>
<th>$pp$</th>
<th>$pp$</th>
<th>$pp$</th>
<th>$pp$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$cc$</td>
<td>CCP1</td>
<td>$osc$</td>
<td>OSC1</td>
<td>$rd$</td>
</tr>
<tr>
<td>$ck$</td>
<td>CLKOUT</td>
<td>$rw$</td>
<td>RD or WR</td>
<td>$sc$</td>
</tr>
<tr>
<td>$cs$</td>
<td>CS</td>
<td>$ss$</td>
<td>SS</td>
<td>$di$</td>
</tr>
<tr>
<td>$do$</td>
<td>SDO</td>
<td>$tt0$</td>
<td>T0CKI</td>
<td>$dt$</td>
</tr>
<tr>
<td>$dl$</td>
<td>I/O port</td>
<td>$t1$</td>
<td>T1CKI</td>
<td>$io$</td>
</tr>
<tr>
<td>$mc$</td>
<td>MCLR</td>
<td>$wr$</td>
<td>WR</td>
<td>$mt$</td>
</tr>
</tbody>
</table>

Lowercase letters (pp) and their meanings:

Uppercase letters and their meanings:

<table>
<thead>
<tr>
<th>$S$</th>
<th>$S$</th>
<th>$S$</th>
<th>$S$</th>
<th>$S$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F$</td>
<td>Fall</td>
<td>$P$</td>
<td>Period</td>
<td>$R$</td>
</tr>
<tr>
<td>$H$</td>
<td>High</td>
<td>$V$</td>
<td>Valid</td>
<td>$L$</td>
</tr>
<tr>
<td>$I$</td>
<td>Invalid (Hi-impedance)</td>
<td>$Z$</td>
<td>Hi-impedance</td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 12-4: LOAD CONDITIONS**

Load Condition 1

- $V_{DD}/2$
- $R_L = 464\Omega$
- $C_L = 50\, pF$ for all pins
- $15\, pF$ for OSC2 output

Load Condition 2

- $V_{SS}$
- $C_L$
- $Pin$
### 12.9 AC CHARACTERISTICS: PIC12F629/675 (INDUSTRIAL, EXTENDED)

#### FIGURE 12-5: EXTERNAL CLOCK TIMING

![External Clock Timing Diagram](image)

#### TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fosc</td>
<td></td>
<td>External CLKIN Frequency(^{(1)})</td>
<td>DC</td>
<td>—</td>
<td>37</td>
<td>kHz</td>
<td>LP Osc mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>XT mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
<td>HS mode</td>
</tr>
<tr>
<td></td>
<td>Fosc</td>
<td></td>
<td>DC</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
<td>EC mode</td>
</tr>
<tr>
<td>Osc</td>
<td>Osc</td>
<td>Oscillator Frequency(^{(1)})</td>
<td>5</td>
<td>—</td>
<td>37</td>
<td>kHz</td>
<td>INTOSC mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>RC Osc mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.1</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>XT Osc mode</td>
</tr>
<tr>
<td></td>
<td>Osc</td>
<td></td>
<td>1</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
<td>HS Osc mode</td>
</tr>
<tr>
<td>Tosc</td>
<td></td>
<td>External CLKIN Period(^{(1)})</td>
<td>27</td>
<td>—</td>
<td>∞</td>
<td>µs</td>
<td>LP Osc mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>—</td>
<td>∞</td>
<td>ns</td>
<td>HS Osc mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>—</td>
<td>∞</td>
<td>ns</td>
<td>EC Osc mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>∞</td>
<td>ns</td>
<td>XT Osc mode</td>
</tr>
<tr>
<td>Osc</td>
<td>Osc</td>
<td>Oscillator Period(^{(1)})</td>
<td>27</td>
<td>—</td>
<td>200</td>
<td>µs</td>
<td>INTOSC mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>10,000</td>
<td>ns</td>
<td>RC Osc mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>XT Osc mode</td>
</tr>
<tr>
<td></td>
<td>Osc</td>
<td></td>
<td>50</td>
<td>—</td>
<td>1,000</td>
<td>ns</td>
<td>HS Osc mode</td>
</tr>
<tr>
<td>TCY</td>
<td></td>
<td>Instruction Cycle Time(^{(1)})</td>
<td>200</td>
<td>TCY</td>
<td>DC</td>
<td>ns</td>
<td>TCY = 4/Fosc</td>
</tr>
<tr>
<td>TosL,</td>
<td></td>
<td>External CLKIN (OSC1) High</td>
<td>2*</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>LP oscillator, Tosc L/H duty cycle</td>
</tr>
<tr>
<td>TosH</td>
<td></td>
<td>External CLKIN Low</td>
<td>20*</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>HS oscillator, Tosc L/H duty cycle</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External CLKIN (OSC1) High</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>XT oscillator, Tosc L/H duty cycle</td>
</tr>
<tr>
<td>TosR,</td>
<td></td>
<td>External CLKIN Rise</td>
<td>—</td>
<td>—</td>
<td>50*</td>
<td>ns</td>
<td>LP oscillator</td>
</tr>
<tr>
<td>TosF</td>
<td></td>
<td>External CLKIN Fall</td>
<td>—</td>
<td>—</td>
<td>25*</td>
<td>ns</td>
<td>XT oscillator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>15*</td>
<td>ns</td>
<td>HS oscillator</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at ‘min’ values with an external clock applied to OSC1 pin. When an external clock input is used, the ‘max’ cycle time limit is ‘DC’ (no clock) for all devices.
TABLE 12-2:  PRECISION INTERNAL OSCILLATOR PARAMETERS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Freq Tolerance</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>F10</td>
<td>Fosc</td>
<td>Internal Calibrated INTOSC Frequency</td>
<td>±1</td>
<td>3.96</td>
<td>4.00</td>
<td>4.04</td>
<td>MHz</td>
<td>Vdd = 3.5V, 25°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>±2</td>
<td>3.92</td>
<td>4.00</td>
<td>4.08</td>
<td>MHz</td>
<td>2.5V ≤ Vdd ≤ 5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>±5</td>
<td>3.80</td>
<td>4.00</td>
<td>4.20</td>
<td>MHz</td>
<td>0°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td>F14</td>
<td>Tiosc</td>
<td>Oscillator Wake-up from SLEEP start-up time*</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>6</td>
<td>μs</td>
<td>Vdd = 2.0V, -40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>4</td>
<td>μs</td>
<td>Vdd = 3.0V, -40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>3</td>
<td>μs</td>
<td>Vdd = 5.0V, -40°C to +85°C</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
### FIGURE 12-6: CLKOUT AND I/O TIMING

![FIGURE 12-6: CLKOUT AND I/O TIMING](image)

### TABLE 12-3: CLKOUT AND I/O TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>TosH2ckL</td>
<td>OSC1↑ to CLK-OUT↓</td>
<td>—</td>
<td>75</td>
<td>200</td>
<td>ns</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>11</td>
<td>TosH2ckH</td>
<td>OSC1↑ to CLK-OUT↑</td>
<td>—</td>
<td>75</td>
<td>200</td>
<td>ns</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>12</td>
<td>TckR</td>
<td>CLKOUT rise time</td>
<td>—</td>
<td>35</td>
<td>100</td>
<td>ns</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>13</td>
<td>TckF</td>
<td>CLKOUT fall time</td>
<td>—</td>
<td>35</td>
<td>100</td>
<td>ns</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>14</td>
<td>TckL2ioV</td>
<td>CLKOUT↓ to Port out valid</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>15</td>
<td>TioV2ckH</td>
<td>Port in valid before CLKOUT↑</td>
<td>Tosc + 200 ns</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>16</td>
<td>Tckh2iol</td>
<td>Port in hold after CLKOUT↑</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>17</td>
<td>TosH2ioV</td>
<td>OSC1↑ (Q1 cycle) to Port out valid</td>
<td>—</td>
<td>50</td>
<td>150</td>
<td>*ns</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>TosH2ioI</td>
<td>OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>TioV2osH</td>
<td>Port input valid to OSC1↑ (I/O in setup time)</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>TioR</td>
<td>Port output rise time</td>
<td>—</td>
<td>10</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>TioF</td>
<td>Port output fall time</td>
<td>—</td>
<td>10</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>Tinp</td>
<td>INT pin high or low time</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Trbp</td>
<td>GPIO change INT high or low time</td>
<td>Tcy</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated.

**Note 1:** Measurements are taken in RC mode where CLKOUT output is 4xTosc.
FIGURE 12-7: 
RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

FIGURE 12-8: 
BROWN-OUT DETECT TIMING AND CHARACTERISTICS

Note 1: 72 ms delay only if PWRT bit in configuration word is programmed to '0'.
### TABLE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT DETECT REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>TmCL</td>
<td>MCLR Pulse Width (low)</td>
<td>2 TBD</td>
<td>— TBD</td>
<td>— TBD</td>
<td>µs ms</td>
<td>VDD = 5V, -40°C to +85°C Extended temperature</td>
</tr>
<tr>
<td>31</td>
<td>TwDT</td>
<td>Watchdog Timer Time-out Period (No Prescaler)</td>
<td>10 10</td>
<td>17 17</td>
<td>25 30</td>
<td>ms ms</td>
<td>VDD = 5V, -40°C to +85°C Extended temperature</td>
</tr>
<tr>
<td>32</td>
<td>TOST</td>
<td>Oscillation Start-up Timer Period</td>
<td>— 1024Tosc</td>
<td>— —</td>
<td>—</td>
<td>—</td>
<td>Tosc = OSC1 period</td>
</tr>
<tr>
<td>33*</td>
<td>TPWRT</td>
<td>Power-up Timer Period</td>
<td>28* TBD</td>
<td>72 TBD</td>
<td>132* TBD</td>
<td>ms ms</td>
<td>VDD = 5V, -40°C to +85°C Extended Temperature</td>
</tr>
<tr>
<td>34</td>
<td>TIOZ</td>
<td>I/O Hi-impedance from MCLR Low or Watchdog Timer Reset</td>
<td>— —</td>
<td>2.0</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>BVDD</td>
<td>Brown-out Detect Voltage</td>
<td>2.025</td>
<td>—</td>
<td>2.175</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Brown-out Hysteresis</td>
<td>TBD</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>TBOD</td>
<td>Brown-out Detect Pulse Width</td>
<td>100*</td>
<td>— —</td>
<td>—</td>
<td>µs</td>
<td>VDD ≤ BVDD (D005)</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
TABLE 12-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>40*</td>
<td>T0H</td>
<td>T0CKI High Pulse Width</td>
<td>No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>41*</td>
<td>T0L</td>
<td>T0CKI Low Pulse Width</td>
<td>No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>42*</td>
<td>T0P</td>
<td>T0CKI Period</td>
<td>Greater of:</td>
<td>20 or TCY + 40 N</td>
<td>—</td>
<td>ns</td>
<td>N = prescale value (2, 4, ..., 256)</td>
</tr>
<tr>
<td>45*</td>
<td>T1H</td>
<td>T1CKI High Time</td>
<td>Synchronous, No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Synchronous, with Prescaler</td>
<td>15</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>30</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>46*</td>
<td>T1L</td>
<td>T1CKI Low Time</td>
<td>Synchronous, No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Synchronous, with Prescaler</td>
<td>15</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>30</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>47*</td>
<td>T1P</td>
<td>T1CKI Input Period</td>
<td>Synchronous</td>
<td>Greater of: 30 or TCY + 40 N</td>
<td>—</td>
<td>ns</td>
<td>N = prescale value (1, 2, 4, 8)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>60</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)</td>
<td>DC</td>
<td>200* kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>TCKE</td>
<td>Delay from external clock edge to timer increment</td>
<td>2 Tosc*</td>
<td>—</td>
<td>7 Tosc*</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
### TABLE 12-6: COMPARATOR SPECIFICATIONS

<table>
<thead>
<tr>
<th>Comparator Specifications</th>
<th>Standard Operating Conditions: -40°C to +125°C (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sym</td>
<td>Characteristics</td>
</tr>
<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
</tr>
<tr>
<td>VCM</td>
<td>Input Common Mode Voltage</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
</tr>
<tr>
<td>TRT</td>
<td>Response Time(1)</td>
</tr>
<tr>
<td>TMC2COV</td>
<td>Comparator Mode Change to Output Valid</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

**Note 1:** Response time measured with one comparator input at (VDD - 1.5)/2 while the other input transitions from VSS to VDD - 1.5V.

### TABLE 12-7: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

<table>
<thead>
<tr>
<th>Voltage Reference Specifications</th>
<th>Standard Operating Conditions: -40°C to +125°C (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sym</td>
<td>Characteristics</td>
</tr>
<tr>
<td>Resolution</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td>Absolute Accuracy</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td>Unit Resistor Value (R)</td>
<td>—</td>
</tr>
<tr>
<td>Settling Time(1)</td>
<td>—</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

**Note 1:** Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.
## TABLE 12-8: PIC12F675 A/D CONVERTER CHARACTERISTICS:

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>A01</td>
<td>NR</td>
<td>Resolution</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>bits</td>
<td></td>
</tr>
<tr>
<td>A02</td>
<td>EABS</td>
<td>Total Absolute Error*</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSb</td>
<td>VREF = 5.0V</td>
</tr>
<tr>
<td>A03</td>
<td>EIL</td>
<td>Integral Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSb</td>
<td>VREF = 5.0V</td>
</tr>
<tr>
<td>A04</td>
<td>EDL</td>
<td>Differential Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSb</td>
<td>No missing codes to 10 bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VREF = 5.0V</td>
</tr>
<tr>
<td>A05</td>
<td>EFS</td>
<td>Full Scale Range</td>
<td>2.2</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>A06</td>
<td>EOFF</td>
<td>Offset Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSb</td>
<td>VREF = 5.0V</td>
</tr>
<tr>
<td>A07</td>
<td>EGN</td>
<td>Gain Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSb</td>
<td>VREF = 5.0V</td>
</tr>
<tr>
<td>A10</td>
<td></td>
<td>Monotonicity</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>VSS ≤ VAIN ≤ VREF+</td>
</tr>
<tr>
<td>A20</td>
<td>VREF</td>
<td>Reference Voltage</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>VDD + 0.3</td>
<td>Absolute minimum to ensure 10-bit accuracy</td>
</tr>
<tr>
<td>A20A</td>
<td></td>
<td></td>
<td>2.5</td>
<td>—</td>
<td>—</td>
<td>VDD + 0.3</td>
<td></td>
</tr>
<tr>
<td>A21</td>
<td>VREF</td>
<td>Reference V High (VDD or VREF)</td>
<td>VSS</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>A25</td>
<td>VAIN</td>
<td>Analog Input Voltage</td>
<td>VSS</td>
<td>—</td>
<td>VREF</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>A30</td>
<td>ZAIN</td>
<td>Recommended Impedance of Analog Voltage Source</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>A50</td>
<td>IREF</td>
<td>VREF Input Current(2)</td>
<td>10</td>
<td>—</td>
<td>1000</td>
<td>μA</td>
<td>During VAIN acquisition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>μA</td>
<td>Based on differential of VHOLD to VAIN. During A/D conversion cycle.</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

**Note 2:** VREF current is from External VREF or VDD pin, whichever is selected as reference input.

**Note 3:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.
FIGURE 12-10: PIC12F675 A/D CONVERSION TIMING (NORMAL MODE)

Note 1: If the A/D clock source is selected as RC, a time of $T_{CY}$ is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

Note 2: See Section 7.1 for minimum conditions.

TABLE 12-9: PIC12F675 A/D CONVERSION REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>130</td>
<td>TAD</td>
<td>A/D Clock Period</td>
<td>1.6</td>
<td>—</td>
<td>—</td>
<td>$\mu$s</td>
<td>$T_{OSC}$ based, $V_{REF} \geq 3.0V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.0*</td>
<td>—</td>
<td>—</td>
<td>$\mu$s</td>
<td>$T_{OSC}$ based, $V_{REF}$ full range</td>
</tr>
<tr>
<td>130</td>
<td>TAD</td>
<td>A/D Internal RC Oscillator Period</td>
<td>3.0*</td>
<td>6.0</td>
<td>9.0*</td>
<td>$\mu$s</td>
<td>$ADCS&lt;1:0&gt; = 11$ (RC mode)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.0*</td>
<td>4.0</td>
<td>6.0*</td>
<td>$\mu$s</td>
<td>$V_{DD} = 2.5V$</td>
</tr>
<tr>
<td>131</td>
<td>TCNV</td>
<td>Conversion Time (not including Acquisition Time)$^{(1)}$</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>TAD</td>
<td>Set GO bit to new data in A/D result register</td>
</tr>
<tr>
<td>132</td>
<td>TACQ</td>
<td>Acquisition Time</td>
<td>(Note 2)</td>
<td>11.5</td>
<td>—</td>
<td>$\mu$s</td>
<td>The minimum time is the amplifier settling time. This may be used if the &quot;new&quot; input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored in CHOLD).</td>
</tr>
<tr>
<td>134</td>
<td>TGO</td>
<td>Q4 to A/D Clock Start</td>
<td>—</td>
<td>$T_{OSC}/2$</td>
<td>—</td>
<td>—</td>
<td>If the A/D clock source is selected as RC, a time of $T_{CY}$ is added before the A/D clock starts. This allows the SLEEP instruction to be executed.</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following Tcy cycle.
2: See Section 7.1 for minimum conditions.
**FIGURE 12-11:** PIC12F675 A/D CONVERSION TIMING (SLEEP MODE)

**TABLE 12-10: PIC12F675 A/D CONVERSION REQUIREMENTS (SLEEP MODE)**

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>130</td>
<td>TAD</td>
<td>A/D Clock Period</td>
<td>1.6</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>VREF ≥ 3.0V</td>
</tr>
<tr>
<td>130</td>
<td>TAD</td>
<td>A/D Internal RC Oscillator Period</td>
<td>3.0*</td>
<td>6.0</td>
<td>9.0*</td>
<td>µs</td>
<td>VREF full range</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.0*</td>
<td>4.0</td>
<td>6.0*</td>
<td>µs</td>
<td>ADCS&lt;1:0&gt; = 11 (RC mode)</td>
</tr>
<tr>
<td>131</td>
<td>TCVN</td>
<td>Conversion Time (not including</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>TAD</td>
<td>TAD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Acquisition Time) (1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>132</td>
<td>TACQ</td>
<td>Acquisition Time</td>
<td>(Note 2)</td>
<td>11.5</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5*</td>
<td>—</td>
<td>µs</td>
<td>The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).</td>
</tr>
<tr>
<td>134</td>
<td>TGO</td>
<td>Q4 to A/D Clock Start</td>
<td>—</td>
<td>TOSC/2 + TCY</td>
<td>—</td>
<td>—</td>
<td>If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.  
† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.  

**Note 1:** If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.  

**Note 1:** ADRES register may be read on the following TCY cycle.  
2: See Section 7.1 for minimum conditions.
13.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for design guidance and are not tested.

In some graphs or tables, the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are ensured to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25°C. ‘Max’ or ‘min’ represents (mean + 3σ) or (mean - 3σ) respectively, where σ is standard deviation, over the whole temperature range.

FIGURE 13-1: TYPICAL IPD vs. VDD OVER TEMP (-40°C TO +25°C)

FIGURE 13-2: TYPICAL IPD vs. VDD OVER TEMP (+85°C)
FIGURE 13-3:  TYPICAL \( I_{PD} \) vs. \( V_{DD} \) OVER TEMP (+125°C)

FIGURE 13-4:  MAXIMUM \( I_{PD} \) vs. \( V_{DD} \) OVER TEMP (-40°C TO +25°C)
FIGURE 13-5: MAXIMUM \( I_{PD} \) vs. \( V_{DD} \) OVER TEMP (+85°C)

![Maximum Baseline \( I_{PD} \)]

FIGURE 13-6: MAXIMUM \( I_{PD} \) vs. \( V_{DD} \) OVER TEMP (+125°C)

![Maximum Baseline \( I_{PD} \)]
FIGURE 13-7: TYPICAL IPD WITH BOD ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)

Typical BOD IPD

FIGURE 13-8: TYPICAL IPD WITH CMP ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)

Typical Comparator IPD
FIGURE 13-9: TYPICAL IPD WITH A/D ENABLED vs. VDD OVER TEMP (-40°C TO +25°C)

Typical A/D IPD

FIGURE 13-10: TYPICAL IPD WITH A/D ENABLED vs. VDD OVER TEMP (+85°C)

Typical A/D IPD
FIGURE 13-11: TYPICAL IPD WITH A/D ENABLED vs. VDD OVER TEMP (+125°C)

Typical A/D IPD

FIGURE 13-12: TYPICAL IPD WITH T1 OSC ENABLED vs. VDD OVER TEMP (-40°C TO +125°C), 32 KHZ, C1 AND C2=50 pF

Typical T1 IPD
FIGURE 13-13: TYPICAL IPD WITH CVREF ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)

Typical CVREF IPD

FIGURE 13-14: TYPICAL IPD WITH WDT ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)

Typical WDT IPD
FIGURE 13-15: MAXIMUM AND MINIMUM INTOSC FREQ vs. TEMPERATURE WITH 0.1µF AND 0.01µF DECOUPLING (VDD = 3.5V)

Internal Oscillator Frequency vs Temperature

Temperature (°C)

Frequency (Hz)

-3sigma
average
+3sigma

FIGURE 13-16: MAXIMUM AND MINIMUM INTOSC FREQ vs. VDD WITH 0.1µF AND 0.01µF DECOUPLING (+25°C)

Internal Oscillator Frequency vs VDD

VDD (V)

Frequency (Hz)

-3sigma
average
+3sigma
FIGURE 13-17: TYPICAL WDT PERIOD vs. \( V_{DD} \) (-40°C TO +125°C)
14.0 PACKAGING INFORMATION

14.1 Package Marking Information

8-Lead PDIP (Skinny DIP)

<table>
<thead>
<tr>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>12F629-I/017</td>
</tr>
<tr>
<td>0215</td>
</tr>
</tbody>
</table>

Legend:  
- XX...X Customer specific information*
- YY Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week ‘01’)
- NNN Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.
14.2 Package Details
The following sections give the technical details of the packages.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

---

**Units** | **INCHES** | **MILLIMETERS**
---|---|---
Number of Pins | n | 8 | 8
Pitch | p | .100 | 2.54
Top to Seating Plane | A | .140 | .155 | .170 | 3.56 | 3.94 | 4.32
Molded Package Thickness | A2 | .115 | .130 | .145 | 2.92 | 3.30 | 3.68
Base to Seating Plane | A1 | .015 | 0.38
Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26
Molded Package Width | E1 | .240 | .250 | .260 | 6.10 | 6.35 | 6.60
Overall Length | D | .360 | .373 | .385 | 9.14 | 9.46 | 9.78
Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43
Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38
Upper Lead Width | B1 | .045 | .058 | .070 | 1.14 | 1.46 | 1.78
Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56
Overall Row Spacing | eB | .310 | .370 | .430 | 7.87 | 9.40 | 10.92
Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15
Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018
8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

<table>
<thead>
<tr>
<th>Units</th>
<th>INCHES*</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
<td>NOM</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>.050</td>
<td>1.27</td>
</tr>
<tr>
<td>Overall Height</td>
<td>.069</td>
<td>.81</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>.061</td>
<td>1.55</td>
</tr>
<tr>
<td>Standoff §</td>
<td>.010</td>
<td>0.25</td>
</tr>
<tr>
<td>Overall Width</td>
<td>.244</td>
<td>6.20</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>.157</td>
<td>3.99</td>
</tr>
<tr>
<td>Overall Length</td>
<td>.197</td>
<td>5.00</td>
</tr>
<tr>
<td>Chamfer Distance</td>
<td>.020</td>
<td>0.51</td>
</tr>
<tr>
<td>Foot Length</td>
<td>.030</td>
<td>0.76</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>.010</td>
<td>0.25</td>
</tr>
<tr>
<td>Lead Width</td>
<td>.020</td>
<td>0.42</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>15</td>
<td>0.15</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>15</td>
<td>0.15</td>
</tr>
</tbody>
</table>

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

© 2003 Microchip Technology Inc.
8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S)

**Units** | **INCHES** | **MILLIMETERS**
---|---|---
**Dimension Limits** | **MIN** | **NOM** | **MAX** | **MIN** | **NOM** | **MAX**
Number of Pins | n | | | | | |
Pitch | P | .050 BSC | | | | |
Overall Height | A | .033 | .039 | .85 | 1.00 |
Molded Package Thickness | A2 | .026 | .031 | .65 | .80 |
Standoff | A1 | .000 | .0004 | .002 | .00 | .01 | .05 |
Base Thickness | A3 | .008 REF. | | | | |
Overall Length | E | .194 BSC | | | | |
Molded Package Length | E1 | .184 BSC | | | | |
Exposed Pad Length | E2 | .152 | .158 | .163 | 3.85 | 4.00 | 4.15 |
Overall Width | D | .236 BSC | | | | |
Molded Package Width | D1 | .226 BSC | | | | |
Exposed Pad Width | D2 | .085 | .091 | .097 | 2.16 | 2.31 | 2.46 |
Lead Width | B | .014 | .016 | .019 | 0.35 | 0.40 | 0.47 |
Lead Length | L | .020 | .024 | .030 | 0.50 | 0.60 | 0.75 |
Tie Bar Width | R | .014 | | | | |
Mold Draft Angle Top | α | | | | | |

*Controlling Parameter

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC equivalent: pending

Drawing No. C04-113
8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S)
Land Pattern and Solder Mask

<table>
<thead>
<tr>
<th>Units</th>
<th>INCHES</th>
<th>MILLIMETERS*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>MIN</td>
<td>NOM</td>
</tr>
<tr>
<td>Pitch</td>
<td>P</td>
<td>.014</td>
</tr>
<tr>
<td>Pad Width</td>
<td>B</td>
<td>.020</td>
</tr>
<tr>
<td>Pad Length</td>
<td>L</td>
<td>.005</td>
</tr>
<tr>
<td>Pad to Solder</td>
<td>M</td>
<td>.005</td>
</tr>
</tbody>
</table>

*Controlling Parameter

Drawing No. C04-2113
APPENDIX A: DATA SHEET

Revision A
This is a new data sheet.

Revision B
Added characterization graphs.
Updated specifications.
Added notes to indicate Microchip programmers maintain all calibration bits to factory settings and the PIC12F675 ANSEL register must be initialized to configure pins as digital I/O.
Updated MLF-S package name to DFN-S.

APPENDIX B: DEVICE DIFFERENCES

The differences between the PIC12F629/675 devices listed in this data sheet are shown in Table B-1.

<table>
<thead>
<tr>
<th>Feature</th>
<th>PIC12F629</th>
<th>PIC12F675</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
APPENDIX C: DEVICE MIGRATIONS

This section is intended to describe the functional and electrical specification differences when migrating between functionally similar devices (such as from a PIC16C74A to a PIC16C74B).

Not Applicable

APPENDIX D: MIGRATING FROM OTHER PICmicro® DEVICES

This discusses some of the issues in migrating from other PICmicro devices to the PIC12F6XX family of devices.

D.1 PIC12C67X to PIC12F6XX

TABLE 1: FEATURE COMPARISON

<table>
<thead>
<tr>
<th>Feature</th>
<th>PIC12C67X</th>
<th>PIC12F6XX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Operating Speed</td>
<td>10 MHz</td>
<td>20 MHz</td>
</tr>
<tr>
<td>Max Program Memory</td>
<td>2048 bytes</td>
<td>1024 bytes</td>
</tr>
<tr>
<td>A/D Resolution</td>
<td>8-bit</td>
<td>10-bit</td>
</tr>
<tr>
<td>Data EEPROM</td>
<td>16 bytes</td>
<td>64 bytes</td>
</tr>
<tr>
<td>Oscillator Modes</td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>Brown-out Detect</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>Internal Pull-ups</td>
<td>GP0/1/3</td>
<td>GP0/1/2/4/5</td>
</tr>
<tr>
<td>Interrupt-on-change</td>
<td>GP0/1/3</td>
<td>GP0/1/2/3/4/5</td>
</tr>
<tr>
<td>Comparator</td>
<td>N</td>
<td>Y</td>
</tr>
</tbody>
</table>

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.
INDEX

A
A/D................................................................. 41
Acquisition Requirements ............................... 45
Block Diagram .................................................. 41
Calculating Acquisition Time ................................ 45
Configuration and Operation ............................ 41
Effects of a RESET ............................................ 46
Internal Sampling Switch (Rss) Impedance ............ 45
Operation During SLEEP ..................................... 46
PIC12F675 Converter Characteristics .................. 101
Source Impedance ............................................. 45
Summary of Registers ........................................ 46
Absolute Maximum Ratings .............................. 83
AC Characteristics
Industrial and Extended ....................................... 94
Additional Pin Functions .................................... 19
Interrupt-on-Change .......................................... 21
Weak Pull-up....................................................... 19
Analog Input Connection Considerations ............... 38
Analog-to-Digital Converter. See A/D
Assembler MPASM Assembler .............................. 77

B
Block Diagram
TMR0/WDT Prescaler ........................................... 27
Block Diagrams
Analog Input Mode ............................................. 38
Analog Input Model ............................................ 45
Comparator Output .............................................. 38
Comparator Voltage Reference ............................ 39
GP0 and GP1 Pins .............................................. 22
GP2 ............................................................... 23
GP3 ............................................................... 23
GP4 ............................................................... 24
GP5 ............................................................... 24
On-Chip Reset Circuit ......................................... 55
RC Oscillator Mode ............................................ 54
Timer1 .................................................................. 30
Watchdog Timer .................................................. 65
Brown-out
Associated Registers ........................................... 58
Brown-out Detect (BOD) ....................................... 57
Brown-out Detect Timing and Characteristics ......... 97

C
C Compilers
MLAB C17 ......................................................... 78
MLAB C18 ......................................................... 78
MLAB C30 ......................................................... 78
Calibrated Internal RC Frequencies ........................ 95
CLKOUT ........................................................... 54
Code Examples
Changing Prescaler ............................................ 29
Data EEPROM Read .......................................... 49
Data EEPROM Write ......................................... 49
Initializing GPIO ............................................... 19
Saving STATUS and W Registers in RAM ............. 64
Write Verify ....................................................... 49
Code Protection ............................................... 67
Comparator
Associated Registers .......................................... 40
Configuration .................................................... 37
Effects of a RESET ............................................ 39
I/O Operating Modes ......................................... 37
Interrupts ......................................................... 40
Operation........................................................ 36
Operation During SLEEP ...................................... 39
Output ............................................................ 38
Reference ......................................................... 39
Response Time ................................................ 39
Comparator Specifications ................................. 100
Comparator Voltage Reference Specifications ....... 100
Configuration Bits .............................................. 52
Configuring the Voltage Reference ....................... 39
Crystal Operation .............................................. 53

D
Data EEPROM Memory
Associated Registers/Bits .................................... 50
Code Protection ................................................. 50
EADDR Register ................................................... 47
EECON1 Register .............................................. 47
EECON2 Register .............................................. 47
EEDATA Register ............................................ 47
Data Memory Organization .................................. 7
DC Characteristics
Extended and Industrial ...................................... 91
Industrial ......................................................... 86
Demonstration Boards
PICDEM 1 ......................................................... 80
PICDEM 17 ......................................................... 80
PICDEM 18R PIC18C601/801 ................................ 81
PICDEM 2 Plus ................................................. 80
PICDEM 3 PIC16C92X ......................................... 80
PICDEM LIN PIC16C43X ..................................... 81
PICDEM USB PIC16C7X5 ................................. 81
PICDEM.net Internet/Ethernet ............................ 80
Development Support ......................................... 77
Device Differences .......................................... 121
Device Migrations ............................................. 122
Device Overview .............................................. 5
EEPROM Data Memory
Reading .......................................................... 49
Spurious Write ................................................. 49
Write Verify ....................................................... 49
Writing ............................................................. 49
Electrical Specifications ...................................... 83
Errata .............................................................. 3
Evaluation and Programming Tools ..................... 81
F
Firmware Instructions ......................................... 69
G
General Purpose Register File ............................... 7
GPIO
Associated Registers .......................................... 25
GPIO Port ......................................................... 19
GPIO, TRISIO Registers ....................................... 19
ID Locations ..................................................... 67
In-Circuit Debugger ......................................... 67
In-Circuit Serial Programming ........................... 67
Indirect Addressing, INDF and FSR Registers ....... 18
Instruction Format ............................................. 69
Instruction Set ................................................... 69
ADDLW .......................................................... 71
ADDWF ........................................................ 71
ANDLW ........................................................ 71
ANDWF ........................................................ 71
BCF ............................................................. 71

DS41190C-page 124

PIC12F629/675

Stack.................................................17
PICkit 1 FLASH Starter Kit..................51
PICSTART Plus Development Programmer 79
Pin Descriptions and Diagrams ..........22
Pinout Descriptions
PIC12F629 ........................................ 6
PIC12F675 ........................................ 6
Power Control/Status Register (PCON) ....57
Power-Down Mode (SLEEP) .................66
Power-on Reset (POR) .........................56
Power-up Timer (PWRT) ......................56
Prescaler ..........................................29
Switching Prescaler Assignment ...........29
PRO MATE II Universal Device Programmer 79
Program Memory Organization ..........7
Programming, Device Instructions .....69

R
RC Oscillator .....................................54
READ-MODIFY-WRITE OPERATIONS ....69

Registers
ADCON0 (A/D Control) .........................43
ANSEL (Analog Select) .........................44
CMCON (Comparator Control) .............35
CONFIG (Configuration Word) .............52
EEADR (EEPROM Address) .................47
EECON1 (EEPROM Control) .................48
EEEDT (EEPROM Data) .......................47
INTCON (Interrupt Control) .................13
IOC (Interrupt-on-Change GPIO) ............21
Maps
PIC12F629 ........................................ 8
PIC12F675 ........................................ 8
OPTION_REG (Option) .........................12, 28
OSC CAL (Oscillator Calibration) .........16
PCON (Power Control) .........................16
PIE1 (Peripheral Interrupt Enable 1) ....14
PIR1 (Peripheral Interrupt 1) ..............15
STATUS .............................................11
T1CON (Timer1 Control) ......................32
VRCON (Voltage Reference Control) ......40
WPU (Weak Pull-up) .........................20

RESET .............................................55
Revision History ................................121

S
Software Simulator (MPLAB SIM) ..........78
Software Simulator (MPLAB SIM30) .......78
Special Features of the CPU ...............51
Special Function Registers .................8
Special Functions Registers Summary .......9

T
Time-out Sequence ..............................57
Timer0 .............................................27
Associated Registers .........................29
External Clock ..................................28
Interrupt .........................................27
Operation ........................................27
TOCKI .............................................28

Timer1
Associated Registers .........................33
Asynchronous Counter Mode .................33
Reading and Writing ..........................33
Interrupt .........................................31
Modes of Operations ..........................31
Operation During SLEEP .....................31
Oscillator .........................................33

N
Maps
PIC12F629 ........................................ 8
PIC12F675 ........................................ 8
OPTION_REG (Option) .........................12, 28
OSC CAL (Oscillator Calibration) .........16
PCON (Power Control) .........................16
PIE1 (Peripheral Interrupt Enable 1) ....14
PIR1 (Peripheral Interrupt 1) ..............15
STATUS .............................................11
T1CON (Timer1 Control) ......................32
VRCON (Voltage Reference Control) ......40
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RESET .............................................55
Revision History ................................121

S
Software Simulator (MPLAB SIM) ..........78
Software Simulator (MPLAB SIM30) .......78
Special Features of the CPU ...............51
Special Function Registers .................8
Special Functions Registers Summary .......9

T
Time-out Sequence ..............................57
Timer0 .............................................27
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External Clock ..................................28
Interrupt .........................................27
Operation ........................................27
TOCKI .............................................28

Timer1
Associated Registers .........................33
Asynchronous Counter Mode .................33
Reading and Writing ..........................33
Interrupt .........................................31
Modes of Operations ..........................31
Operation During SLEEP .....................31
Oscillator .........................................33

O
OPCODE Field Descriptions .................69
Oscillator Configurations ...................53
Oscillator Start-up Timer (OST) ..........56

P
Packaging ...........................................115
Details ..............................................116
Marking ...........................................115
PCL and PCLATH .................................17
Computed GOTO .................................17

M
MCLR ................................................56
Memory Organization
Data EEPROM Memory .........................47
Migrating from other PICmicro Devices ....122
MPLAB ASM30 Assembler, Linker, Librarian 78
MPLAB ICD 2 In-Circuit Debugger ..........79
MPLAB ICE 2000 High Performance Universal
In-Circuit Emulator .........................79
MPLAB ICE 4000 High Performance Universal
In-Circuit Emulator .........................79
MPLAB Integrated Development Environment Software ..........77
MPLINK Object Linker/MPLIB Object Librarian ........78

O
OPCODE Field Descriptions .................69
Oscillator Configurations ...................53
Oscillator Start-up Timer (OST) ..........56

P
Packaging ...........................................115
Details ..............................................116
Marking ...........................................115
PCL and PCLATH .................................17
Computed GOTO .................................17

M
MCLR ................................................56
Memory Organization
Data EEPROM Memory .........................47
Migrating from other PICmicro Devices ....122
MPLAB ASM30 Assembler, Linker, Librarian 78
MPLAB ICD 2 In-Circuit Debugger ..........79
MPLAB ICE 2000 High Performance Universal
In-Circuit Emulator .........................79
MPLAB ICE 4000 High Performance Universal
In-Circuit Emulator .........................79
MPLAB Integrated Development Environment Software ..........77
MPLINK Object Linker/MPLIB Object Librarian ........78

O
OPCODE Field Descriptions .................69
Oscillator Configurations ...................53
Oscillator Start-up Timer (OST) ..........56

P
Packaging ...........................................115
Details ..............................................116
Marking ...........................................115
PCL and PCLATH .................................17
Computed GOTO .................................17

DS41190C-page 124

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Literature Number: DS41190C

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7. How would you improve this document?
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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>XX</th>
<th>XXX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>PIC12F6XX: Standard Vco range</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>PIC12F6XXT: (Tape and Reel)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I</td>
<td>+40°C to +85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>+40°C to +125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td>P = PDIP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SN</td>
<td>SOIC (Gull wing, 150 mil body)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MF</td>
<td>MLF-S</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pattern</td>
<td>3-Digit Pattern Code for QTP (blank otherwise)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Examples:

a) PIC12F629 – E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301
b) PIC12F675 – I/SO = Industrial Temp., SOIC package, 20 MHz

* JW Devices are UVerasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.

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