NOTE: The Intel 64 and IA-32 Architectures Software Developer’s Manual consists of five volumes: Basic Architecture, Order Number 253665; Instruction Set Reference A-M, Order Number 253666; Instruction Set Reference N-Z, Order Number 253667; System Programming Guide, Part 1, Order Number 253668; System Programming Guide, Part 2, Order Number 253669. Refer to all five volumes when evaluating your design needs.
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- The Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1: Basic Architecture (Order Number 253665).

The Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, describes the basic architecture and programming environment of Intel 64 and IA-32 processors. The Intel® 64 and IA-32 Architectures Software Developer's Manual, Volumes 2A & 2B, describe the instruction set of the processor and the opcode structure. These volumes apply to application programmers and to programmers who write operating systems or executives. The Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volumes 3A & 3B, describe the operating-system support environment of Intel 64 and IA-32 processors. These volumes target operating-system and BIOS designers. In addition, the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B, addresses the programming environment for classes of software that host operating systems.

### 1.1 IA-32 PROCESSORS COVERED IN THIS MANUAL

This manual set includes information pertaining primarily to the most recent Intel 64 and IA-32 processors, which include:

- Pentium® processors
- P6 family processors
- Pentium® 4 processors
- Pentium® M processors
- Intel® Xeon® processors
- Pentium® D processors
- Pentium® processor Extreme Editions
- 64-bit Intel® Xeon® processors
- Intel® Core™ Duo processor
- Intel® Core™ Solo processor
- Dual-Core Intel® Xeon® processor LV
ABOUT THIS MANUAL

- Intel® Core™2 Duo processor
- Intel® Core™2 Quad processor Q6000 series
- Intel® Xeon® processor 3000, 3200 series
- Intel® Xeon® processor 5000 series
- Intel® Xeon® processor 5100, 5300 series
- Intel® Core™2 Extreme processor X7000 and X6800 series
- Intel® Core™2 Extreme QX6000 series
- Intel® Xeon® processor 7100 series
- Intel® Pentium® Dual-Core processor
- Intel® Xeon® processor 7200, 7300 series
- Intel® Xeon® processor 5200, 5400, 7400 series
- Intel® Core™2 Extreme processor QX9000 and X9000 series
- Intel® Core™2 Quad processor Q9000 series
- Intel® Core™2 Duo processor E8000, T9000 series
- Intel® Atom™ processor family
- Intel® Core™i7 processor
- Intel® Core™i5 processor

P6 family processors are IA-32 processors based on the P6 family microarchitecture. This includes the Pentium® Pro, Pentium® II, Pentium® III, and Pentium® III Xeon® processors.


The Intel® Core™ Duo, Intel® Core™ Solo and dual-core Intel® Xeon® processor LV are based on an improved Pentium® M processor microarchitecture.

The Intel® Xeon® processor 3000, 3200, 5100, 5300, 7200, and 7300 series, Intel® Pentium® dual-core, Intel® Core™2 Duo, Intel® Core™2 Quad, and Intel® Core™2 Extreme processors are based on Intel® Core™ microarchitecture.

The Intel® Xeon® processor 5200, 5400, 7400 series, Intel® Core™2 Quad processor Q9000 series, and Intel® Core™2 Extreme processors QX9000, X9000 series, Intel® Core™2 processor E8000 series are based on Enhanced Intel® Core™ microarchitecture.

The Intel® Atom™ processor family is based on the Intel® Atom™ microarchitecture and supports Intel 64 architecture.

The Intel® Core™i7 processor and the Intel® Core™i5 processor are based on the Intel® microarchitecture (Nehalem) and support Intel 64 architecture.
Processors based on the Next Generation Intel Processor, codenamed Westmere, support Intel 64 architecture.

P6 family, Pentium® M, Intel® Core™ Solo, Intel® Core™ Duo processors, dual-core Intel® Xeon® processor LV, and early generations of Pentium 4 and Intel Xeon processors support IA-32 architecture. The Intel® Atom™ processor Z5xx series support IA-32 architecture.

The Intel® Xeon® processor 3000, 3200, 5000, 5100, 5200, 5300, 5400, 7100, 7200, 7300, 7400 series, Intel® Core™2 Duo, Intel® Core™2 Extreme, Intel® Core™2 Quad processors, Pentium® D processors, Pentium® Dual-Core processor, newer generations of Pentium 4 and Intel Xeon processor family support Intel® 64 architecture.

IA-32 architecture is the instruction set architecture and programming environment for Intel's 32-bit microprocessors.

Intel® 64 architecture is the instruction set architecture and programming environment which is the superset of Intel's 32-bit and 64-bit architectures. It is compatible with the IA-32 architecture.

1.2 OVERVIEW OF VOLUME 2A AND 2B: INSTRUCTION SET REFERENCE

A description of Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volumes 2A & 2B, content follows:

Chapter 1 — About This Manual. Gives an overview of all five volumes of the Intel® 64 and IA-32 Architectures Software Developer’s Manual. It also describes the notational conventions in these manuals and lists related Intel® manuals and documentation of interest to programmers and hardware designers.

Chapter 2 — Instruction Format. Describes the machine-level instruction format used for all IA-32 instructions and gives the allowable encodings of prefixes, the operand-identifier byte (ModR/M byte), the addressing-mode specifier byte (SIB byte), and the displacement and immediate bytes.

Chapter 3 — Instruction Set Reference, A-M. Describes Intel 64 and IA-32 instructions in detail, including an algorithmic description of operations, the effect on flags, the effect of operand- and address-size attributes, and the exceptions that may be generated. The instructions are arranged in alphabetical order. General-purpose, x87 FPU, Intel MMX™ technology, SSE/SSE2/SSE3/SSSE3/SSE4 extensions, and system instructions are included.

Chapter 4 — Instruction Set Reference, N-Z. Continues the description of Intel 64 and IA-32 instructions started in Chapter 3. It provides the balance of the alphabetized list of instructions and starts Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B.
ABOUT THIS MANUAL

Chapter 5 — VMX Instruction Reference. Describes the virtual-machine extensions (VMX). VMX is intended for a system executive to support virtualization of processor hardware and a system software layer acting as a host to multiple guest software environments.

Chapter 6— Safer Mode Extensions Reference. Describes the safer mode extensions (SMX). SMX is intended for a system executive to support launching a measured environment in a platform where the identity of the software controlling the platform hardware can be measured for the purpose of making trust decisions.

Appendix A — Opcode Map. Gives an opcode map for the IA-32 instruction set.

Appendix B — Instruction Formats and Encodings. Gives the binary encoding of each form of each IA-32 instruction.

Appendix C — Intel® C/C++ Compiler Intrinsics and Functional Equivalents. Lists the Intel® C/C++ compiler intrinsics and their assembly code equivalents for each of the IA-32 MMX and SSE/SSE2/SSE3 instructions.

1.3 NOTATIONAL CONVENTIONS

This manual uses specific notation for data-structure formats, for symbolic representation of instructions, and for hexadecimal and binary numbers. A review of this notation makes the manual easier to read.

1.3.1 Bit and Byte Order

In illustrations of data structures in memory, smaller addresses appear toward the bottom of the figure; addresses increase toward the top. Bit positions are numbered from right to left. The numerical value of a set bit is equal to two raised to the power of the bit position. IA-32 processors are "little endian" machines; this means the bytes of a word are numbered starting from the least significant byte. Figure 1-1 illustrates these conventions.
1.3.2 Reserved Bits and Software Compatibility

In many register and memory layout descriptions, certain bits are marked as reserved. When bits are marked as reserved, it is essential for compatibility with future processors that software treat these bits as having a future, though unknown, effect. The behavior of reserved bits should be regarded as not only undefined, but unpredictable. Software should follow these guidelines in dealing with reserved bits:

- Do not depend on the states of any reserved bits when testing the values of registers which contain such bits. Mask out the reserved bits before testing.
- Do not depend on the states of any reserved bits when storing to memory or to a register.
- Do not depend on the ability to retain information written into any reserved bits.
- When loading a register, always load the reserved bits with the values indicated in the documentation, if any, or reload them with values previously read from the same register.

**NOTE**

Avoid any software dependence upon the state of reserved bits in IA-32 registers. Depending upon the values of reserved register bits will make software dependent upon the unspecified manner in which the processor handles these bits. Programs that depend upon reserved values risk incompatibility with future processors.
1.3.3 Instruction Operands

When instructions are represented symbolically, a subset of the IA-32 assembly language is used. In this subset, an instruction has the following format:

```
label: mnemonic argument1, argument2, argument3
```

where:

- A **label** is an identifier which is followed by a colon.
- A **mnemonic** is a reserved name for a class of instruction opcodes which have the same function.
- The operands **argument1**, **argument2**, and **argument3** are optional. There may be from zero to three operands, depending on the opcode. When present, they take the form of either literals or identifiers for data items. Operand identifiers are either reserved names of registers or are assumed to be assigned to data items declared in another part of the program (which may not be shown in the example).

When two operands are present in an arithmetic or logical instruction, the right operand is the source and the left operand is the destination.

For example:

```
LOADREG: MOV EAX, SUBTOTAL
```

In this example, LOADREG is a label, MOV is the mnemonic identifier of an opcode, EAX is the destination operand, and SUBTOTAL is the source operand. Some assembly languages put the source and destination in reverse order.

1.3.4 Hexadecimal and Binary Numbers

Base 16 (hexadecimal) numbers are represented by a string of hexadecimal digits followed by the character H (for example, F82EH). A hexadecimal digit is a character from the following set: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F.

Base 2 (binary) numbers are represented by a string of 1s and 0s, sometimes followed by the character B (for example, 1010B). The "B" designation is only used in situations where confusion as to the type of number might arise.

1.3.5 Segmented Addressing

The processor uses byte addressing. This means memory is organized and accessed as a sequence of bytes. Whether one or more bytes are being accessed, a byte address is used to locate the byte or bytes in memory. The range of memory that can be addressed is called an **address space**.

The processor also supports segmented addressing. This is a form of addressing where a program may have many independent address spaces, called **segments**.
For example, a program can keep its code (instructions) and stack in separate segments. Code addresses would always refer to the code space, and stack addresses would always refer to the stack space. The following notation is used to specify a byte address within a segment:

Segment-register:Byte-address

For example, the following segment address identifies the byte at address FF79H in the segment pointed by the DS register:

DS:FF79H

The following segment address identifies an instruction address in the code segment. The CS register points to the code segment and the EIP register contains the address of the instruction.

CS:EIP

### 1.3.6 Exceptions

An exception is an event that typically occurs when an instruction causes an error. For example, an attempt to divide by zero generates an exception. However, some exceptions, such as breakpoints, occur under other conditions. Some types of exceptions may provide error codes. An error code reports additional information about the error. An example of the notation used to show an exception and error code is shown below:

#PF(fault code)

This example refers to a page-fault exception under conditions where an error code naming a type of fault is reported. Under some conditions, exceptions which produce error codes may not be able to report an accurate code. In this case, the error code is zero, as shown below for a general-protection exception:

#GP(0)

### 1.3.7 A New Syntax for CPUID, CR, and MSR Values

Obtain feature flags, status, and system information by using the CPUID instruction, by checking control register bits, and by reading model-specific registers. We are moving toward a new syntax to represent this information. See Figure 1-2.
1.4 RELATED LITERATURE

Literature related to Intel 64 and IA-32 processors is listed on-line at:


Some of the documents listed at this web site can be viewed on-line; others can be
ordered. The literature available is listed by Intel processor and then by the following
literature types: applications notes, data sheets, manuals, papers, and specification updates.

See also:

• The data sheet for a particular Intel 64 or IA-32 processor
• The specification update for a particular Intel 64 or IA-32 processor
• Intel® C++ Compiler documentation and online help
• Intel® Fortran Compiler documentation and online help
• Intel® VTune™ Performance Analyzer documentation and online help
• Intel® 64 and IA-32 Architectures Software Developer’s Manual (in five volumes)
• Intel® 64 and IA-32 Architectures Optimization Reference Manual
• Intel® Processor Identification with the CPUID Instruction, AP-485
  http://www.intel.com/support/processors/sb/cs-009861.htm
• Intel 64 Architecture x2APIC Specification:
• Intel 64 Architecture Processor Topology Enumeration:
  http://softwarecommunity.intel.com/articles/eng/3887.htm
• Intel® Trusted Execution Technology Measured Launched Environment Programming Guide,
• Intel® SSE4 Programming Reference,
• Developing Multi-threaded Applications: A Platform Consistent Approach
  http://cache-wwww.intel.com/cd/00/00/05/15/51534_developing_multithreaded_applications.pdf
• Using Spin-Loops on Intel Pentium 4 Processor and Intel Xeon Processor MP

More relevant links are:

• Software network link:
  http://softwarecommunity.intel.com/isn/home/
• Developer centers:
• Processor support general link:
  http://www.intel.com/support/processors/
ABOUT THIS MANUAL

- Software products and packages:
- Intel 64 and IA-32 processor manuals (printed or PDF downloads):
- Intel® Multi-Core Technology:
- Intel® Hyper-Threading Technology (Intel® HT Technology):
  http://developer.intel.com/technology/hyperthread/
CHAPTER 2
INSTRUCTION FORMAT

This chapter describes the instruction format for all Intel 64 and IA-32 processors. The instruction format for protected mode, real-address mode and virtual-8086 mode is described in Section 2.1. Increments provided for IA-32e mode and its sub-modes are described in Section 2.2.

2.1 INSTRUCTION FORMAT FOR PROTECTED MODE, REAL-ADDRESS MODE, AND VIRTUAL-8086 MODE

The Intel 64 and IA-32 architectures instruction encodings are subsets of the format shown in Figure 2-1. Instructions consist of optional instruction prefixes (in any order), primary opcode bytes (up to three bytes), an addressing-form specifier (if required) consisting of the ModR/M byte and sometimes the SIB (Scale-Index-Base) byte, a displacement (if required), and an immediate data field (if required).

<table>
<thead>
<tr>
<th>Instruction Prefixes</th>
<th>Opcode</th>
<th>ModR/M</th>
<th>SIB</th>
<th>Displacement</th>
<th>Immediate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Up to four prefixes of 1 byte each (optional)</td>
<td>1-, 2-, or 3-byte opcode</td>
<td>1 byte (if required)</td>
<td>1 byte (if required)</td>
<td>Address displacement of 1, 2, or 4 bytes or none</td>
<td>Immediate data of 1, 2, or 4 bytes or none</td>
</tr>
</tbody>
</table>

Figure 2-1. Intel 64 and IA-32 Architectures Instruction Format

2.1.1 Instruction Prefixes

Instruction prefixes are divided into four groups, each with a set of allowable prefix codes. For each instruction, it is only useful to include up to one prefix code from each of the four groups (Groups 1, 2, 3, 4). Groups 1 through 4 may be placed in any order relative to each other.

- Group 1
  - Lock and repeat prefixes:
INSTRUCTION FORMAT

- **LOCK** prefix is encoded using F0H
- **REPNE/REPNZ** prefix is encoded using F2H. Repeat-Not-Zero prefix applies only to string and input/output instructions. (F2H is also used as a mandatory prefix for some instructions)
- **REP or REPE/REPZ** is encoded using F3H. Repeat prefix applies only to string and input/output instructions. (F3H is also used as a mandatory prefix for some instructions)

**Group 2**
- Segment override prefixes:
  - 2EH—CS segment override (use with any branch instruction is reserved)
  - 36H—SS segment override prefix (use with any branch instruction is reserved)
  - 3EH—DS segment override prefix (use with any branch instruction is reserved)
  - 26H—ES segment override prefix (use with any branch instruction is reserved)
  - 64H—FS segment override prefix (use with any branch instruction is reserved)
  - 65H—GS segment override prefix (use with any branch instruction is reserved)
- Branch hints:
  - 2EH—Branch not taken (used only with Jcc instructions)
  - 3EH—Branch taken (used only with Jcc instructions)

**Group 3**
- Operand-size override prefix is encoded using 66H (66H is also used as a mandatory prefix for some instructions).

**Group 4**
- 67H—Address-size override prefix

The **LOCK** prefix (F0H) forces an operation that ensures exclusive use of shared memory in a multiprocessor environment. See “LOCK—Assert LOCK# Signal Prefix” in Chapter 3, “Instruction Set Reference, A-M,” for a description of this prefix.

Repeat prefixes (F2H, F3H) cause an instruction to be repeated for each element of a string. Use these prefixes only with string and I/O instructions (MOV, CMPS, SCAS, LODS, STOS, INS, and OUTS). Use of repeat prefixes and/or undefined opcodes with other Intel 64 or IA-32 instructions is reserved; such use may cause unpredictable behavior.

Some instructions may use F2H,F3H as a mandatory prefix to express distinct functionality. A mandatory prefix generally should be placed after other optional prefixes (exception to this is discussed in Section 2.2.1, "REX Prefixes")
Branch hint prefixes (2EH, 3EH) allow a program to give a hint to the processor about the most likely code path for a branch. Use these prefixes only with conditional branch instructions (Jcc). Other use of branch hint prefixes and/or other undefined opcodes with Intel 64 or IA-32 instructions is reserved; such use may cause unpredictable behavior.

The operand-size override prefix allows a program to switch between 16- and 32-bit operand sizes. Either size can be the default; use of the prefix selects the non-default size.

Some SSE2/SSE3/SSSE3/SSE4 instructions and instructions using a three-byte sequence of primary opcode bytes may use 66H as a mandatory prefix to express distinct functionality. A mandatory prefix generally should be placed after other optional prefixes (exception to this is discussed in Section 2.2.1, “REX Prefixes”)

Other use of the 66H prefix is reserved; such use may cause unpredictable behavior.

The address-size override prefix (67H) allows programs to switch between 16- and 32-bit addressing. Either size can be the default; the prefix selects the non-default size. Using this prefix and/or other undefined opcodes when operands for the instruction do not reside in memory is reserved; such use may cause unpredictable behavior.

2.1.2 Opcodes

A primary opcode can be 1, 2, or 3 bytes in length. An additional 3-bit opcode field is sometimes encoded in the ModR/M byte. Smaller fields can be defined within the primary opcode. Such fields define the direction of operation, size of displacements, register encoding, condition codes, or sign extension. Encoding fields used by an opcode vary depending on the class of operation.

Two-byte opcode formats for general-purpose and SIMD instructions consist of:

• An escape opcode byte 0FH as the primary opcode and a second opcode byte, or
• A mandatory prefix (66H, F2H, or F3H), an escape opcode byte, and a second opcode byte (same as previous bullet)

For example, CVTDQ2PD consists of the following sequence: F3 0F E6. The first byte is a mandatory prefix (it is not considered as a repeat prefix).

Three-byte opcode formats for general-purpose and SIMD instructions consist of:

• An escape opcode byte 0FH as the primary opcode, plus two additional opcode bytes, or
• A mandatory prefix (66H, F2H, or F3H), an escape opcode byte, plus two additional opcode bytes (same as previous bullet)

For example, PHADDW for XMM registers consists of the following sequence: 66 0F 38 01. The first byte is the mandatory prefix.

Valid opcode expressions are defined in Appendix A and Appendix B.
2.1.3 ModR/M and SIB Bytes

Many instructions that refer to an operand in memory have an addressing-form specifier byte (called the ModR/M byte) following the primary opcode. The ModR/M byte contains three fields of information:
- The *mod* field combines with the *r/m* field to form 32 possible values: eight registers and 24 addressing modes.
- The *reg(opcode)* field specifies either a register number or three more bits of opcode information. The purpose of the *reg(opcode)* field is specified in the primary opcode.
- The *r/m* field can specify a register as an operand or it can be combined with the *mod* field to encode an addressing mode. Sometimes, certain combinations of the *mod* field and the *r/m* field is used to express opcode information for some instructions.

Certain encodings of the ModR/M byte require a second addressing byte (the SIB byte). The base-plus-index and scale-plus-index forms of 32-bit addressing require the SIB byte. The SIB byte includes the following fields:
- The *scale* field specifies the scale factor.
- The *index* field specifies the register number of the index register.
- The *base* field specifies the register number of the base register.

See Section 2.1.5 for the encodings of the ModR/M and SIB bytes.

2.1.4 Displacement and Immediate Bytes

Some addressing forms include a displacement immediately following the ModR/M byte (or the SIB byte if one is present). If a displacement is required; it be 1, 2, or 4 bytes.

If an instruction specifies an immediate operand, the operand always follows any displacement bytes. An immediate operand can be 1, 2 or 4 bytes.

2.1.5 Addressing-Mode Encoding of ModR/M and SIB Bytes

The values and corresponding addressing forms of the ModR/M and SIB bytes are shown in Table 2-1 through Table 2-3: 16-bit addressing forms specified by the ModR/M byte are in Table 2-1 and 32-bit addressing forms are in Table 2-2. Table 2-3 shows 32-bit addressing forms specified by the SIB byte. In cases where the *reg(opcode)* field in the ModR/M byte represents an extended opcode, valid encodings are shown in Appendix B.

In Table 2-1 and Table 2-2, the Effective Address column lists 32 effective addresses that can be assigned to the first operand of an instruction by using the Mod and R/M fields of the ModR/M byte. The first 24 options provide ways of specifying a memory
location; the last eight (Mod = 11B) provide ways of specifying general-purpose, MMX technology and XMM registers.

The Mod and R/M columns in Table 2-1 and Table 2-2 give the binary encodings of the Mod and R/M fields required to obtain the effective address listed in the first column. For example: see the row indicated by Mod = 11B, R/M = 000B. The row identifies the general-purpose registers EAX, AX or AL; MMX technology register MM0; or XMM register XMM0. The register used is determined by the opcode byte and the operand-size attribute.

Now look at the seventh row in either table (labeled “REG =”). This row specifies the use of the 3-bit Reg/Opcode field when the field is used to give the location of a second operand. The second operand must be a general-purpose, MMX technology, or XMM register. Rows one through five list the registers that may correspond to the value in the table. Again, the register used is determined by the opcode byte along with the operand-size attribute.

If the instruction does not require a second operand, then the Reg/Opcode field may be used as an opcode extension. This use is represented by the sixth row in the tables (labeled “/digit (Opcode)”). Note that values in row six are represented in decimal form.

The body of Table 2-1 and Table 2-2 (under the label “Value of ModR/M Byte (in Hexadecimal)”) contains a 32 by 8 array that presents all of 256 values of the ModR/M byte (in hexadecimal). Bits 3, 4 and 5 are specified by the column of the table in which a byte resides. The row specifies bits 0, 1 and 2; and bits 6 and 7. The figure below demonstrates interpretation of one table value.

<table>
<thead>
<tr>
<th>Mod</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>00</td>
</tr>
<tr>
<td>REG</td>
<td>001</td>
</tr>
<tr>
<td>C8H</td>
<td>11001000</td>
</tr>
</tbody>
</table>

**Figure 2-2. Table Interpretation of ModR/M Byte (C8H)**
INSTRUCTION FORMAT

Table 2-1. 16-Bit Addressing Forms with the ModR/M Byte

<table>
<thead>
<tr>
<th>Effective Address</th>
<th>Mod R/M</th>
<th>Value of ModR/M Byte (in Hexadecimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[BX+S]</td>
<td>00 00 00</td>
<td>00 08 10 18 20 28 30 38</td>
</tr>
<tr>
<td>[BX+DI]</td>
<td>00 01 01 09 11 19 21 29</td>
<td></td>
</tr>
<tr>
<td>[BP+S]</td>
<td>01 02 02 0A 12 1A 22 2A</td>
<td></td>
</tr>
<tr>
<td>[BP+DI]</td>
<td>01 03 03 0B 13 1B 23 2B</td>
<td></td>
</tr>
<tr>
<td>[SI]</td>
<td>10 04 04 0C 14 1C 24 2C</td>
<td></td>
</tr>
<tr>
<td>[DI]</td>
<td>10 05 05 0D 15 1D 25 2D</td>
<td></td>
</tr>
<tr>
<td>disp16</td>
<td>11 06 0E 16 1F 26 2E 36</td>
<td></td>
</tr>
<tr>
<td>[BX]</td>
<td>11 07 0F 17 1F 27 2F 37</td>
<td></td>
</tr>
<tr>
<td>[BX+S]+disp8</td>
<td>01 00 00 40 48 50 58 60 68 70 78</td>
<td></td>
</tr>
<tr>
<td>[BX+DI]+disp8</td>
<td>00 01 41 49 51 59 61 69 71 79</td>
<td></td>
</tr>
<tr>
<td>[BP+S]+disp8</td>
<td>01 02 42 4A 52 5A 62 6A 72 7A</td>
<td></td>
</tr>
<tr>
<td>[BP+DI]+disp8</td>
<td>01 03 43 4B 53 5B 63 6B 73 7B</td>
<td></td>
</tr>
<tr>
<td>[SI]+disp8</td>
<td>10 04 44 4C 54 5C 64 6C 74 7C</td>
<td></td>
</tr>
<tr>
<td>[DI]+disp8</td>
<td>10 05 45 4D 55 5D 65 6D 75 7D</td>
<td></td>
</tr>
<tr>
<td>[BP]+disp8</td>
<td>11 06 46 4E 56 5E 66 6E 76 7E</td>
<td></td>
</tr>
<tr>
<td>[BX]+disp8</td>
<td>11 07 4F 57 5F 67 6F 77 7F</td>
<td></td>
</tr>
<tr>
<td>[BX+S]+disp16</td>
<td>10 00 00 80 88 90 98 9A 9B 9C 9D 9E 9F</td>
<td></td>
</tr>
<tr>
<td>[BX+DI]+disp16</td>
<td>00 01 81 89 91 99 9A 9B 9C 9D 9E 9F</td>
<td></td>
</tr>
<tr>
<td>[BP+S]+disp16</td>
<td>01 02 82 8A 92 9A 9B 9C 9D 9E 9F 9G</td>
<td></td>
</tr>
<tr>
<td>[BP+DI]+disp16</td>
<td>01 03 83 8B 93 9B 9A 9B 9C 9D 9E 9F</td>
<td></td>
</tr>
<tr>
<td>[SI]+disp16</td>
<td>10 04 84 8C 94 9C 9A 9B 9C 9D 9E 9F</td>
<td></td>
</tr>
<tr>
<td>[DI]+disp16</td>
<td>10 05 85 8D 95 9D 9A 9B 9C 9D 9E 9F</td>
<td></td>
</tr>
<tr>
<td>[BP]+disp16</td>
<td>11 06 86 8E 96 9E 9A 9B 9C 9D 9E 9F</td>
<td></td>
</tr>
<tr>
<td>[BX]+disp16</td>
<td>11 07 8F 97 9F 97 9A 9B 9C 9D 9E 9F</td>
<td></td>
</tr>
<tr>
<td>EAX/AX/AL/MM0/XMM0</td>
<td>11 00 00</td>
<td>00 00 00 00 00 00 00 00 00 00 00 00</td>
</tr>
<tr>
<td>ECX/CL/MM1/XMM1</td>
<td>00 01 01</td>
<td>01 01 01 01 01 01 01 01 01 01 01 01</td>
</tr>
<tr>
<td>EDX/DM/MM2/XMM2</td>
<td>01 02 02</td>
<td>02 02 02 02 02 02 02 02 02 02 02 02</td>
</tr>
<tr>
<td>EBX/BL/MM3/XMM3</td>
<td>02 03 03</td>
<td>03 03 03 03 03 03 03 03 03 03 03 03</td>
</tr>
<tr>
<td>ESP/SP/XMM4/XMM4</td>
<td>03 04 04</td>
<td>04 04 04 04 04 04 04 04 04 04 04 04</td>
</tr>
<tr>
<td>EBP/BP/XMM5/XMM5</td>
<td>04 05 05</td>
<td>05 05 05 05 05 05 05 05 05 05 05 05</td>
</tr>
<tr>
<td>ESI/SI/DH/MM6/XMM6</td>
<td>05 06 06</td>
<td>06 06 06 06 06 06 06 06 06 06 06 06</td>
</tr>
<tr>
<td>EDI/DI/BH/MM7/XMM7</td>
<td>06 07 07</td>
<td>07 07 07 07 07 07 07 07 07 07 07 07</td>
</tr>
</tbody>
</table>

NOTES:
1. The default segment register is SS for the effective addresses containing a BP index, DS for other effective addresses.
2. The disp16 nomenclature denotes a 16-bit displacement that follows the ModR/M byte and that is added to the index.
3. The disp8 nomenclature denotes an 8-bit displacement that follows the ModR/M byte and that is sign-extended and added to the index.
Table 2-2. 32-Bit Addressing Forms with the ModR/M Byte

INSTRUCTION FORMAT

<table>
<thead>
<tr>
<th>Effective Address</th>
<th>Mod</th>
<th>R/M</th>
<th>Value of ModR/M Byte (in Hexadecimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(EAX)</td>
<td>00</td>
<td>00</td>
<td>00 00 00 08 10 18 20 28 30 38</td>
</tr>
<tr>
<td>(ECX)</td>
<td>00</td>
<td>01</td>
<td>01 01 09 11 19 21 29 31 39</td>
</tr>
<tr>
<td>(EDX)</td>
<td>01</td>
<td>02</td>
<td>02 02 0A 12 1A 22 2A 32 3A</td>
</tr>
<tr>
<td>(EBX)</td>
<td>02</td>
<td>03</td>
<td>03 03 0B 13 1B 23 2B 33 3B</td>
</tr>
<tr>
<td>disp32</td>
<td>10</td>
<td>04</td>
<td>04 04 0C 14 1C 24 2C 34 3C</td>
</tr>
<tr>
<td>(ESI)</td>
<td>11</td>
<td>06</td>
<td>06 06 0E 16 1E 26 2E 36 3E</td>
</tr>
<tr>
<td>(EDI)</td>
<td>11</td>
<td>07</td>
<td>07 07 0F 17 1F 27 2F 37 3F</td>
</tr>
<tr>
<td>(EAX)-disp8</td>
<td>01</td>
<td>00</td>
<td>00 00 40 48 50 58 60 68 70 78</td>
</tr>
<tr>
<td>(ECX)-disp8</td>
<td>00</td>
<td>01</td>
<td>01 01 41 49 51 59 61 69 71 79</td>
</tr>
<tr>
<td>(EDX)-disp8</td>
<td>02</td>
<td>03</td>
<td>02 02 42 4A 52 5A 62 6A 72 7A</td>
</tr>
<tr>
<td>(EBX)-disp8</td>
<td>03</td>
<td>04</td>
<td>03 04 43 4B 54 5B 63 6B 73 7B</td>
</tr>
<tr>
<td>disp32</td>
<td>04</td>
<td>04</td>
<td>04 04 44 4C 54 5C 64 6C 74 7C</td>
</tr>
<tr>
<td>(ESI)-disp8</td>
<td>05</td>
<td>06</td>
<td>06 06 45 4D 55 5D 65 6D 75 7D</td>
</tr>
<tr>
<td>(EDI)-disp8</td>
<td>07</td>
<td>07</td>
<td>07 07 46 4E 56 5E 66 6E 76 7E</td>
</tr>
<tr>
<td>disp32</td>
<td>08</td>
<td>08</td>
<td>08 08 47 4F 57 5F 67 6F 77 7F</td>
</tr>
<tr>
<td>disp32</td>
<td>10</td>
<td>00</td>
<td>00 00 80 88 90 98 A0 A8 B0 B8</td>
</tr>
<tr>
<td>disp32</td>
<td>11</td>
<td>01</td>
<td>01 01 81 89 91 99 A1 A9 B1 B9</td>
</tr>
<tr>
<td>disp32</td>
<td>02</td>
<td>02</td>
<td>02 02 82 8A 92 9A A2 AA B2 BA</td>
</tr>
<tr>
<td>disp32</td>
<td>03</td>
<td>03</td>
<td>03 03 83 8B 93 9B A3 AB B3 BB</td>
</tr>
<tr>
<td>disp32</td>
<td>10</td>
<td>04</td>
<td>04 04 84 8C 94 9C A4 AC B4 BC</td>
</tr>
<tr>
<td>disp32</td>
<td>11</td>
<td>05</td>
<td>05 05 85 8D 95 9D A5 AD B5 BD</td>
</tr>
<tr>
<td>disp32</td>
<td>00</td>
<td>06</td>
<td>06 06 86 8E 96 9E A6 AE B6 BE</td>
</tr>
<tr>
<td>disp32</td>
<td>01</td>
<td>07</td>
<td>07 07 87 8F 97 9F A7 AF B7 BF</td>
</tr>
</tbody>
</table>

NOTES:

1. The [−][−] nomenclature means a SIB follows the ModR/M byte.
2. The disp32 nomenclature denotes a 32-bit displacement that follows the ModR/M byte (or the SIB byte if one is present) and that is added to the index.
3. The disp8 nomenclature denotes an 8-bit displacement that follows the ModR/M byte (or the SIB byte if one is present) and that is sign-extended and added to the index.

Table 2-3 is organized to give 256 possible values of the SIB byte (in hexadecimal). General purpose registers used as a base are indicated across the top of the table, along with corresponding values for the SIB byte’s base field. Table rows in the body
INSTRUCTION FORMAT

of the table indicate the register used as the index (SIB byte bits 3, 4 and 5) and the scaling factor (determined by SIB byte bits 6 and 7).

### Table 2-3. 32-Bit Addressing Forms with the SIB Byte

<table>
<thead>
<tr>
<th>Scaled Index</th>
<th>SS</th>
<th>Index</th>
<th>Value of SIB Byte (in Hexadecimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EAX</td>
<td>00</td>
<td>00</td>
<td>00 01 02 03 04 05 06 07</td>
</tr>
<tr>
<td>ECX</td>
<td>00</td>
<td>08</td>
<td>0A 0B OC 0D 0E 0F</td>
</tr>
<tr>
<td>EDX</td>
<td>01</td>
<td>11</td>
<td>12 13 14 15 16 17</td>
</tr>
<tr>
<td>EBX</td>
<td>01</td>
<td>18</td>
<td>1A 1B 1C 1D 1E 1F</td>
</tr>
<tr>
<td>none</td>
<td>100</td>
<td>20</td>
<td>21 22 23 24 25 26 27</td>
</tr>
<tr>
<td>[ESI]</td>
<td>110</td>
<td>30</td>
<td>31 32 33 34 35 36 37</td>
</tr>
<tr>
<td>[EDI]</td>
<td>111</td>
<td>38</td>
<td>39 3A 3B 3C 3D 3E 3F</td>
</tr>
<tr>
<td>[EAX*2]</td>
<td>01</td>
<td>40</td>
<td>41 42 43 44 45 46 47</td>
</tr>
<tr>
<td>[ECX*2]</td>
<td>01</td>
<td>48</td>
<td>49 4A 4B 4C 4D 4E 4F</td>
</tr>
<tr>
<td>[EDX*2]</td>
<td>01</td>
<td>50</td>
<td>51 52 53 54 55 56 57</td>
</tr>
<tr>
<td>[EBX*2]</td>
<td>01</td>
<td>58</td>
<td>59 5A 5B 5C 5D 5E 5F</td>
</tr>
<tr>
<td>none</td>
<td>100</td>
<td>60</td>
<td>61 62 63 64 65 66 67</td>
</tr>
<tr>
<td>[EBP*2]</td>
<td>101</td>
<td>68</td>
<td>69 6A 6B 6C 6D 6E 6F</td>
</tr>
<tr>
<td>[ESI*2]</td>
<td>110</td>
<td>70</td>
<td>71 72 73 74 75 76 77</td>
</tr>
<tr>
<td>[EDI*2]</td>
<td>111</td>
<td>78</td>
<td>79 7A 7B 7C 7D 7E 7F</td>
</tr>
<tr>
<td>[EAX*4]</td>
<td>10</td>
<td>80</td>
<td>81 82 83 84 85 86 87</td>
</tr>
<tr>
<td>[ECX*4]</td>
<td>01</td>
<td>88</td>
<td>89 8A 8B 8C 8D 8E 8F</td>
</tr>
<tr>
<td>[EDX*4]</td>
<td>01</td>
<td>90</td>
<td>91 92 93 94 95 96 97</td>
</tr>
<tr>
<td>[EBX*4]</td>
<td>01</td>
<td>98</td>
<td>99 9A 9B 9C 9D 9E 9F</td>
</tr>
<tr>
<td>none</td>
<td>100</td>
<td>A0</td>
<td>A1 A2 A3 A4 A5 A6 A7</td>
</tr>
<tr>
<td>[EBP*4]</td>
<td>101</td>
<td>A8</td>
<td>A9 AA AB AC AD AE AF</td>
</tr>
<tr>
<td>[ESI*4]</td>
<td>110</td>
<td>B0</td>
<td>B1 B2 B3 B4 B5 B6 B7</td>
</tr>
<tr>
<td>[EDI*4]</td>
<td>111</td>
<td>B8</td>
<td>B9 BA BB BC BD BE BF</td>
</tr>
<tr>
<td>[EAX*8]</td>
<td>11</td>
<td>C0</td>
<td>C1 C2 C3 C4 C5 C6 C7</td>
</tr>
<tr>
<td>[ECX*8]</td>
<td>01</td>
<td>C8</td>
<td>C9 CA CB CC CD CF CF</td>
</tr>
<tr>
<td>[EDX*8]</td>
<td>01</td>
<td>D0</td>
<td>D1 D2 D3 D4 D5 D6 D7</td>
</tr>
<tr>
<td>[EBX*8]</td>
<td>01</td>
<td>D8</td>
<td>DA DB DC DD DE DF</td>
</tr>
<tr>
<td>none</td>
<td>100</td>
<td>E0</td>
<td>E1 E2 E3 E4 E5 E6 E7</td>
</tr>
<tr>
<td>[EBP*8]</td>
<td>101</td>
<td>E8</td>
<td>EE EB EC ED EE EF</td>
</tr>
<tr>
<td>[ESI*8]</td>
<td>110</td>
<td>F0</td>
<td>F1 F2 F3 F4 F5 F6 F7</td>
</tr>
<tr>
<td>[EDI*8]</td>
<td>111</td>
<td>F8</td>
<td>FA FB FC FD FE FF</td>
</tr>
</tbody>
</table>

#### NOTES:

1. The [*] nomenclature means a disp32 with no base if the MOD is 00B. Otherwise, [*] means disp8 or disp32 + [EBP]. This provides the following address modes:

<table>
<thead>
<tr>
<th>MOD bits</th>
<th>Effective Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>[scaled index] + disp32</td>
</tr>
<tr>
<td>01</td>
<td>[scaled index] + disp8 + [EBP]</td>
</tr>
<tr>
<td>10</td>
<td>[scaled index] + disp32 + [EBP]</td>
</tr>
</tbody>
</table>
2.2 IA-32E MODE

IA-32e mode has two sub-modes. These are:

- **Compatibility Mode.** Enables a 64-bit operating system to run most legacy protected mode software unmodified.
- **64-Bit Mode.** Enables a 64-bit operating system to run applications written to access 64-bit address space.

2.2.1 REX Prefixes

REX prefixes are instruction-prefix bytes used in 64-bit mode. They do the following:

- Specify GPRs and SSE registers.
- Specify 64-bit operand size.
- Specify extended control registers.

Not all instructions require a REX prefix in 64-bit mode. A prefix is necessary only if an instruction references one of the extended registers or uses a 64-bit operand. If a REX prefix is used when it has no meaning, it is ignored.

Only one REX prefix is allowed per instruction. If used, the REX prefix byte must immediately precede the opcode byte or the escape opcode byte (0FH). When a REX prefix is used in conjunction with an instruction containing a mandatory prefix, the mandatory prefix must come before the REX so the REX prefix can be immediately preceding the opcode or the escape byte. For example, CVTDQ2PD with a REX prefix should have REX placed between F3 and 0F E6. Other placements are ignored. The instruction-size limit of 15 bytes still applies to instructions with a REX prefix. See Figure 2-3.

<table>
<thead>
<tr>
<th>Legacy Prefixes</th>
<th>REX Prefix</th>
<th>Opcode</th>
<th>ModR/M</th>
<th>SIB</th>
<th>Displacement</th>
<th>Immediate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grp 1, Grp 2, Grp 3, Grp 4 (optional)</td>
<td>(optional)</td>
<td>1-, 2-, or 3-byte opcode</td>
<td>1 byte (if required)</td>
<td>1 byte (if required)</td>
<td>Address displacement of 1, 2, or 4 bytes</td>
<td>Immediate data of 1, 2, or 4 bytes or none</td>
</tr>
</tbody>
</table>

**Figure 2-3. Prefix Ordering in 64-bit Mode**
INSTRUCTION FORMAT

2.2.1.1 Encoding
Intel 64 and IA-32 instruction formats specify up to three registers by using 3-bit fields in the encoding, depending on the format:

- ModR/M: the reg and r/m fields of the ModR/M byte
- ModR/M with SIB: the reg field of the ModR/M byte, the base and index fields of the SIB (scale, index, base) byte
- Instructions without ModR/M: the reg field of the opcode

In 64-bit mode, these formats do not change. Bits needed to define fields in the 64-bit context are provided by the addition of REX prefixes.

2.2.1.2 More on REX Prefix Fields
REX prefixes are a set of 16 opcodes that span one row of the opcode map and occupy entries 40H to 4FH. These opcodes represent valid instructions (INC or DEC) in IA-32 operating modes and in compatibility mode. In 64-bit mode, the same opcodes represent the instruction prefix REX and are not treated as individual instructions.

The single-byte-opcode form of INC/DEC instruction not available in 64-bit mode. INC/DEC functionality is still available using ModR/M forms of the same instructions (opcodes FF/0 and FF/1).

See Table 2-4 for a summary of the REX prefix format. Figure 2-4 though Figure 2-7 show examples of REX prefix fields in use. Some combinations of REX prefix fields are invalid. In such cases, the prefix is ignored. Some additional information follows:

- Setting REX.W can be used to determine the operand size but does not solely determine operand width. Like the 66H size prefix, 64-bit operand size override has no effect on byte-specific operations.
- For non-byte operations: if a 66H prefix is used with prefix (REX.W = 1), 66H is ignored.
- If a 66H override is used with REX and REX.W = 0, the operand size is 16 bits.
- REX.R modifies the ModR/M reg field when that field encodes a GPR, SSE, control or debug register. REX.R is ignored when ModR/M specifies other registers or defines an extended opcode.
- REX.X bit modifies the SIB index field.
- REX.B either modifies the base in the ModR/M r/m field or SIB base field; or it modifies the opcode reg field used for accessing GPRs.
Table 2-4. REX Prefix Fields [BITS: 0100WRXB]

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bit Position</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>7:4</td>
<td>0100</td>
</tr>
<tr>
<td>W</td>
<td>3</td>
<td>0 = Operand size determined by CS.D</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = 64 Bit Operand Size</td>
</tr>
<tr>
<td>R</td>
<td>2</td>
<td>Extension of the ModR/M reg field</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>Extension of the SIB index field</td>
</tr>
<tr>
<td>B</td>
<td>0</td>
<td>Extension of the ModR/M r/m field, SIB base field, or Opcode reg field</td>
</tr>
</tbody>
</table>

![Figure 2-4. Memory Addressing Without an SIB Byte; REX.X Not Used](OM17X8g1-3)

![Figure 2-5. Register-Register Addressing (No Memory Operand); REX.X Not Used](OM17X8g1-4)
In the IA-32 architecture, byte registers (AH, AL, BH, BL, CH, CL, DH, and DL) are encoded in the ModR/M byte’s reg field, the r/m field or the opcode reg field as registers 0 through 7. REX prefixes provide an additional addressing capability for byte-registers that makes the least-significant byte of GPRs available for byte operations.

Certain combinations of the fields of the ModR/M byte and the SIB byte have special meaning for register encodings. For some combinations, fields expanded by the REX prefix are not decoded. Table 2-5 describes how each case behaves.
2.2.1.3 Displacement

Addressing in 64-bit mode uses existing 32-bit ModR/M and SIB encodings. The ModR/M and SIB displacement sizes do not change. They remain 8 bits or 32 bits and are sign-extended to 64 bits.

2.2.1.4 Direct Memory-Offset MOVs

In 64-bit mode, direct memory-offset forms of the MOV instruction are extended to specify a 64-bit immediate absolute address. This address is called a moffset. No prefix is needed to specify this 64-bit memory offset. For these MOV instructions, the
INSTRUCTION FORMAT

size of the memory offset follows the address-size default (64 bits in 64-bit mode). See Table 2-6.

Table 2-6. Direct Memory Offset Form of MOV

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>MOV AL, moffset</td>
</tr>
<tr>
<td>A1</td>
<td>MOV EAX, moffset</td>
</tr>
<tr>
<td>A2</td>
<td>MOV moffset, AL</td>
</tr>
<tr>
<td>A3</td>
<td>MOV moffset, EAX</td>
</tr>
</tbody>
</table>

2.2.1.5  Immediates

In 64-bit mode, the typical size of immediate operands remains 32 bits. When the operand size is 64 bits, the processor sign-extends all immediates to 64 bits prior to their use.

Support for 64-bit immediate operands is accomplished by expanding the semantics of the existing move (MOV reg, imm16/32) instructions. These instructions (opcodes B8H – BFH) move 16-bits or 32-bits of immediate data (depending on the effective operand size) into a GPR. When the effective operand size is 64 bits, these instructions can be used to load an immediate into a GPR. A REX prefix is needed to override the 32-bit default operand size to a 64-bit operand size.

For example:

48 B8 8877665544332211 MOV RAX,1122334455667788H

2.2.1.6  RIP-Relative Addressing

A new addressing form, RIP-relative (relative instruction-pointer) addressing, is implemented in 64-bit mode. An effective address is formed by adding displacement to the 64-bit RIP of the next instruction.

In IA-32 architecture and compatibility mode, addressing relative to the instruction pointer is available only with control-transfer instructions. In 64-bit mode, instructions that use ModR/M addressing can use RIP-relative addressing. Without RIP-relative addressing, all ModR/M instruction modes address memory relative to zero.

RIP-relative addressing allows specific ModR/M modes to address memory relative to the 64-bit RIP using a signed 32-bit displacement. This provides an offset range of ±2GB from the RIP. Table 2-7 shows the ModR/M and SIB encodings for RIP-relative addressing. Redundant forms of 32-bit displacement-addressing exist in the current ModR/M and SIB encodings. There is one ModR/M encoding and there are several SIB encodings. RIP-relative addressing is encoded using a redundant form.

In 64-bit mode, the ModR/M Disp32 (32-bit displacement) encoding is re-defined to be RIP+Disp32 rather than displacement-only. See Table 2-7.
The ModR/M encoding for RIP-relative addressing does not depend on using prefix. Specifically, the r/m bit field encoding of 101B (used to select RIP-relative addressing) is not affected by the REX prefix. For example, selecting R13 (REX.B = 1, r/m = 101B) with mod = 00B still results in RIP-relative addressing. The 4-bit r/m field of REX.B combined with ModR/M is not fully decoded. In order to address R13 with no displacement, software must encode R13 + 0 using a 1-byte displacement of zero.

RIP-relative addressing is enabled by 64-bit mode, not by a 64-bit address-size. The use of the address-size prefix does not disable RIP-relative addressing. The effect of the address-size prefix is to truncate and zero-extend the computed effective address to 32 bits.

### 2.2.1.7 Default 64-Bit Operand Size

In 64-bit mode, two groups of instructions have a default operand size of 64 bits (do not need a REX prefix for this operand size). These are:

- Near branches
- All instructions, except far branches, that implicitly reference the RSP

### 2.2.2 Additional Encodings for Control and Debug Registers

In 64-bit mode, more encodings for control and debug registers are available. The REX.R bit is used to modify the ModR/M reg field when that field encodes a control or debug register (see Table 2-4). These encodings enable the processor to address CR8-CR15 and DR8-DR15. An additional control register (CR8) is defined in 64-bit mode. CR8 becomes the Task Priority Register (TPR).

In the first implementation of IA-32e mode, CR9-CR15 and DR8-DR15 are not implemented. Any attempt to access unimplemented registers results in an invalid-opcode exception (#UD).
CHAPTER 3
INSTRUCTION SET REFERENCE, A-M

This chapter describes the instruction set for the Intel 64 and IA-32 architectures (A-M) in IA-32e, protected, Virtual-8086, and real modes of operation. The set includes general-purpose, x87 FPU, MMX, SSE/SSE2/SSE3/SSSE3/SSE4, and system instructions. See also Chapter 4, "Instruction Set Reference, N-Z," in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B.

For each instruction, each operand combination is described. A description of the instruction and its operand, an operational description, a description of the effect of the instructions on flags in the EFLAGS register, and a summary of exceptions that can be generated are also provided.

3.1 INTERPRETING THE INSTRUCTION REFERENCE PAGES

This section describes the format of information contained in the instruction reference pages in this chapter. It explains notational conventions and abbreviations used in these sections.

3.1.1 Instruction Format

The following is an example of the format used for each instruction description in this chapter. The heading below introduces the example. The table below provides an example summary table.

CMC—Complement Carry Flag [this is an example]

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F5</td>
<td>CMC</td>
<td>Valid</td>
<td>Valid</td>
<td>Complement carry flag.</td>
</tr>
</tbody>
</table>
3.1.1.1 Opcode Column in the Instruction Summary Table

The “Opcode” column in the table above shows the object code produced for each form of the instruction. When possible, codes are given as hexadecimal bytes in the same order in which they appear in memory. Definitions of entries other than hexadecimal bytes are as follows:

- **REX.W** — Indicates the use of a REX prefix that affects operand size or instruction semantics. The ordering of the REX prefix and other optional/mandatory instruction prefixes are discussed Chapter 2. Note that REX prefixes that promote legacy instructions to 64-bit behavior are not listed explicitly in the opcode column.

- **/digit** — A digit between 0 and 7 indicates that the ModR/M byte of the instruction uses only the r/m (register or memory) operand. The reg field contains the digit that provides an extension to the instruction's opcode.

- **/r** — Indicates that the ModR/M byte of the instruction contains a register operand and an r/m operand.

- **cb, cw, cd, cp, co, ct** — A 1-byte (cb), 2-byte (cw), 4-byte (cd), 6-byte (cp), 8-byte (co) or 10-byte (ct) value following the opcode. This value is used to specify a code offset and possibly a new value for the code segment register.

- **ib, iw, id, io** — A 1-byte (ib), 2-byte (iw), 4-byte (id) or 8-byte (io) immediate operand to the instruction that follows the opcode, ModR/M bytes or scale-indexing bytes. The opcode determines if the operand is a signed value. All words, doublewords and quadwords are given with the low-order byte first.

- **+rb, +rw, +rd, +ro** — A register code, from 0 through 7, added to the hexadecimal byte given at the left of the plus sign to form a single opcode byte. See Table 3-1 for the codes. The +ro columns in the table are applicable only in 64-bit mode.

- **+i** — A number used in floating-point instructions when one of the operands is ST(i) from the FPU register stack. The number i (which can range from 0 to 7) is added to the hexadecimal byte given at the left of the plus sign to form a single opcode byte.

<table>
<thead>
<tr>
<th>Table 3-1. Register Codes Associated With +rb, +rw, +rd, +ro</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>Register</td>
</tr>
<tr>
<td>AL</td>
</tr>
<tr>
<td>CL</td>
</tr>
<tr>
<td>DL</td>
</tr>
</tbody>
</table>
3.1.1.2 Instruction Column in the Opcode Summary Table

The “Instruction” column gives the syntax of the instruction statement as it would appear in an ASM386 program. The following is a list of the symbols used to represent operands in the instruction statements:

- **rel8** — A relative address in the range from 128 bytes before the end of the instruction to 127 bytes after the end of the instruction.
- **rel16, rel32, rel64** — A relative address within the same code segment as the instruction assembled. The rel16 symbol applies to instructions with an operand-size attribute of 16 bits; the rel32 symbol applies to instructions with an operand-size attribute of 32 bits; the rel64 symbol applies to instructions with an operand-size attribute of 64 bits.

### Table 3-1. Register Codes Associated With +rb, +rw, +rd, +ro (Contd.)

<table>
<thead>
<tr>
<th>byte register</th>
<th>word register</th>
<th>dword register</th>
<th>quadword register (64-Bit Mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register</td>
<td>REX.B</td>
<td>Reg Field</td>
<td>Register</td>
</tr>
<tr>
<td>BL</td>
<td>None</td>
<td>3</td>
<td>BX</td>
</tr>
<tr>
<td>AH</td>
<td>Not</td>
<td>4</td>
<td>SP</td>
</tr>
<tr>
<td>CH</td>
<td>N.E.</td>
<td>5</td>
<td>BP</td>
</tr>
<tr>
<td>DH</td>
<td>N.E.</td>
<td>6</td>
<td>SI</td>
</tr>
<tr>
<td>BH</td>
<td>N.E.</td>
<td>7</td>
<td>DI</td>
</tr>
<tr>
<td>SPL</td>
<td>Yes</td>
<td>4</td>
<td>SP</td>
</tr>
<tr>
<td>BPL</td>
<td>Yes</td>
<td>5</td>
<td>BP</td>
</tr>
<tr>
<td>SIL</td>
<td>Yes</td>
<td>6</td>
<td>SI</td>
</tr>
<tr>
<td>DIL</td>
<td>Yes</td>
<td>7</td>
<td>DI</td>
</tr>
<tr>
<td>Registers R8 - R15 (see below): Available in 64-Bit Mode Only</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R8L</td>
<td>Yes</td>
<td>0</td>
<td>R8W</td>
</tr>
<tr>
<td>R9L</td>
<td>Yes</td>
<td>1</td>
<td>R9W</td>
</tr>
<tr>
<td>R10L</td>
<td>Yes</td>
<td>2</td>
<td>R10W</td>
</tr>
<tr>
<td>R11L</td>
<td>Yes</td>
<td>3</td>
<td>R11W</td>
</tr>
<tr>
<td>R12L</td>
<td>Yes</td>
<td>4</td>
<td>R12W</td>
</tr>
<tr>
<td>R13L</td>
<td>Yes</td>
<td>5</td>
<td>R13W</td>
</tr>
<tr>
<td>R14L</td>
<td>Yes</td>
<td>6</td>
<td>R14W</td>
</tr>
<tr>
<td>R15L</td>
<td>Yes</td>
<td>7</td>
<td>R15W</td>
</tr>
</tbody>
</table>
• **ptr16:16, ptr16:32 and ptr16:64** — A far pointer, typically to a code segment different from that of the instruction. The notation 16:16 indicates that the value of the pointer has two parts. The value to the left of the colon is a 16-bit selector or value destined for the code segment register. The value to the right corresponds to the offset within the destination segment. The ptr16:16 symbol is used when the instruction’s operand-size attribute is 16 bits; the ptr16:32 symbol is used when the operand-size attribute is 32 bits; the ptr16:64 symbol is used when the operand-size attribute is 64 bits.

• **r8** — One of the byte general-purpose registers: AL, CL, DL, BL, AH, CH, DH, BH, BPL, SPL, DIL and SIL; or one of the byte registers (R8L - R15L) available when using REX.R and 64-bit mode.

• **r16** — One of the word general-purpose registers: AX, CX, DX, BX, SP, BP, SI, DI; or one of the word registers (R8-R15) available when using REX.R and 64-bit mode.

• **r32** — One of the doubleword general-purpose registers: EAX, ECX, EDX, EBX, ESP, EBP, ESI, EDI; or one of the doubleword registers (R8D - R15D) available when using REX.R in 64-bit mode.

• **r64** — One of the quadword general-purpose registers: RAX, RBX, RCX, RDX, RDI, RSI, RBP, RSP, R8–R15. These are available when using REX.R and 64-bit mode.

• **imm8** — An immediate byte value. The imm8 symbol is a signed number between –128 and +127 inclusive. For instructions in which imm8 is combined with a word or doubleword operand, the immediate value is sign-extended to form a word or doubleword. The upper byte of the word is filled with the topmost bit of the immediate value.

• **imm16** — An immediate word value used for instructions whose operand-size attribute is 16 bits. This is a number between –32,768 and +32,767 inclusive.

• **imm32** — An immediate doubleword value used for instructions whose operand-size attribute is 32 bits. It allows the use of a number between +2,147,483,647 and –2,147,483,648 inclusive.

• **imm64** — An immediate quadword value used for instructions whose operand-size attribute is 64 bits. The value allows the use of a number between +9,223,372,036,854,775,807 and –9,223,372,036,854,775,808 inclusive.

• **r/m8** — A byte operand that is either the contents of a byte general-purpose register (AL, CL, DL, BL, AH, CH, DH, BH, BPL, SPL, DIL and SIL) or a byte from memory. Byte registers R8L - R15L are available using REX.R in 64-bit mode.

• **r/m16** — A word general-purpose register or memory operand used for instructions whose operand-size attribute is 16 bits. The word general-purpose registers are: AX, CX, DX, BX, SP, BP, SI, DI. The contents of memory are found at the address provided by the effective address computation. Word registers R8W - R15W are available using REX.R in 64-bit mode.
• **r/m32** — A doubleword general-purpose register or memory operand used for instructions whose operand-size attribute is 32 bits. The doubleword general-purpose registers are: EAX, ECX, EDX, EBX, ESP, EBP, ESI, EDI. The contents of memory are found at the address provided by the effective address computation. Doubleword registers R8D - R15D are available when using REX.R in 64-bit mode.

• **r/m64** — A quadword general-purpose register or memory operand used for instructions whose operand-size attribute is 64 bits when using REX.W. Quadword general-purpose registers are: RAX, RBX, RCX, RDX, RDI, RSI, RBP, RSP, R8–R15; these are available only in 64-bit mode. The contents of memory are found at the address provided by the effective address computation.

• **m** — A 16-, 32- or 64-bit operand in memory.

• **m8** — A byte operand in memory, usually expressed as a variable or array name, but pointed to by the DS:(E)SI or ES:(E)DI registers. In 64-bit mode, it is pointed to by the RSI or RDI registers.

• **m16** — A word operand in memory, usually expressed as a variable or array name, but pointed to by the DS:(E)SI or ES:(E)DI registers. This nomenclature is used only with the string instructions.

• **m32** — A doubleword operand in memory, usually expressed as a variable or array name, but pointed to by the DS:(E)SI or ES:(E)DI registers. This nomenclature is used only with the string instructions.

• **m64** — A memory quadword operand in memory.

• **m128** — A memory double quadword operand in memory.

• **m16:16, m16:32 & m16:64** — A memory operand containing a far pointer composed of two numbers. The number to the left of the colon corresponds to the pointer's segment selector. The number to the right corresponds to its offset.

• **m16&32, m16&16, m32&32, m16&64** — A memory operand consisting of data item pairs whose sizes are indicated on the left and the right side of the ampersand. All memory addressing modes are allowed. The m16&16 and m32&32 operands are used by the BOUND instruction to provide an operand containing an upper and lower bounds for array indices. The m16&32 operand is used by LIDT and LGDT to provide a word with which to load the limit field, and a doubleword with which to load the base field of the corresponding GDTR and IDTR registers. The m16&64 operand is used by LIDT and LGDT in 64-bit mode to provide a word with which to load the limit field, and a quadword with which to load the base field of the corresponding GDTR and IDTR registers.

• **moffs8, moffs16, moffs32, moffs64** — A simple memory variable (memory offset) of type byte, word, or doubleword used by some variants of the MOV instruction. The actual address is given by a simple offset relative to the segment base. No ModR/M byte is used in the instruction. The number shown with moffs indicates its size, which is determined by the address-size attribute of the instruction.
• **Sreg** — A segment register. The segment register bit assignments are ES = 0, CS = 1, SS = 2, DS = 3, FS = 4, and GS = 5.

• **m32fp, m64fp, m80fp** — A single-precision, double-precision, and double extended-precision (respectively) floating-point operand in memory. These symbols designate floating-point values that are used as operands for x87 FPU floating-point instructions.

• **m16int, m32int, m64int** — A word, doubleword, and quadword integer (respectively) operand in memory. These symbols designate integers that are used as operands for x87 FPU integer instructions.

• **ST or ST(0)** — The top element of the FPU register stack.

• **ST(i)** — The i\(^{th}\) element from the top of the FPU register stack (i ← 0 through 7).

• **mm** — An MMX register. The 64-bit MMX registers are: MM0 through MM7.

• **mm/m32** — The low order 32 bits of an MMX register or a 32-bit memory operand. The 64-bit MMX registers are: MM0 through MM7. The contents of memory are found at the address provided by the effective address computation.

• **mm/m64** — An MMX register or a 64-bit memory operand. The 64-bit MMX registers are: MM0 through MM7. The contents of memory are found at the address provided by the effective address computation.

• **xmm** — An XMM register. The 128-bit XMM registers are: XMM0 through XMM7; XMM8 through XMM15 are available using REX.R in 64-bit mode.

• **xmm/m32** — An XMM register or a 32-bit memory operand. The 128-bit XMM registers are: XMM0 through XMM7; XMM8 through XMM15 are available using REX.R in 64-bit mode. The contents of memory are found at the address provided by the effective address computation.

• **xmm/m64** — An XMM register or a 64-bit memory operand. The 128-bit SIMD floating-point registers are: XMM0 through XMM7; XMM8 through XMM15 are available using REX.R in 64-bit mode. The contents of memory are found at the address provided by the effective address computation.

• **xmm/m128** — An XMM register or a 128-bit memory operand. The 128-bit XMM registers are: XMM0 through XMM7; XMM8 through XMM15 are available using REX.R in 64-bit mode. The contents of memory are found at the address provided by the effective address computation.

• **<XMM0>** — Indicates implied use of the XMM0 register. When there is ambiguity, xmm1 indicates the first source operand using an XMM register and xmm2 the second source operand using an XMM register. Some instructions use the XMM0 register as the third source operand, indicated by <XMM0>. The use of the third XMM register operand is implicit in the instruction encoding and does not affect the ModR/M encoding.
3.1.1.3 64-bit Mode Column in the Instruction Summary Table

The "64-bit Mode" column indicates whether the opcode sequence is supported in 64-bit mode. The column uses the following notation:

- **Valid** — Supported.
- **Invalid** — Not supported.
- **N.E.** — Indicates an instruction syntax is not encodable in 64-bit mode (it may represent part of a sequence of valid instructions in other modes).
- **N.P.** — Indicates the REX prefix does not affect the legacy instruction in 64-bit mode.
- **N.I.** — Indicates the opcode is treated as a new instruction in 64-bit mode.
- **N.S.** — Indicates an instruction syntax that requires an address override prefix in 64-bit mode and is not supported. Using an address override prefix in 64-bit mode may result in model-specific execution behavior.

3.1.1.4 Compatibility/Legacy Mode Column in the Instruction Summary Table

The "Compatibility/Legacy Mode" column provides information on the opcode sequence in either the compatibility mode or other IA-32 modes. The column uses the following notation:

- **Valid** — Supported.
- **Invalid** — Not supported.
- **N.E.** — Indicates an Intel 64 instruction mnemonics/syntax that is not encodable; the opcode sequence is not applicable as an individual instruction in compatibility mode or IA-32 mode. The opcode may represent a valid sequence of legacy IA-32 instructions.

3.1.1.5 Description Column in the Instruction Summary Table

The "Description" column briefly explains forms of the instruction.

3.1.1.6 Description Section

Each instruction is then described by number of information sections. The "Description" section describes the purpose of the instructions and required operands in more detail.

3.1.1.7 Operation Section

The "Operation" section contains an algorithm description (frequently written in pseudo-code) for the instruction. Algorithms are composed of the following elements:
INSTRUCTION SET REFERENCE, A-M

• Comments are enclosed within the symbol pairs "(*" and ")*".
• Compound statements are enclosed in keywords, such as: IF, THEN, ELSE and FI for an if statement; DO and OD for a do statement; or CASE... OF for a case statement.
• A register name implies the contents of the register. A register name enclosed in brackets implies the contents of the location whose address is contained in that register. For example, ES:[DI] indicates the contents of the location whose ES segment relative address is in register DI. [SI] indicates the contents of the address contained in register SI relative to the SI register’s default segment (DS) or the overridden segment.
• Parentheses around the “E” in a general-purpose register name, such as (E)SI, indicates that the offset is read from the SI register if the address-size attribute is 16, from the ESI register if the address-size attribute is 32. Parentheses around the “R” in a general-purpose register name, (R)SI, in the presence of a 64-bit register definition such as (R)SI, indicates that the offset is read from the 64-bit RSI register if the address-size attribute is 64.
• Brackets are used for memory operands where they mean that the contents of the memory location is a segment-relative offset. For example, [SRC] indicates that the content of the source operand is a segment-relative offset.
• A ← B indicates that the value of B is assigned to A.
• The symbols =, ≠, >, <, ≥, and ≤ are relational operators used to compare two values: meaning equal, not equal, greater or equal, less or equal, respectively. A relational expression such as A ← B is TRUE if the value of A is equal to B; otherwise it is FALSE.
• The expression “<< COUNT” and “>> COUNT” indicates that the destination operand should be shifted left or right by the number of bits indicated by the count operand.

The following identifiers are used in the algorithmic descriptions:

- **OperandSize and AddressSize** — The OperandSize identifier represents the operand-size attribute of the instruction, which is 16, 32 or 64-bits. The AddressSize identifier represents the address-size attribute, which is 16, 32 or 64-bits. For example, the following pseudo-code indicates that the operand-size attribute depends on the form of the MOV instruction used.

  IF Instruction ← MOVw
  THEN OperandSize ← 16;
  ELSE
    IF Instruction ← MOVD
    THEN OperandSize ← 32;
    ELSE
      IF Instruction ← MOVQ
      THEN OperandSize ← 64;
      FI;
See "Operand-Size and Address-Size Attributes" in Chapter 3 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for guidelines on how these attributes are determined.

- **StackAddrSize** — Represents the stack address-size attribute associated with the instruction, which has a value of 16, 32 or 64-bits. See "Address-Size Attribute for Stack" in Chapter 6, "Procedure Calls, Interrupts, and Exceptions," of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

- **SRC** — Represents the source operand.
- **DEST** — Represents the destination operand.

The following functions are used in the algorithmic descriptions:

- **ZeroExtend(value)** — Returns a value zero-extended to the operand-size attribute of the instruction. For example, if the operand-size attribute is 32, zero extending a byte value of –10 converts the byte from F6H to a doubleword value of 000000F6H. If the value passed to the ZeroExtend function and the operand-size attribute are the same size, ZeroExtend returns the value unaltered.

- **SignExtend(value)** — Returns a value sign-extended to the operand-size attribute of the instruction. For example, if the operand-size attribute is 32, sign extending a byte containing the value –10 converts the byte from F6H to a doubleword value of FFFFFFF6H. If the value passed to the SignExtend function and the operand-size attribute are the same size, SignExtend returns the value unaltered.

- **SaturateSignedWordToSignedByte** — Converts a signed 16-bit value to a signed 8-bit value. If the signed 16-bit value is less than –128, it is represented by the saturated value -128 (80H); if it is greater than 127, it is represented by the saturated value 127 (7FH).

- **SaturateSignedDwordToSignedWord** — Converts a signed 32-bit value to a signed 16-bit value. If the signed 32-bit value is less than –32768, it is represented by the saturated value –32768 (8000H); if it is greater than 32767, it is represented by the saturated value 32767 (7FFFH).

- **SaturateSignedWordToUnsignedByte** — Converts a signed 16-bit value to an unsigned 8-bit value. If the signed 16-bit value is less than zero, it is represented by the saturated value zero (00H); if it is greater than 255, it is represented by the saturated value 255 (FFH).

- **SaturateToSignedByte** — Represents the result of an operation as a signed 8-bit value. If the result is less than –128, it is represented by the saturated value –128 (80H); if it is greater than 127, it is represented by the saturated value 127 (7FH).

- **SaturateToSignedWord** — Represents the result of an operation as a signed 16-bit value. If the result is less than –32768, it is represented by the saturated value –32768 (8000H); if it is greater than 32767, it is represented by the saturated value 32767 (7FFFH).
• **SaturateToUnsignedByte** — Represents the result of an operation as a signed 8-bit value. If the result is less than zero it is represented by the saturated value zero (00H); if it is greater than 255, it is represented by the saturated value 255 (FFH).

• **SaturateToUnsignedWord** — Represents the result of an operation as a signed 16-bit value. If the result is less than zero it is represented by the saturated value zero (00H); if it is greater than 65535, it is represented by the saturated value 65535 (FFFFH).

• **LowOrderWord**(DEST * SRC) — Multiplies a word operand by a word operand and stores the least significant word of the doubleword result in the destination operand.

• **HighOrderWord**(DEST * SRC) — Multiplies a word operand by a word operand and stores the most significant word of the doubleword result in the destination operand.

• **Push**(value) — Pushes a value onto the stack. The number of bytes pushed is determined by the operand-size attribute of the instruction. See the “Operation” subsection of the “PUSH—Push Word, Doubleword or Quadword Onto the Stack” section in Chapter 4 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*.

• **Pop()** removes the value from the top of the stack and returns it. The statement EAX ← Pop(); assigns to EAX the 32-bit value from the top of the stack. Pop will return either a word, a doubleword or a quadword depending on the operand-size attribute. See the “Operation” subsection in the ”POP—Pop a Value from the Stack” section of Chapter 4 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*.

• **PopRegisterStack** — Marks the FPU ST(0) register as empty and increments the FPU register stack pointer (TOP) by 1.

• **Switch-Tasks** — Performs a task switch.

• **Bit**(BitBase, BitOffset) — Returns the value of a bit within a bit string. The bit string is a sequence of bits in memory or a register. Bits are numbered from low-order to high-order within registers and within memory bytes. If the BitBase is a register, the BitOffset can be in the range 0 to [15, 31, 63] depending on the mode and register size. See Figure 3-1: the function Bit[RAX, 21] is illustrated.

![Figure 3-1. Bit Offset for BIT[RAX, 21]](image_url)
If BitBase is a memory address, the BitOffset can range depending on the operand size (see Table 3-2).

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Immediate BitOffset</th>
<th>Register BitOffset</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>0 to 15</td>
<td>(-2^{15} to 2^{15} - 1)</td>
</tr>
<tr>
<td>32</td>
<td>0 to 31</td>
<td>(-2^{31} to 2^{31} - 1)</td>
</tr>
<tr>
<td>64</td>
<td>0 to 63</td>
<td>(-2^{63} to 2^{63} - 1)</td>
</tr>
</tbody>
</table>

The addressed bit is numbered (Offset MOD 8) within the byte at address (BitBase + (BitOffset DIV 8)) where DIV is signed division with rounding towards negative infinity and MOD returns a positive number (see Figure 3-2).

**Figure 3-2. Memory Bit Indexing**

### 3.1.1.8 Intel® C/C++ Compiler Intrinsics Equivalents Section

The Intel C/C++ compiler intrinsics equivalents are special C/C++ coding extensions that allow using the syntax of C function calls and C variables instead of hardware registers. Using these intrinsics frees programmers from having to manage registers and assembly programming. Further, the compiler optimizes the instruction scheduling so that executable run faster.

The following sections discuss the intrinsics API and the MMX technology and SIMD floating-point intrinsics. Each intrinsic equivalent is listed with the instruction description. There may be additional intrinsics that do not have an instruction equiv-
alent. It is strongly recommended that the reader reference the compiler documentation for the complete list of supported intrinsics.


**Intrinsics API**

The benefit of coding with MMX technology intrinsics and the SSE/SSE2/SSE3 intrinsics is that you can use the syntax of C function calls and C variables instead of hardware registers. This frees you from managing registers and programming assembly. Further, the compiler optimizes the instruction scheduling so that your executable runs faster. For each computational and data manipulation instruction in the new instruction set, there is a corresponding C intrinsic that implements it directly. The intrinsics allow you to specify the underlying implementation (instruction selection) of an algorithm yet leave instruction scheduling and register allocation to the compiler.

**MMX™ Technology Intrinsics**

The MMX technology intrinsics are based on a __m64 data type that represents the specific contents of an MMX technology register. You can specify values in bytes, short integers, 32-bit values, or a 64-bit object. The __m64 data type, however, is not a basic ANSI C data type, and therefore you must observe the following usage restrictions:

- Use __m64 data only on the left-hand side of an assignment, as a return value, or as a parameter. You cannot use it with other arithmetic expressions (“+”, “>”, and so on).
- Use __m64 objects in aggregates, such as unions to access the byte elements and structures; the address of an __m64 object may be taken.
- Use __m64 data only with the MMX technology intrinsics described in this manual and Intel® C/C++ compiler documentation.
- See:
  - http://www.intel.com/support/performancetools/
  - SSE/SSE2/SSE3 Intrinsics
  - SSE/SSE2/SSE3 intrinsics all make use of the XMM registers of the Pentium III, Pentium 4, and Intel Xeon processors. There are three data types supported by these intrinsics: __m128, __m128d, and __m128i.
• The __m128 data type is used to represent the contents of an XMM register used by an SSE intrinsic. This is either four packed single-precision floating-point values or a scalar single-precision floating-point value.

• The __m128d data type holds two packed double-precision floating-point values or a scalar double-precision floating-point value.

• The __m128i data type can hold sixteen byte, eight word, or four doubleword, or two quadword integer values.

The compiler aligns __m128, __m128d, and __m128i local and global data to 16-byte boundaries on the stack. To align integer, float, or double arrays, use thedeclspec statement as described in Intel C/C++ compiler documentation. See http://www.intel.com/support/performancetools/.

The __m128, __m128d, and __m128i data types are not basic ANSI C data types and therefore some restrictions are placed on its usage:

• Use __m128, __m128d, and __m128i only on the left-hand side of an assignment, as a return value, or as a parameter. Do not use it in other arithmetic expressions such as “+” and “>>.”

• Do not initialize __m128, __m128d, and __m128i with literals; there is no way to express 128-bit constants.

• Use __m128, __m128d, and __m128i objects in aggregates, such as unions (for example, to access the float elements) and structures. The address of these objects may be taken.

• Use __m128, __m128d, and __m128i data only with the intrinsics described in this user’s guide. See Appendix C, “Intel® C/C++ Compiler Intrinsics and Functional Equivalents,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B, for more information on using intrinsics.

The compiler aligns __m128, __m128d, and __m128i local data to 16-byte boundaries on the stack. Global __m128 data is also aligned on 16-byte boundaries. (To align float arrays, you can use the alignmentdeclspec described in the following section.) Because the new instruction set treats the SIMD floating-point registers in the same way whether you are using packed or scalar data, there is no __m32 data type to represent scalar data as you might expect. For scalar operations, you should use the __m128 objects and the “scalar” forms of the intrinsics; the compiler and the processor implement these operations with 32-bit memory references.

The suffixes ps and ss are used to denote “packed single” and “scalar single” precision operations. The packed floats are represented in right-to-left order, with the lowest word (right-most) being used for scalar operations: [z, y, x, w]. To explain how memory storage reflects this, consider the following example.

The operation:

```c
float a[4] ← [ 1.0, 2.0, 3.0, 4.0 ];
__m128 t ← _mm_load_ps(a);
```

Produces the same result as follows:
In other words:

\[
t \leftarrow [4.0, 3.0, 2.0, 1.0]
\]

Where the “scalar” element is 1.0.

Some intrinsics are “composites” because they require more than one instruction to implement them. You should be familiar with the hardware features provided by the SSE, SSE2, SSE3, and MMX technology when writing programs with the intrinsics.

Keep the following important issues in mind:

- Certain intrinsics, such as _mm_loadr_ps and _mm_cmpgt_ss, are not directly supported by the instruction set. While these intrinsics are convenient programming aids, be mindful of their implementation cost.
- Data loaded or stored as __m128 objects must generally be 16-byte-aligned.
- Some intrinsics require that their argument be immediates, that is, constant integers (literals), due to the nature of the instruction.
- The result of arithmetic operations acting on two NaN (Not a Number) arguments is undefined. Therefore, floating-point operations using NaN arguments may not match the expected behavior of the corresponding assembly instructions.

For a more detailed description of each intrinsic and additional information related to its usage, refer to Intel C/C++ compiler documentation. See:


### 3.1.1.9 Flags Affected Section

The “Flags Affected” section lists the flags in the EFLAGS register that are affected by the instruction. When a flag is cleared, it is equal to 0; when it is set, it is equal to 1. The arithmetic and logical instructions usually assign values to the status flags in a uniform manner (see Appendix A, “EFLAGS Cross-Reference,” in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*). Non-conventional assignments are described in the “Operation” section. The values of flags listed as *undefined* may be changed by the instruction in an indeterminate manner. Flags that are not listed are unchanged by the instruction.

### 3.1.1.10 FPU Flags Affected Section

The floating-point instructions have an “FPU Flags Affected” section that describes how each instruction can affect the four condition code flags of the FPU status word.
### 3.1.1.11 Protected Mode Exceptions Section

The "Protected Mode Exceptions" section lists the exceptions that can occur when the instruction is executed in protected mode and the reasons for the exceptions. Each exception is given a mnemonic that consists of a pound sign (#) followed by two letters and an optional error code in parentheses. For example, #GP(0) denotes a general protection exception with an error code of 0. Table 3-3 associates each two-letter mnemonic with the corresponding interrupt vector number and exception name. See Chapter 6, "Interrupt and Exception Handling," in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, for a detailed description of the exceptions.

Application programmers should consult the documentation provided with their operating systems to determine the actions taken when exceptions occur.

**Table 3-3. Intel 64 and IA-32 General Exceptions**

<table>
<thead>
<tr>
<th>Vector No.</th>
<th>Name</th>
<th>Source</th>
<th>Protected Mode&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Real Address Mode</th>
<th>Virtual 8086 Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>#DE—Divide Error</td>
<td>DIV and IDIV instructions.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>1</td>
<td>#DB—Debug</td>
<td>Any code or data reference.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>#BP—Breakpoint</td>
<td>INT 3 instruction.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>#OF—Overflow</td>
<td>INTO instruction.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>#BR—BOUND Range Exceeded</td>
<td>BOUND instruction.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>6</td>
<td>#UD—Invalid Opcode (Undefined Opcode)</td>
<td>UD2 instruction or reserved opcode.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>7</td>
<td>#NM—Device Not Available (No Math Coprocessor)</td>
<td>Floating-point or WAIT/FWAIT instruction.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>8</td>
<td>#DF—Double Fault</td>
<td>Any instruction that can generate an exception, an NMI, or an INTR.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>10</td>
<td>#TS—Invalid TSS</td>
<td>Task switch or TSS access.</td>
<td>Yes</td>
<td>Reserved</td>
<td>Yes</td>
</tr>
<tr>
<td>11</td>
<td>#NP—Segment Not Present</td>
<td>Loading segment registers or accessing system segments.</td>
<td>Yes</td>
<td>Reserved</td>
<td>Yes</td>
</tr>
<tr>
<td>12</td>
<td>#SS—Stack Segment Fault</td>
<td>Stack operations and SS register loads.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>13</td>
<td>#GP—General Protection&lt;sup&gt;2&lt;/sup&gt;</td>
<td>Any memory reference and other protection checks.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

<sup>1</sup> The Protected Mode column indicates whether the exception occurs in protected mode.

<sup>2</sup> General Protection refers to exceptions that can occur for any memory reference and other protection checks.
3.1.1.12 Real-Address Mode Exceptions Section

The "Real-Address Mode Exceptions" section lists the exceptions that can occur when the instruction is executed in real-address mode (see Table 3-3).

3.1.1.13 Virtual-8086 Mode Exceptions Section

The "Virtual-8086 Mode Exceptions" section lists the exceptions that can occur when the instruction is executed in virtual-8086 mode (see Table 3-3).

3.1.1.14 Floating-Point Exceptions Section

The "Floating-Point Exceptions" section lists exceptions that can occur when an x87 FPU floating-point instruction is executed. All of these exception conditions result in a floating-point error exception (#MF, vector number 16) being generated. Table 3-4 associates a one- or two-letter mnemonic with the corresponding exception name. See "Floating-Point Exception Conditions" in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a detailed description of these exceptions.
3.1.1.15  SIMD Floating-Point Exceptions Section

The "SIMD Floating-Point Exceptions" section lists exceptions that can occur when an SSE/SSE2/SSE3 floating-point instruction is executed. All of these exception conditions result in a SIMD floating-point error exception (#XM, vector number 19) being generated. Table 3-5 associates a one-letter mnemonic with the corresponding exception name. For a detailed description of these exceptions, refer to "SSE and SSE2 Exceptions", in Chapter 11 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

Table 3-5. SIMD Floating-Point Exceptions

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Name</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>#I</td>
<td>Floating-point invalid operation: - Stack overflow or underflow - Invalid arithmetic operation</td>
<td>Invalid arithmetic operation or source operand</td>
</tr>
<tr>
<td>#Z</td>
<td>Floating-point divide-by-zero</td>
<td>Divide-by-zero</td>
</tr>
<tr>
<td>#D</td>
<td>Floating-point denormal operand</td>
<td>Source operand that is a denormal number</td>
</tr>
<tr>
<td>#O</td>
<td>Floating-point numeric overflow</td>
<td>Overflow in result</td>
</tr>
<tr>
<td>#U</td>
<td>Floating-point numeric underflow</td>
<td>Underflow in result</td>
</tr>
<tr>
<td>#P</td>
<td>Floating-point inexact result (precision)</td>
<td>Inexact result (precision)</td>
</tr>
</tbody>
</table>

3.1.1.16  Compatibility Mode Exceptions Section

This section lists exception that occur within compatibility mode.

3.1.1.17  64-Bit Mode Exceptions Section

This section lists exception that occur within 64-bit mode.
3.1.2 Imm8 Control Byte Operation for PCMPESTRI / PCMPESTRM / PCMPISTRI / PCMPISTRM

The notations introduced in this section are referenced in the reference pages of PCMPESTRI, PCMPESTRM, PCMPISTRI, PCMPISTRM. The operation of the immediate control byte is common to these four string text processing instructions of SSE4.2, see Chapter 4, “Instruction Set Reference, N-Z,”. This section describes the common operations.

3.1.2.1 General Description

The operation of PCMPESTRI, PCMPESTRM, PCMPISTRI, PCMPISTRM is defined by the combination of the respective opcode and the interpretation of an immediate control byte that is part of the instruction encoding.

The opcode controls the relationship of input bytes/words to each other (determines whether the inputs terminated strings or whether lengths are expressed explicitly) as well as the desired output (index or mask).

The Imm8 Control Byte for PCMPxSTRx encodes a significant amount of programmable control over the functionality of those instructions. Some functionality is unique to each instruction while some is common across some or all of the four instructions. This section describes functionality which is common across the four instructions.

The arithmetic flags (ZF, CF, SF, OF, AF, PF) are set as a result of these instructions. However, the meanings of the flags have been overloaded from their typical meanings in order to provide additional information regarding the relationships of the two inputs.

PCMPxSTRx instructions perform arithmetic comparisons between all possible pairs of bytes or words, one from each packed input source operand. The boolean results of those comparisons are then aggregated in order to produce meaningful results. The Imm8 Control Byte is used to affect the interpretation of individual input elements as well as control the arithmetic comparisons used and the specific aggregation scheme.

Specifically, the Imm8 Control Byte consists of bit fields that control the following attributes:

- **Source data format** — Byte/word data element granularity, signed or unsigned elements
- **Aggregation operation** — Encodes the mode of per-element comparison operation and the aggregation of per-element comparisons into an intermediate result
• **Polarity** — Specifies intermediate processing to be performed on the intermediate result

• **Output selection** — Specifies final operation to produce the output (depending on index or mask) from the intermediate result

### 3.1.2.2 Source Data Format

**Table 3-6. Source Data Format**

<table>
<thead>
<tr>
<th>Imm8[1:0]</th>
<th>Meaning</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00b</td>
<td>Unsigned bytes</td>
<td>Both 128-bit sources are treated as packed, unsigned bytes.</td>
</tr>
<tr>
<td>01b</td>
<td>Unsigned words</td>
<td>Both 128-bit sources are treated as packed, unsigned words.</td>
</tr>
<tr>
<td>10b</td>
<td>Signed bytes</td>
<td>Both 128-bit sources are treated as packed, signed bytes.</td>
</tr>
<tr>
<td>11b</td>
<td>Signed words</td>
<td>Both 128-bit sources are treated as packed, signed words.</td>
</tr>
</tbody>
</table>

If the Imm8 Control Byte has bit[0] cleared, each source contains 16 packed bytes. If the bit is set each source contains 8 packed words. If the Imm8 Control Byte has bit[1] cleared, each input contains unsigned data. If the bit is set each source contains signed data.
3.1.2.3 Aggregation Operation

Table 3-7. Aggregation Operation

<table>
<thead>
<tr>
<th>Imm8[3:2]</th>
<th>Mode</th>
<th>Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>00b</td>
<td>Equal any</td>
<td>The arithmetic comparison is “equal.”</td>
</tr>
<tr>
<td>01b</td>
<td>Ranges</td>
<td>Arithmetic comparison is “greater than or equal” between even indexed bytes/words of reg and each byte/word of reg/mem. Arithmetic comparison is “less than or equal” between odd indexed bytes/words of reg and each byte/word of reg/mem. (reg/mem[m] &gt;= reg[n] for n = even, reg/mem[m] &lt;= reg[n] for n = odd)</td>
</tr>
<tr>
<td>10b</td>
<td>Equal each</td>
<td>The arithmetic comparison is “equal.”</td>
</tr>
<tr>
<td>11b</td>
<td>Equal ordered</td>
<td>The arithmetic comparison is “equal.”</td>
</tr>
</tbody>
</table>

All 256 (64) possible comparisons are always performed. The individual Boolean results of those comparisons are referred to as “BoolRes[Reg/Mem element index, Reg element index].” Comparisons evaluating to “True” are represented with a 1, False with a 0 (positive logic). The initial results are then aggregated into a 16-bit (8-bit) intermediate result (IntRes1) using one of the modes described in the table above, as determined by Imm8 Control Byte bit[3:2].

See Section 3.1.2.6 for a description of the overrideIfDataInvalid() function used in Table 3-8.
3.1.2.4 Polarity

IntRes1 may then be further modified by performing a 1’s compliment, according to the value of the Imm8 Control Byte bit[4]. Optionally, a mask may be used such that only those IntRes1 bits which correspond to "valid" reg/mem input elements are complemented (note that the definition of a valid input element is dependant on the specific opcode and is defined in each opcode’s description). The result of the possible negation is referred to as IntRes2.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Pseudocode</th>
</tr>
</thead>
</table>
| Equal any                   | UpperBound = imm8[0] ? 7 : 15;  
                           | IntRes1 = 0;                                 |
|                             | For j = 0 to UpperBound, j++  
                           | For i = 0 to UpperBound, i++                  |
|                             | IntRes1[j] OR= overrideIfDataInvalid(BoolRes[j,i]) |
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3.1.2.5 Output Selection

Table 3-9. Polarity

<table>
<thead>
<tr>
<th>Imm8[5:4]</th>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00b</td>
<td>Positive Polarity (+)</td>
<td>IntRes2 = IntRes1</td>
</tr>
<tr>
<td>01b</td>
<td>Negative Polarity (-)</td>
<td>IntRes2 = -1 XOR IntRes1</td>
</tr>
<tr>
<td>10b</td>
<td>Masked (+)</td>
<td>IntRes2 = IntRes1</td>
</tr>
</tbody>
</table>

3.1.2.6 Valid/Invalid Override of Comparisons

PCMPxSTRx instructions allow for the possibility that an end-of-string (EOS) situation may occur within the 128-bit packed data value (see the instruction descriptions.

For PCMPESTRI/PCMPISTRI, the Imm8 Control Byte bit[6] is used to determine if the index is of the least significant or most significant bit of IntRes2.

Table 3-10. Output Selection

<table>
<thead>
<tr>
<th>Imm8[6]</th>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b</td>
<td>Least significant index</td>
<td>The index returned to ECX is of the least significant set bit in IntRes2.</td>
</tr>
<tr>
<td>1b</td>
<td>Most significant index</td>
<td>The index returned to ECX is of the most significant set bit in IntRes2.</td>
</tr>
</tbody>
</table>

Specifically for PCMPESTRM/PCMPISTRM, the Imm8 Control Byte bit[6] is used to determine if the mask is a 16 (8) bit mask or a 128 bit byte/word mask.

Table 3-11. Output Selection

<table>
<thead>
<tr>
<th>Imm8[6]</th>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b</td>
<td>Bit mask</td>
<td>IntRes2 is returned as the mask to the least significant bits of XMMO with zero extension to 128 bits.</td>
</tr>
<tr>
<td>1b</td>
<td>Byte/word mask</td>
<td>IntRes2 is expanded into a byte/word mask (based on imm8[1]) and placed in XMMO. The expansion is performed by replicating each bit into all of the bits of the byte/word of the same index.</td>
</tr>
</tbody>
</table>

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below for details). Any data elements on either source that are determined to be past the EOS are considered to be invalid, and the treatment of invalid data within a comparison pair varies depending on the aggregation function being performed.

In general, the individual comparison result for each element pair \( \text{BoolRes}[i,j] \) can be forced true or false if one or more elements in the pair are invalid. See Table 3-12.

### Table 3-12. Comparison Result for Each Element Pair \( \text{BoolRes}[i,j] \)

<table>
<thead>
<tr>
<th>xmm1 byte/word</th>
<th>xmm2/m128 byte/word</th>
<th>Imm8[3:2] = 00b (equal any)</th>
<th>Imm8[3:2] = 01b (ranges)</th>
<th>Imm8[3:2] = 10b (equal each)</th>
<th>Imm8[3:2] = 11b (equal ordered)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid</td>
<td>Invalid</td>
<td>Force false</td>
<td>Force false</td>
<td>Force true</td>
<td>Force true</td>
</tr>
<tr>
<td>Invalid</td>
<td>Valid</td>
<td>Force false</td>
<td>Force false</td>
<td>Force false</td>
<td>Force true</td>
</tr>
<tr>
<td>Valid</td>
<td>Invalid</td>
<td>Force false</td>
<td>Force false</td>
<td>Force false</td>
<td>Force false</td>
</tr>
<tr>
<td>Valid</td>
<td>Valid</td>
<td>Do not force</td>
<td>Do not force</td>
<td>Do not force</td>
<td>Do not force</td>
</tr>
</tbody>
</table>

### 3.1.2.7 Summary of Imm8 Control byte

### Table 3-13. Summary of Imm8 Control Byte

<table>
<thead>
<tr>
<th>Imm8</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>------0b</td>
<td>128-bit sources treated as 16 packed bytes.</td>
</tr>
<tr>
<td>------1b</td>
<td>128-bit sources treated as 8 packed words.</td>
</tr>
<tr>
<td>------0-b</td>
<td>Packed bytes/words are unsigned.</td>
</tr>
<tr>
<td>------1-b</td>
<td>Packed bytes/words are signed.</td>
</tr>
<tr>
<td>-----00-b</td>
<td>Mode is equal any.</td>
</tr>
<tr>
<td>-----01-b</td>
<td>Mode is ranges.</td>
</tr>
<tr>
<td>-----10-b</td>
<td>Mode is equal each.</td>
</tr>
<tr>
<td>-----11-b</td>
<td>Mode is equal ordered.</td>
</tr>
<tr>
<td>------0-b</td>
<td>IntRes1 is unmodified.</td>
</tr>
<tr>
<td>------1-b</td>
<td>IntRes1 is negated (1’s compliment).</td>
</tr>
<tr>
<td>------0-b</td>
<td>Negation of IntRes1 is for all 16 (8) bits.</td>
</tr>
<tr>
<td>------1-b</td>
<td>Negation of IntRes1 is masked by reg/mem validity.</td>
</tr>
<tr>
<td>------0-b</td>
<td>Index of the least significant, set, bit is used (regardless of corresponding input element validity).</td>
</tr>
<tr>
<td></td>
<td>IntRes2 is returned in least significant bits of XMM0.</td>
</tr>
</tbody>
</table>
### Table 3-13. Summary of Imm8 Control Byte (Contd.)

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1-----b</td>
<td>Index of the most significant, set, bit is used (regardless of corresponding input element validity). Each bit of IntRes2 is expanded to byte/word.</td>
</tr>
<tr>
<td>0-----b</td>
<td>This bit currently has no defined effect, should be 0.</td>
</tr>
<tr>
<td>1-----b</td>
<td>This bit currently has no defined effect, should be 0.</td>
</tr>
</tbody>
</table>
3.2 INSTRUCTIONS (A-M)

The remainder of this chapter provides descriptions of Intel 64 and IA-32 instructions (A-M). See also: Chapter 4, “Instruction Set Reference, N-Z,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B.
AAA—ASCII Adjust After Addition

Description
Adjusts the sum of two unpacked BCD values to create an unpacked BCD result. The AL register is the implied source and destination operand for this instruction. The AAA instruction is only useful when it follows an ADD instruction that adds (binary addition) two unpacked BCD values and stores a byte result in the AL register. The AAA instruction then adjusts the contents of the AL register to contain the correct 1-digit unpacked BCD result.

If the addition produces a decimal carry, the AH register increments by 1, and the CF and AF flags are set. If there was no decimal carry, the CF and AF flags are cleared and the AH register is unchanged. In either case, bits 4 through 7 of the AL register are set to 0.

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

Operation
IF 64-Bit Mode
THEN
#UD;
ELSE
IF ((AL AND 0FH) > 9) or (AF = 1)
THEN
AL ← AL + 6;
AH ← AH + 1;
AF ← 1;
CF ← 1;
AL ← AL AND 0FH;
ELSE
AF ← 0;
CF ← 0;
AL ← AL AND 0FH;
FI;
FI;

Flags Affected
The AF and CF flags are set to 1 if the adjustment results in a decimal carry; otherwise they are set to 0. The OF, SF, ZF, and PF flags are undefined.
Protected Mode Exceptions
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as protected mode.

Compatibility Mode Exceptions
Same exceptions as protected mode.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
AAD—ASCII Adjust AX Before Division

Description

Adjusts two unpacked BCD digits (the least-significant digit in the AL register and the most-significant digit in the AH register) so that a division operation performed on the result will yield a correct unpacked BCD value. The AAD instruction is only useful when it precedes a DIV instruction that divides (binary division) the adjusted value in the AX register by an unpacked BCD value.

The AAD instruction sets the value in the AL register to \((AL + (10 \times AH))\), and then clears the AH register to 00H. The value in the AX register is then equal to the binary equivalent of the original unpacked two-digit (base 10) number in registers AH and AL.

The generalized version of this instruction allows adjustment of two unpacked digits of any number base (see the “Operation” section below), by setting the \(imm8\) byte to the selected number base (for example, 08H for octal, 0AH for decimal, or 0CH for base 12 numbers). The AAD mnemonic is interpreted by all assemblers to mean adjust ASCII (base 10) values. To adjust values in another number base, the instruction must be hand coded in machine code \((D5 imm8)\).

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

Operation

IF 64-Bit Mode
   THEN
      #UD;
   ELSE
      tempAL ← AL;
      tempAH ← AH;
      AL ← (tempAL + (tempAH + imm8)) AND FFH;
      (\(^*\) imm8 is set to 0AH for the AAD mnemonic.\(^*\))
      AH ← 0;
   FI;

The immediate value \((imm8)\) is taken from the second byte of the instruction.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D5 0A</td>
<td>AAD</td>
<td>Invalid</td>
<td>Valid</td>
<td>ASCII adjust AX before division.</td>
</tr>
<tr>
<td>D5 ib</td>
<td>(No mnemonic)</td>
<td>Invalid</td>
<td>Valid</td>
<td>Adjust AX before division to number base imm8.</td>
</tr>
</tbody>
</table>
Flags Affected
The SF, ZF, and PF flags are set according to the resulting binary value in the AL register; the OF, AF, and CF flags are undefined.

Protected Mode Exceptions
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as protected mode.

Compatibility Mode Exceptions
Same exceptions as protected mode.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
INSTRUCTION SET REFERENCE, A-M

AAM—ASCII Adjust AX After Multiply

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D4 0A</td>
<td>AAM</td>
<td>Invalid</td>
<td>Valid</td>
<td>ASCII adjust AX after multiply.</td>
</tr>
<tr>
<td>D4 ib</td>
<td>(No mnemonic)</td>
<td>Invalid</td>
<td>Valid</td>
<td>Adjust AX after multiply to number base imm8.</td>
</tr>
</tbody>
</table>

Description

Adjusts the result of the multiplication of two unpacked BCD values to create a pair of unpacked (base 10) BCD values. The AX register is the implied source and destination operand for this instruction. The AAM instruction is only useful when it follows an MUL instruction that multiplies (binary multiplication) two unpacked BCD values and stores a word result in the AX register. The AAM instruction then adjusts the contents of the AX register to contain the correct 2-digit unpacked (base 10) BCD result.

The generalized version of this instruction allows adjustment of the contents of the AX to create two unpacked digits of any number base (see the “Operation” section below). Here, the imm8 byte is set to the selected number base (for example, 08H for octal, 0AH for decimal, or 0CH for base 12 numbers). The AAM mnemonic is interpreted by all assemblers to mean adjust to ASCII (base 10) values. To adjust to values in another number base, the instruction must be hand coded in machine code (D4 imm8).

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

Operation

IF 64-Bit Mode
    THEN
        #UD;
    ELSE
        tempAL ← AL;
        AH ← tempAL / imm8; (* imm8 is set to 0AH for the AAM mnemonic *)
        AL ← tempAL MOD imm8;
    FI;

The immediate value (imm8) is taken from the second byte of the instruction.

Flags Affected

The SF, ZF, and PF flags are set according to the resulting binary value in the AL register. The OF, AF, and CF flags are undefined.
Protected Mode Exceptions
#DE If an immediate value of 0 is used.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as protected mode.

Compatibility Mode Exceptions
Same exceptions as protected mode.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
AAS—ASCII Adjust AL After Subtraction

Description
Adjusts the result of the subtraction of two unpacked BCD values to create a unpacked BCD result. The AL register is the implied source and destination operand for this instruction. The AAS instruction is only useful when it follows a SUB instruction that subtracts (binary subtraction) one unpacked BCD value from another and stores a byte result in the AL register. The AAA instruction then adjusts the contents of the AL register to contain the correct 1-digit unpacked BCD result.

If the subtraction produced a decimal carry, the AH register decrements by 1, and the CF and AF flags are set. If no decimal carry occurred, the CF and AF flags are cleared, and the AH register is unchanged. In either case, the AL register is left with its top four bits set to 0.

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

Operation
IF 64-bit mode
    THEN
        #UD;
    ELSE
        IF ((AL AND 0FH) > 9) or (AF = 1)
            THEN
                AL ← AL - 6;
                AH ← AH - 1;
                AF ← 1;
                CF ← 1;
                AL ← AL AND 0FH;
            ELSE
                CF ← 0;
                AF ← 0;
                AL ← AL AND 0FH;
        FI;
    FI;

Flags Affected
The AF and CF flags are set to 1 if there is a decimal borrow; otherwise, they are cleared to 0. The OF, SF, ZF, and PF flags are undefined.
Protected Mode Exceptions
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as protected mode.

Compatibility Mode Exceptions
Same exceptions as protected mode.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
### ADC—Add with Carry

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 ib</td>
<td>ADC AL, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm8 to AL.</td>
</tr>
<tr>
<td>15 iw</td>
<td>ADC AX, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm16 to AX.</td>
</tr>
<tr>
<td>15 id</td>
<td>ADC EAX, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm32 to EAX.</td>
</tr>
<tr>
<td>REX.w + 15 id</td>
<td>ADC RAX, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with carry imm32 sign extended to 64-bits to RAX.</td>
</tr>
<tr>
<td>80 /2 ib</td>
<td>ADC r/m8, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm8 to r/m8.</td>
</tr>
<tr>
<td>REX + 80 /2 ib</td>
<td>ADC r/m8’, imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with carry imm8 to r/m8.</td>
</tr>
<tr>
<td>81 /2 iw</td>
<td>ADC r/m16, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm16 to r/m16.</td>
</tr>
<tr>
<td>81 /2 id</td>
<td>ADC r/m32, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with CF imm32 to r/m32.</td>
</tr>
<tr>
<td>REX.w + 81 /2 id</td>
<td>ADC r/m64, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with CF imm32 sign extended to 64-bits to r/m64.</td>
</tr>
<tr>
<td>83 /2 ib</td>
<td>ADC r/m16, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with CF sign-extended imm8 to r/m16.</td>
</tr>
<tr>
<td>83 /2 ib</td>
<td>ADC r/m32, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with CF sign-extended imm8 into r/m32.</td>
</tr>
<tr>
<td>REX.w + 83 /2 ib</td>
<td>ADC r/m64, imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with CF sign-extended imm8 into r/m64.</td>
</tr>
<tr>
<td>10 /r</td>
<td>ADC r/m8, r8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry byte register to r/m8.</td>
</tr>
<tr>
<td>REX + 10 /r</td>
<td>ADC r/m8’, r8’</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with carry byte register to r/m64.</td>
</tr>
<tr>
<td>11 /r</td>
<td>ADC r/m16, r16</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry r16 to r/m16.</td>
</tr>
<tr>
<td>11 /r</td>
<td>ADC r/m32, r32</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with CF r32 to r/m32.</td>
</tr>
<tr>
<td>REX.w + 11 /r</td>
<td>ADC r/m64, r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with CF r64 to r/m64.</td>
</tr>
<tr>
<td>12 /r</td>
<td>ADC r8, r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry r/m8 to byte register.</td>
</tr>
<tr>
<td>REX + 12 /r</td>
<td>ADC r8’, r/m8’</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with carry r/m64 to byte register.</td>
</tr>
<tr>
<td>13 /r</td>
<td>ADC r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry r/m16 to r16.</td>
</tr>
</tbody>
</table>
Description

The ADC instruction adds the destination operand (first operand), the source operand (second operand), and the carry (CF) flag and stores the result in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location. (However, two memory operands cannot be used in one instruction.) The state of the CF flag represents a carry from a previous addition. When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The ADC instruction does not distinguish between signed or unsigned operands. Instead, the processor evaluates the result for both data types and sets the OF and CF flags to indicate a carry in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

The ADC instruction is usually executed as part of a multibyte or multiword addition in which an ADD instruction is followed by an ADC instruction.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

\[ \text{DEST} \leftarrow \text{DEST} + \text{SRC} + \text{CF}; \]

Flags Affected

The OF, SF, ZF, AF, CF, and PF flags are set according to the result.

Protected Mode Exceptions

- \#GP(0): If the destination is located in a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
INSTRUCTION SET REFERENCE, A-M

If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#UD  If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

#UD  If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used but the destination is not a memory operand.
## ADD—Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04 ib</td>
<td>ADD AL, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm8 to AL.</td>
</tr>
<tr>
<td>05 iw</td>
<td>ADD AX, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm16 to AX.</td>
</tr>
<tr>
<td>05 id</td>
<td>ADD EAX, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm32 to EAX.</td>
</tr>
<tr>
<td>REX.W + 05 id</td>
<td>ADD RAX, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add imm32 sign-extended to 64-bits to RAX.</td>
</tr>
<tr>
<td>80 /0 ib</td>
<td>ADD r/m8, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm8 to r/m8.</td>
</tr>
<tr>
<td>REX + 80 /0 ib</td>
<td>ADD r/m8*, imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add sign-extended imm8 to r/m64.</td>
</tr>
<tr>
<td>81 /0 iw</td>
<td>ADD r/m16, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm16 to r/m16.</td>
</tr>
<tr>
<td>81 /0 id</td>
<td>ADD r/m32, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm32 to r/m32.</td>
</tr>
<tr>
<td>REX.W + 81 /0 id</td>
<td>ADD r/m64, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add imm32 sign-extended to 64-bits to r/m64.</td>
</tr>
<tr>
<td>83 /0 ib</td>
<td>ADD r/m16, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add sign-extended imm8 to r/m16.</td>
</tr>
<tr>
<td>83 /0 ib</td>
<td>ADD r/m32, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add sign-extended imm8 to r/m32.</td>
</tr>
<tr>
<td>REX.W + 83 /0 ib</td>
<td>ADD r/m64, imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add sign-extended imm8 to r/m64.</td>
</tr>
<tr>
<td>00 /r</td>
<td>ADD r/m8, r8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r8 to r/m8.</td>
</tr>
<tr>
<td>REX + 00 /r</td>
<td>ADD r/m8*, r8*</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add r8 to r/m8.</td>
</tr>
<tr>
<td>01 /r</td>
<td>ADD r/m16, r16</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r16 to r/m16.</td>
</tr>
<tr>
<td>01 /r</td>
<td>ADD r/m32, r32</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r32 to r/m32.</td>
</tr>
<tr>
<td>REX.W + 01 /r</td>
<td>ADD r/m64, r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add r64 to r/m64.</td>
</tr>
<tr>
<td>02 /r</td>
<td>ADD r8, r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r/m8 to r8.</td>
</tr>
<tr>
<td>REX + 02 /r</td>
<td>ADD r8*, r/m8*</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add r/m8 to r8.</td>
</tr>
<tr>
<td>03 /r</td>
<td>ADD r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r/m16 to r16.</td>
</tr>
<tr>
<td>03 /r</td>
<td>ADD r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r/m32 to r32.</td>
</tr>
<tr>
<td>REX.W + 03 /r</td>
<td>ADD r/m64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add r/m64 to r64.</td>
</tr>
</tbody>
</table>

**NOTES:**
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
**Description**

Adds the destination operand (first operand) and the source operand (second operand) and then stores the result in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location. (However, two memory operands cannot be used in one instruction.) When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The ADD instruction performs integer addition. It evaluates the result for both signed and unsigned integer operands and sets the OF and CF flags to indicate a carry (overflow) in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[ \text{DEST} \leftarrow \text{DEST} + \text{SRC}; \]

**Flags Affected**

The OF, SF, ZF, AF, CF, and PF flags are set according to the result.

**Protected Mode Exceptions**

- **#GP(0)**: If the destination is located in a non-writable segment.
- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)**: If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**

- **#GP**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
ADD—Add

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.
INSTRUCTION SET REFERENCE, A-M

ADDPD—Add Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 5B /r</td>
<td>ADDPD xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Add packed double-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
</tbody>
</table>

Description
Performs a SIMD add of the two packed double-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the packed double-precision floating-point results in the destination operand.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Chapter 11 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an overview of SIMD double-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST[63:0] ← DEST[63:0] + SRC[63:0];
DEST[127:64] ← DEST[127:64] + SRC[127:64];

Intel C/C++ Compiler Intrinsic Equivalent
ADDPD __m128d _mm_add_pd (m128d a, m128d b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments. If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCPNT[bit 10] = 1.
ADDPPD—Add Packed Double-Precision Floating-Point Values

INSTRUCTION SET REFERENCE, A-M

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD

If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
ADDPS—Add Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 58</td>
<td>ADDPS xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Add packed single-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD add of the four packed single-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the packed single-precision floating-point results in the destination operand.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Chapter 10 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an overview of SIMD single-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{DEST}[31:0] + \text{SRC}[31:0]; \\
\text{DEST}[63:32] & \leftarrow \text{DEST}[63:32] + \text{SRC}[63:32]; \\
\text{DEST}[95:64] & \leftarrow \text{DEST}[95:64] + \text{SRC}[95:64]; \\
\text{DEST}[127:96] & \leftarrow \text{DEST}[127:96] + \text{SRC}[127:96];
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

ADDPS _m128 _mm_add_ps(_m128 a, _m128 b)

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
ADDPS—Add Packed Single-Precision Floating-Point Values

#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
     If CR0.EM[bit 2] = 1.
     If CR4.OSFXSR[bit 9] = 0.
     If CPUID.01H:EDX.SSE[bit 25] = 0.
     If the LOCK prefix is used.
ADDSD—Add Scalar Double-Precision Floating-Point Values

**Description**

Adds the low double-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the double-precision floating-point result in the destination operand.

The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. The high quadword of the destination operand remains unchanged. See Chapter 11 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an overview of a scalar double-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\text{DEST}[63:0] \leftarrow \text{DEST}[63:0] + \text{SRC}[63:0];
\]

(* DEST[127:64] unchanged *)

**Intel C/C++ Compiler Intrinsic Equivalent**

ADDSD __m128d _mm_add_sd (m128d a, m128d b)

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE2[bit 26] = 0.
    If the LOCK prefix is used.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP  If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM  If CR0.TS[bit 3] = 1.

#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE2[bit 26] = 0.
    If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code)  For a page fault.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.

#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD
If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

#AC(0)
If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
ADDSS—Add Scalar Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 58 /r</td>
<td>ADDSS xmm1, xmm2/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Add the low single-precision floating-point value from xmm2/m32 to xmm1.</td>
</tr>
</tbody>
</table>

Description

Adds the low single-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the single-precision floating-point result in the destination operand.

The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. The three high-order doublewords of the destination operand remain unchanged. See Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an overview of a scalar single-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

Operation

DEST[31:0] ← DEST[31:0] + SRC[31:0];
(* DEST[127:32] unchanged *)

Intel C/C++ Compiler Intrinsic Equivalent

ADDSS __m128 _mm_add_ss(__m128 a, __m128 b)

SIMD Floating-Point Exceptions

Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
ADDSS—Add Scalar Single-Precision Floating-Point Values

INSTRUCTION SET REFERENCE, A-M

#UD
If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

#AC(0)
If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP
If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM
If CR0.TS[bit 3] = 1.

#XM

#UD
If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code)
For a page fault.

#AC(0)
If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)
If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)
If the memory address is in a non-canonical form.

#PF(fault-code)
For a page fault.

#NM
If CR0.TS[bit 3] = 1.

#XM
ADDSS—Add Scalar Single-Precision Floating-Point Values

INSTRUCTION SET REFERENCE, A-M

#UD If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE[bit 25] = 0.
    If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
ADDSUBPD—Packed Double-FP Add/Subtract

Description

Adds the double-precision floating-point values in the high quadword of the source and destination operands and stores the result in the high quadword of the destination operand.

Subtracts the double-precision floating-point value in the low quadword of the source operand from the low quadword of the destination operand and stores the result in the low quadword of the destination operand. See Figure 3-4.

The source operand can be a 128-bit memory location or an XMM register. The destination operand is an XMM register.

Figure 3-4. ADDSUBPD—Packed Double-FP Add/Subtract

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).
Operation
xmm1[63:0] = xmm1[63:0] - xmm2/m128[63:0];
xmm1[127:64] = xmm1[127:64] + xmm2/m128[127:64];

Intel C/C++ Compiler Intrinsic Equivalent
ADDSUBPD __m128d _mm_addsub_pd(__m128d a, __m128d b)

Exceptions
When the source operand is a memory operand, it must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM is 1.
For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.

Real Address Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#NM If TS bit in CR0 is 1.
#UD If CR0.EM[bit 2] = 1.
   For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:ECX.SSE3[bit 0] = 0.
   If the LOCK prefix is used.

Virtual 8086 Mode Exceptions

GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
   If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
   For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:ECX.SSE3[bit 0] = 0.
   If the LOCK prefix is used.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
   If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD

If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
ADDSUBPS—Packed Single-FP Add/Subtract

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F D0 /r</td>
<td>ADDSUBPS xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Add/subtract single-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Adds odd-numbered single-precision floating-point values of the source operand (second operand) with the corresponding single-precision floating-point values from the destination operand (first operand); stores the result in the odd-numbered values of the destination operand.

Subtracts the even-numbered single-precision floating-point values in the source operand from the corresponding single-precision floating values in the destination operand; stores the result into the even-numbered values of the destination operand.

The source operand can be a 128-bit memory location or an XMM register. The destination operand is an XMM register. See Figure 3-5.

**Figure 3-5. ADDSUBPS—Packed Single-FP Add/Subtract**

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).
Operation

\[
\begin{align*}
\text{xmm1}[31:0] &= \text{xmm1}[31:0] - \text{xmm2/m128}[31:0]; \\
\text{xmm1}[63:32] &= \text{xmm1}[63:32] + \text{xmm2/m128}[63:32]; \\
\text{xmm1}[95:64] &= \text{xmm1}[95:64] - \text{xmm2/m128}[95:64]; \\
\text{xmm1}[127:96] &= \text{xmm1}[127:96] + \text{xmm2/m128}[127:96];
\end{align*}
\]

Intel C/C++ Compiler Intrinsic Equivalent

\[
\text{ADDSUBPS } \text{_m128 } \text{_mm_addsub_ps(}_\text{m128 a, _m128 b)}
\]

Exceptions

When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

SiMD Floating-Point Exceptions

Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.


#UD If CR0.EM[bit 2] = 1.
For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.

Real Address Mode Exceptions

GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM If CR0.TS[bit 3] = 1.
INSTRUCTION SET REFERENCE, A-M


#UD  If CR0.EM[bit 2] = 1.
      For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
      If CR4.OSFXSR[bit 9] = 0.
      If CPUID.01H:ECX.SSE3[bit 0] = 0.
      If the LOCK prefix is used.

Virtual 8086 Mode Exceptions

GP(0)  If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
       If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM  If CR0.TS[bit 3] = 1.


#UD  If CR0.EM[bit 2] = 1.
      For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
      If CR4.OSFXSR[bit 9] = 0.
      If CPUID.01H:ECX.SSE3[bit 0] = 0.
      If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.
       If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.

#XM  If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
ADDSUBPS—Packed Single-FP Add/Subtract

#UD

If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
If CR0.E[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
### AND—Logical AND

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24 ib</td>
<td>AND AL, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>AL AND imm8.</td>
</tr>
<tr>
<td>25 iw</td>
<td>AND AX, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>AX AND imm16.</td>
</tr>
<tr>
<td>25 id</td>
<td>AND EAX, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>EAX AND imm32.</td>
</tr>
<tr>
<td>REX.w + 25 id</td>
<td>AND RAX, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>RAX AND imm32 sign-extended to 64-bits.</td>
</tr>
<tr>
<td>80 /4 ib</td>
<td>AND r/m8, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m8 AND imm8.</td>
</tr>
<tr>
<td>REX + 80 /4 ib</td>
<td>AND r/m8', imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 AND imm8 (sign-extended).</td>
</tr>
<tr>
<td>81 /4 iw</td>
<td>AND r/m16, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 AND imm16.</td>
</tr>
<tr>
<td>81 /4 id</td>
<td>AND r/m32, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 AND imm32.</td>
</tr>
<tr>
<td>REX.w + 81 /4 id</td>
<td>AND r/m64, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 AND imm32 sign extended to 64-bits.</td>
</tr>
<tr>
<td>83 /4 ib</td>
<td>AND r/m16, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 AND imm8 (sign-extended).</td>
</tr>
<tr>
<td>83 /4 ib</td>
<td>AND r/m32, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 AND imm8 (sign-extended).</td>
</tr>
<tr>
<td>REX.w + 83 /4 ib</td>
<td>AND r/m64, imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 AND imm8 (sign-extended).</td>
</tr>
<tr>
<td>20 /r</td>
<td>AND r/m8, r8</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m8 AND r8.</td>
</tr>
<tr>
<td>REX + 20 /r</td>
<td>AND r/m8', r8'</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 AND r8 (sign-extended).</td>
</tr>
<tr>
<td>21 /r</td>
<td>AND r/m16, r16</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 AND r16.</td>
</tr>
<tr>
<td>21 /r</td>
<td>AND r/m32, r32</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 AND r32.</td>
</tr>
<tr>
<td>REX.w + 21 /r</td>
<td>AND r/m64, r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 AND r32.</td>
</tr>
<tr>
<td>22 /r</td>
<td>AND r8, r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>r8 AND r/m8.</td>
</tr>
<tr>
<td>REX + 22 /r</td>
<td>AND r8', r/m8'</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 AND r8 (sign-extended).</td>
</tr>
<tr>
<td>23 /r</td>
<td>AND r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>r16 AND r/m16.</td>
</tr>
<tr>
<td>23 /r</td>
<td>AND r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>r32 AND r/m32.</td>
</tr>
<tr>
<td>REX.w + 23 /r</td>
<td>AND r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>r64 AND r/m64.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
Description

Performs a bitwise AND operation on the destination (first) and source (second) operands and stores the result in the destination operand location. The source operand can be an immediate, a register, or a memory location; the destination operand can be a register or a memory location. (However, two memory operands cannot be used in one instruction.) Each bit of the result is set to 1 if both corresponding bits of the first and second operands are 1; otherwise, it is set to 0.

This instruction can be used with a LOCK prefix to allow the it to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

DEST ← DEST AND SRC;

Flags Affected

The OF and CF flags are cleared; the SF, ZF, and PF flags are set according to the result. The state of the AF flag is undefined.

Protected Mode Exceptions

#GP(0) If the destination operand points to a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.
INSTRUCTION SET REFERENCE, A-M

#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.
**ANDPD—Bitwise Logical AND of Packed Double-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 54</td>
<td>ANDPD xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Bitwise logical AND of xmm2/m128 and xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical AND of the two packed double-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the result in the destination operand.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[127:0] ← DEST[127:0] BitwiseAND SRC[127:0];

**Intel C/C++ Compiler Intrinsic Equivalent**

```c
ANDPD _m128d _mm_and_pd(_m128d a, _m128d b)
```

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- **#GP(0)**: For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
  - If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
- **#SS(0)**: For an illegal address in the SS segment.
- **#PF(fault-code)**: For a page fault.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
  - If the LOCK prefix is used.
Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
**ANDPS—Bitwise Logical AND of Packed Single-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 54 /r</td>
<td>ANDPS xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Bitwise logical AND of xmm2/m128 and xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical AND of the four packed single-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the result in the destination operand.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[127:0] ← DEST[127:0] BitwiseAND SRC[127:0];

**Intel C/C++ Compiler Intrinsic Equivalent**

ANDPS _m128 _mm_and_ps(_m128 a, _m128 b)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- #GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
  - If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
- #SS(0) For an illegal address in the SS segment.
- #PF(fault-code) For a page fault.
- #NM If CR0.TS[bit 3] = 1.
- #UD If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.
Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
**ANDNPD—Bitwise Logical AND NOT of Packed Double-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 55 /r</td>
<td>ANDNPD xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Bitwise logical AND NOT of xmm2/m128 and xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Inverts the bits of the two packed double-precision floating-point values in the destination operand (first operand), performs a bitwise logical AND of the two packed double-precision floating-point values in the source operand (second operand) and the temporary inverted result, and stores the result in the destination operand.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[127:0] ← (NOT(DEST[127:0])) BitwiseAND (SRC[127:0]);

**Intel C/C++ Compiler Intrinsic Equivalent**

```
ANDNPD   _m128d  _mm_andnot_pd(_m128d  a,  _m128d  b)
```

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
  
  If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

- **#SS(0)** For an illegal address in the SS segment.

- **#PF(fault-code)** For a page fault.

- **#NM** If CR0.TS[bit 3] = 1.
INSTRUCTION SET REFERENCE, A-M

#UD If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE2[bit 26] = 0.
    If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
    If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE2[bit 26] = 0.
    If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
    If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE2[bit 26] = 0.
    If the LOCK prefix is used.
ANDNPS—Bitwise Logical AND NOT of Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 55 Jr</td>
<td>ANDNPS xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Bitwise logical AND NOT of xmm2/m128 and xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Inverts the bits of the four packed single-precision floating-point values in the destination operand (first operand), performs a bitwise logical AND of the four packed single-precision floating-point values in the source operand (second operand) and the temporary inverted result, and stores the result in the destination operand.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[127:0] ← (NOT(DEST[127:0])) BitwiseAND (SRC[127:0]);

**Intel C/C++ Compiler Intrinsic Equivalent**

ANDNPS __m128 _mm_andnot_ps(__m128 a, __m128 b)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- #GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
  - If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
- #SS(0) For an illegal address in the SS segment.
- #PF(fault-code) For a page fault.
- #NM If CR0.TS[bit 3] = 1.
- #UD If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.
Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
   If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD  If CR0.EM[bit 2] = 1.
      If CR4.OSFXSR[bit 9] = 0.
      If CPUID.01H:EDX.SSE[bit 25] = 0.
      If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
       If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM  If CR0.TS[bit 3] = 1.
#UD   If CR0.EM[bit 2] = 1.
      If CR4.OSFXSR[bit 9] = 0.
      If CPUID.01H:EDX.SSE[bit 25] = 0.
      If the LOCK prefix is used.
ARPL—Adjust RPL Field of Segment Selector

Description

Compares the RPL fields of two segment selectors. The first operand (the destination operand) contains one segment selector and the second operand (source operand) contains the other. (The RPL field is located in bits 0 and 1 of each operand.) If the RPL field of the destination operand is less than the RPL field of the source operand, the ZF flag is set and the RPL field of the destination operand is increased to match that of the source operand. Otherwise, the ZF flag is cleared and no change is made to the destination operand. (The destination operand can be a word register or a memory location; the source operand must be a word register.)

The ARPL instruction is provided for use by operating-system procedures (however, it can also be used by applications). It is generally used to adjust the RPL of a segment selector that has been passed to the operating system by an application program to match the privilege level of the application program. Here the segment selector passed to the operating system is placed in the destination operand and segment selector for the application program’s code segment is placed in the source operand. (The RPL field in the source operand represents the privilege level of the application program.) Execution of the ARPL instruction then insures that the RPL of the segment selector received by the operating system is no lower (does not have a higher privilege) than the privilege level of the application program (the segment selector for the application program’s code segment can be read from the stack following a procedure call).

This instruction executes as described in compatibility mode and legacy mode. It is not encodable in 64-bit mode.


Operation

IF 64-BIT MODE
THEN
  See MOVSXD;
ELSE
  IF DEST[RPL] < SRC[RPL]
  THEN
    ZF ← 1;
    DEST[RPL] ← SRC[RPL];
Flags Affected
The ZF flag is set to 1 if the RPL field of the destination operand is less than that of the source operand; otherwise, it is set to 0.

Protected Mode Exceptions
#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD The ARPL instruction is not recognized in real-address mode.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#UD The ARPL instruction is not recognized in virtual-8086 mode.
If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Not applicable.
BLENDPD — Blend Packed Double Precision Floating-Point Values

Description
Packed double-precision floating-point values from the source operand (second operand) are conditionally copied to the destination operand depending on the mask bits in the immediate operand. The mask bits are bits [1:0] of the immediate byte (third operand). Each mask bit corresponds to a quadword element in a 128-bit operand.

If a mask bit is "1", then the corresponding quadword in the source operand is copied to the destination, else the quadword element in the destination operand is left unchanged.

Operation
IF (imm8[0] == 1)
THEN DEST[63:0] ← SRC[63:0];
ELSE DEST[63:0] ← DEST[63:0]; Fl;
IF (imm8[1] == 1)
THEN DEST[127:64] ← SRC[127:64];
ELSE DEST[127:64] ← DEST[127:64]; Fl;

Intel C/C++ Compiler Intrinsic Equivalent
BLENDPD _m128d _mm_blend_pd (_m128d v1, _m128d v2, const int mask);

SIMD Floating-Point Exceptions
None

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
INSTRUCTION SET REFERENCE, A-M

#NM  If CR0.TS[bit 3] = 1.
#UD  If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Real Mode Exceptions
#GP(0)  If any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#NM  If CR0.TS[bit 3] = 1.
#UD  If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Virtual 8086 Mode Exceptions
Same exceptions as in Real Address Mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in Protected Mode.

64-Bit Mode Exceptions
#GP(0)  If the memory address is in a non-canonical form.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM  If TS in CR0 is set.
#UD  If EM in CR0 is set.
If OSFXSR in CR4 is 0.
If CPUID feature flag ECX.SSE4_1 is 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.
BLENDPS — Blend Packed Single Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 0C</td>
<td>BLENDPS xmm1, xmm2/m128, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Select packed single precision floating-point values from xmm1 and xmm2/m128 from mask specified in imm8 and store the values into xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Packed single-precision floating-point values from the source operand (second operand) are conditionally copied to the destination operand (first operand) depending on the mask bits in the immediate operand. The mask bits are bits [3:0] of the immediate byte (third operand). Each mask bit corresponds to a dword element in a 128-bit operand.

If a mask bit is "1", then the corresponding dword in the source operand is copied to the destination, else the dword element in the destination operand is left unchanged.

**Operation**

IF (imm8[0] == 1)
THEN DEST[31:0] ← SRC[31:0];
ELSE DEST[31:0] ← DEST[31:0]; Fl;
IF (imm8[1] == 1)
THEN DEST[63:32] ← SRC[63:32];
ELSE DEST[63:32] ← DEST[63:32]; Fl;
IF (imm8[2] == 1)
THEN DEST[95:64] ← SRC[95:64];
ELSE DEST[95:64] ← DEST[95:64]; Fl;
IF (imm8[3] == 1)
THEN DEST[127:96] ← SRC[127:96];
ELSE DEST[127:96] ← DEST[127:96]; Fl;

**Intel C/C++ Compiler Intrinsic Equivalent**

BLENDPS __m128 _mm_blend_ps (__m128 v1, __m128 v2, const int mask);

**SIMD Floating-Point Exceptions**

None
Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Real Mode Exceptions

#GP(0) If any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
If not aligned on 16-byte boundary, regardless of segment
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Virtual 8086 Mode Exceptions

Same exceptions as in Real Address Mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in Protected Mode.

64-Bit Mode Exceptions

#GP(0) If the memory address is in a non-canonical form.
If not aligned on 16-byte boundary, regardless of segment
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If TS in CR0 is set.
BLENDPS — Blend Packed Single Precision Floating-Point Values

#UD

If EM in CR0 is set.
If OSFXSR in CR4 is 0.
If CPUID feature flag ECX.SSE4_1 is 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.
BLENDVPD — Variable Blend Packed Double Precision Floating-Point Values

Description

Packed double-precision floating-point values from the source operand (second argument) are conditionally copied to the destination operand (first argument) depending on the mask bits in the implicit third register argument, XMM0. The mask bits are the most significant bit in each qword element of XMM0. Each mask bit corresponds to a quadword element in a 128-bit operand.

If a mask bit is "1", then the corresponding quadword element in the source operand is copied to the destination, else the quadword element in the destination operand is left unchanged.

The register assignment of the third operand is defined to be the architectural register XMM0.

Operation

MASK \leftarrow XMM0;

IF (MASK[63] == 1)

THEN DEST[63:0] \leftarrow SRC[63:0];

ELSE DEST[63:0] \leftarrow DEST[63:0]; FI;

IF (MASK[127] == 1)

THEN DEST[127:64] \leftarrow SRC[127:64];

ELSE DEST[127:64] \leftarrow DEST[127:64]; FI;

Intel C/C++ Compiler Intrinsic Equivalent

BLENDVPD _m128d_mm_blendv_pd(_m128d v1, _m128d v2, _m128d v3);

SIMD Floating-Point Exceptions

None
Protected Mode Exceptions

#GP(0)  For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0)  For an illegal address in the SS segment.

#PF(fault-code)  For a page fault.

#NM     If CR0.TS[bit 3] = 1.
#UD     If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Real Mode Exceptions

#GP(0)  if any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM     If CR0.TS[bit 3] = 1.
#UD     If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Virtual 8086 Mode Exceptions

Same exceptions as in Real Address Mode.

#PF(fault-code)  For a page fault.

Compatibility Mode Exceptions

Same exceptions as in Protected Mode.

64-Bit Mode Exceptions

#GP(0)  If the memory address is in a non-canonical form.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
INSTRUCTION SET REFERENCE, A-M

#PF(fault-code)  For a page fault.
#NM  If TS in CR0 is set.

#UD  If EM in CR0 is set.
  If OSFXSR in CR4 is 0.
  If CPUID feature flag ECX.SSE4_1 is 0.
  If LOCK prefix is used.
  Either the prefix REP (F3h) or REPN (F2H) is used.
### BLENDVPS — Variable Blend Packed Single Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 14 /r</td>
<td>BLENDVPS xmm1, xmm2/m128, &lt;XMM0&gt;</td>
<td>Valid</td>
<td>Valid</td>
<td>Select packed single precision floating-point values from xmm1 and xmm2/m128 from mask specified in XMM0 and store the values into xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Packed single-precision floating-point values from the source operand (second argument) are conditionally written to the destination operand (first argument) depending on the mask bits in the third register argument. The mask bits are the most significant bit in each dword element of XMM0. Each mask bit corresponds to a dword element in a 128-bit operand.

If a mask bit is "1", then the corresponding dword element in the source operand is copied to the destination, else the dword element in the destination operand is left unchanged.

The register assignment of the third operand is defined to be the architectural register XMM0.

**Operation**

```
MASK ← XMM0;
IF (MASK[31] == 1)
    THEN DEST[31:0] ← SRC[31:0];
    ELSE DEST[31:0] ← DEST[31:0]; Fl;
IF (MASK[63] == 1)
    THEN DEST[63:32] ← SRC[63:32];
    ELSE DEST[63:32] ← DEST[63:32]; Fl;
IF (MASK[95] == 1)
    THEN DEST[95:64] ← SRC[95:64];
    ELSE DEST[95:64] ← DEST[95:64]; Fl;
IF (MASK[127] == 1)
    THEN DEST[127:96] ← SRC[127:96];
    ELSE DEST[127:96] ← DEST[127:96]; Fl;
```
Intel C/C++ Compiler Intrinsic Equivalent

BLENDVPS __m128 _mm_blendv_ps(__m128 v1, __m128 v2, __m128 v3);

SIMD Floating-Point Exceptions

None

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Real Mode Exceptions

#GP(0) if any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Virtual 8086 Mode Exceptions

Same exceptions as in Real Address Mode.
#PF(fault-code) For a page fault.
**Compatibility Mode Exceptions**
Same exceptions as in Protected Mode.

**64-Bit Mode Exceptions**

- **#GP(0)** If the memory address is in a non-canonical form.
  If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
- **#SS(0)** If a memory address referencing the SS segment is in a non-canonical form.
- **#PF(fault-code)** For a page fault.
- **#NM** If TS in CR0 is set.
- **#UD** If EM in CR0 is set.
  If OSFXSR in CR4 is 0.
  If CPUID feature flag ECX.SSE4_1 is 0.
  If LOCK prefix is used.
  Either the prefix REP (F3h) or REPN (F2H) is used.
BOUND—Check Array Index Against Bounds

Description
BOUND determines if the first operand (array index) is within the bounds of an array specified the second operand (bounds operand). The array index is a signed integer located in a register. The bounds operand is a memory location that contains a pair of signed doubleword-integers (when the operand-size attribute is 32) or a pair of signed word-integers (when the operand-size attribute is 16). The first doubleword (or word) is the lower bound of the array and the second doubleword (or word) is the upper bound of the array. The array index must be greater than or equal to the lower bound and less than or equal to the upper bound plus the operand size in bytes. If the index is not within bounds, a BOUND range exceeded exception (#BR) is signaled. When this exception is generated, the saved return instruction pointer points to the BOUND instruction.

The bounds limit data structure (two words or doublewords containing the lower and upper limits of the array) is usually placed just before the array itself, making the limits addressable via a constant offset from the beginning of the array. Because the address of the array already will be present in a register, this practice avoids extra bus cycles to obtain the effective address of the array bounds.

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

Operation
IF 64bit Mode
THEN
  #UD;
ELSE
  IF (ArrayIndex < LowerBound OR ArrayIndex > UpperBound)
  (* Below lower bound or above upper bound *)
  THEN #BR; Fl;
FI;
Flags Affected
None.

Protected Mode Exceptions
#BR If the bounds test fails.
#UD If second operand is not a memory location.
If the LOCK prefix is used.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
#BR If the bounds test fails.
#UD If second operand is not a memory location.
If the LOCK prefix is used.
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual-8086 Mode Exceptions
#BR If the bounds test fails.
#UD If second operand is not a memory location.
If the LOCK prefix is used.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
BSF—Bit Scan Forward

Description
Searches the source operand (second operand) for the least significant set bit (1 bit). If a least significant 1 bit is found, its bit index is stored in the destination operand (first operand). The source operand can be a register or a memory location; the destination operand is a register. The bit index is an unsigned offset from bit 0 of the source operand. If the content of the source operand is 0, the content of the destination operand is undefined.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation
IF SRC = 0
THEN
    ZF ← 1;
    DEST is undefined;
ELSE
    ZF ← 0;
    temp ← 0;
    WHILE Bit(SRC, temp) = 0
    DO
        temp ← temp + 1;
        DEST ← temp;
    OD;
FI;

Flags Affected
The ZF flag is set to 1 if all the source operand is 0; otherwise, the ZF flag is cleared. The CF, OF, SF, AF, and PF, flags are undefined.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F BC /r</td>
<td>BSF r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Bit scan forward on r/m16.</td>
</tr>
<tr>
<td>0F BC /r</td>
<td>BSF r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Bit scan forward on r/m32.</td>
</tr>
<tr>
<td>REX.W + 0F BC</td>
<td>BSF r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Bit scan forward on r/m64.</td>
</tr>
</tbody>
</table>
Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
BSR—Bit Scan Reverse

Description

Searches the source operand (second operand) for the most significant set bit (1 bit). If a most significant 1 bit is found, its bit index is stored in the destination operand (first operand). The source operand can be a register or a memory location; the destination operand is a register. The bit index is an unsigned offset from bit 0 of the source operand. If the content source operand is 0, the content of the destination operand is undefined.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

IF SRC = 0
    THEN
        ZF ← 1;
        DEST is undefined;
    ELSE
        ZF ← 0;
        temp ← OperandSize - 1;
        WHILE Bit(SRC, temp) = 0
            temp ← temp - 1;
        OD
        DEST ← temp;
    FI;

Flags Affected

The ZF flag is set to 1 if all the source operand is 0; otherwise, the ZF flag is cleared. The CF, OF, SF, AF, and PF, flags are undefined.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F BD /r</td>
<td>BSR r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Bit scan reverse on r/m16.</td>
</tr>
<tr>
<td>0F BD /r</td>
<td>BSR r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Bit scan reverse on r/m32.</td>
</tr>
<tr>
<td>REX.W + 0F BD</td>
<td>BSR r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Bit scan reverse on r/m64.</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-M

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
#UD  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
#UD  If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.
BSWAP—Byte Swap

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F C8+rd</td>
<td>BSWAP r32</td>
<td>Valid*</td>
<td>Valid</td>
<td>Reverses the byte order of a 32-bit register.</td>
</tr>
<tr>
<td>REX.W + 0F C8+rd</td>
<td>BSWAP r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Reverses the byte order of a 64-bit register.</td>
</tr>
</tbody>
</table>

NOTES:
* See IA-32 Architecture Compatibility section below.

Description
Reverses the byte order of a 32-bit or 64-bit (destination) register. This instruction is provided for converting little-endian values to big-endian format and vice versa. To swap bytes in a word value (16-bit register), use the XCHG instruction. When the BSWAP instruction references a 16-bit register, the result is undefined.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

IA-32 Architecture Legacy Compatibility
The BSWAP instruction is not supported on IA-32 processors earlier than the Intel486™ processor family. For compatibility with this instruction, software should include functionally equivalent code for execution on Intel processors earlier than the Intel486 processor family.

Operation
TEMP ← DEST
IF 64-bit mode AND OperandSize = 64
THEN
    DEST[7:0] ← TEMP[63:56];
    DEST[15:8] ← TEMP[55:48];
    DEST[23:16] ← TEMP[47:40];
    DEST[39:32] ← TEMP[31:24];
    DEST[47:40] ← TEMP[23:16];
    DEST[55:48] ← TEMP[15:8];
    DEST[63:56] ← TEMP[7:0];
ELSE
    DEST[7:0] ← TEMP[31:24];
INSTRUCTION SET REFERENCE, A-M

DEST[15:8] ← TEMP[23:16];
DEST[23:16] ← TEMP[15:8];
DEST[31:24] ← TEMP[7:0];
FI;

Flags Affected
None.

Exceptions (All Operating Modes)
#UD If the LOCK prefix is used.
**BT—Bit Test**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F A3</td>
<td>BT r/m16, r16</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>0F A3</td>
<td>BT r/m32, r32</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>REX.W + 0F A3</td>
<td>BT r/m64, r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>0F BA /4 ib</td>
<td>BT r/m16, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>0F BA /4 ib</td>
<td>BT r/m32, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>REX.W + 0F BA /4 ib</td>
<td>BT r/m64, imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag.</td>
</tr>
</tbody>
</table>

**Description**

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset (specified by the second operand) and stores the value of the bit in the CF flag. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value:

- If the bit base operand specifies a register, the instruction takes the modulo 16, 32, or 64 of the bit offset operand (modulo size depends on the mode and register size; 64-bit operands are available only in 64-bit mode).
- If the bit base operand specifies a memory location, the operand represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The range of the bit position that can be referenced by the offset operand depends on the operand size.

See also: **Bit(BitBase, BitOffset)** on page 3-10.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. In this case, the low-order 3 or 5 bits (3 for 16-bit operands, 5 for 32-bit operands) of the immediate bit offset are stored in the immediate bit offset field, and the high-order bits are shifted and combined with the byte displacement in the addressing mode by the assembler. The processor will ignore the high order bits if they are not zero.

When accessing a bit in memory, the processor may access 4 bytes starting from the memory address for a 32-bit operand size, using by the following relationship:

\[ \text{Effective Address} + (4 \times (\text{BitOffset DIV 32})) \]
Or, it may access 2 bytes starting from the memory address for a 16-bit operand, using this relationship:

\[ \text{Effective Address} + (2 \times (\text{BitOffset DIV 16})) \]

It may do so even when only a single byte needs to be accessed to reach the given bit. When using this bit addressing mechanism, software should avoid referencing areas of memory close to address space holes. In particular, it should avoid references to memory-mapped I/O registers. Instead, software should use the MOV instructions to load from or store to these addresses, and use the register form of these instructions to manipulate the data.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bit operands. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[ \text{CF} \leftarrow \text{Bit(BitBase, BitOffset)} \]

**Flags Affected**

The CF flag contains the value of the selected bit. The OF, SF, ZF, AF, and PF flags are undefined.

**Protected Mode Exceptions**

- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- #UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.
- #UD If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
BTC—Bit Test and Complement

Description

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand), stores the value of the bit in the CF flag, and complements the selected bit in the bit string. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value:

- If the bit base operand specifies a register, the instruction takes the modulo 16, 32, or 64 of the bit offset operand (modulo size depends on the mode and register size; 64-bit operands are available only in 64-bit mode). This allows any bit position to be selected.
- If the bit base operand specifies a memory location, the operand represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The range of the bit position that can be referenced by the offset operand depends on the operand size.

See also: Bit(BitBase, BitOffset) on page 3-10.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. See ”BT—Bit Test” in this chapter for more information on this addressing mechanism.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX
prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\begin{align*}
CF & \leftarrow \text{Bit(BitBase, BitOffset)}; \\
\text{Bit(BitBase, BitOffset)} & \leftarrow \text{NOT Bit(BitBase, BitOffset)};
\end{align*}
\]

**Flags Affected**
The CF flag contains the value of the selected bit before it is complemented. The OF, SF, ZF, AF, and PF flags are undefined.

**Protected Mode Exceptions**
- **#GP(0)** If the destination operand points to a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**
- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS** If a memory operand effective address is outside the SS segment limit.
- **#UD** If the LOCK prefix is used but the destination is not a memory operand.

**Virtual-8086 Mode Exceptions**
- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
INSTRUCTION SET REFERENCE, A-M

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
BTR—Bit Test and Reset

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F B3</td>
<td>BTR r/m16, r16</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and clear.</td>
</tr>
<tr>
<td>0F B3</td>
<td>BTR r/m32, r32</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and clear.</td>
</tr>
<tr>
<td>REX.W + 0F B3</td>
<td>BTR r/m64, r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag and clear.</td>
</tr>
<tr>
<td>0F BA /6 ib</td>
<td>BTR r/m16, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and clear.</td>
</tr>
<tr>
<td>0F BA /6 ib</td>
<td>BTR r/m32, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and clear.</td>
</tr>
<tr>
<td>REX.W + 0F BA /6 ib</td>
<td>BTR r/m64, imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag and clear.</td>
</tr>
</tbody>
</table>

**DESCRIPTION**

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand), stores the value of the bit in the CF flag, and clears the selected bit in the bit string to 0. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value:

- If the bit base operand specifies a register, the instruction takes the modulo 16, 32, or 64 of the bit offset operand (modulo size depends on the mode and register size; 64-bit operands are available only in 64-bit mode). This allows any bit position to be selected.
- If the bit base operand specifies a memory location, the operand represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The range of the bit position that can be referenced by the offset operand depends on the operand size.

See also: Bit(BitBase, BitOffset) on page 3-10.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. See “BT—Bit Test” in this chapter for more information on this addressing mechanism.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX
prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\begin{align*}
CF & \leftarrow \text{Bit(BitBase, BitOffset)}; \\
\text{Bit(BitBase, BitOffset)} & \leftarrow 0;
\end{align*}
\]

**Flags Affected**
The CF flag contains the value of the selected bit before it is cleared. The OF, SF, ZF, AF, and PF flags are undefined.

**Protected Mode Exceptions**

- **#GP(0)** If the destination operand points to a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS** If a memory operand effective address is outside the SS segment limit.
- **#UD** If the LOCK prefix is used but the destination is not a memory operand.

**Virtual-8086 Mode Exceptions**

- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
BTS—Bit Test and Set

Description

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand), stores the value of the bit in the CF flag, and sets the selected bit in the bit string to 1. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value:

- If the bit base operand specifies a register, the instruction takes the modulo 16, 32, or 64 of the bit offset operand (modulo size depends on the mode and register size; 64-bit operands are available only in 64-bit mode). This allows any bit position to be selected.
- If the bit base operand specifies a memory location, the operand represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The range of the bit position that can be referenced by the offset operand depends on the operand size.

See also: Bit(BitBase, BitOffset) on page 3-10.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. See “BT—Bit Test” in this chapter for more information on this addressing mechanism.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX
prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\begin{align*}
CF & \leftarrow \text{Bit(BitBase, BitOffset)}; \\
\text{Bit(BitBase, BitOffset)} & \leftarrow 1;
\end{align*}
\]

**Flags Affected**

The CF flag contains the value of the selected bit before it is set. The OF, SF, ZF, AF, and PF flags are undefined.

**Protected Mode Exceptions**

- **#GP(0)** If the destination operand points to a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS** If a memory operand effective address is outside the SS segment limit.
- **#UD** If the LOCK prefix is used but the destination is not a memory operand.

**Virtual-8086 Mode Exceptions**

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
INSTRUCTION SET REFERENCE, A-M

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
**CALL—Call Procedure**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E8 cw</td>
<td>CALL rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Call near, relative, displacement relative to next instruction.</td>
</tr>
<tr>
<td>E8 cd</td>
<td>CALL rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Call near, relative, displacement relative to next instruction. 32-bit displacement sign extended to 64-bits in 64-bit mode.</td>
</tr>
<tr>
<td>FF /2</td>
<td>CALL r/m16</td>
<td>N.E.</td>
<td>Valid</td>
<td>Call near, absolute indirect, address given in r/m16.</td>
</tr>
<tr>
<td>FF /2</td>
<td>CALL r/m32</td>
<td>N.E.</td>
<td>Valid</td>
<td>Call near, absolute indirect, address given in r/m32.</td>
</tr>
<tr>
<td>FF /2</td>
<td>CALL r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Call near, absolute indirect, address given in r/m64.</td>
</tr>
<tr>
<td>9A cd</td>
<td>CALL ptr16:16</td>
<td>Invalid</td>
<td>Valid</td>
<td>Call far, absolute, address given in operand.</td>
</tr>
<tr>
<td>9A cp</td>
<td>CALL ptr16:32</td>
<td>Invalid</td>
<td>Valid</td>
<td>Call far, absolute, address given in operand.</td>
</tr>
<tr>
<td>FF /3</td>
<td>CALL m16:16</td>
<td>Valid</td>
<td>Valid</td>
<td>Call far, absolute indirect address given in m16:16. In 32-bit mode: if selector points to a gate, then RIP = 32-bit zero extended displacement taken from gate; else RIP = zero extended 16-bit offset from far pointer referenced in the instruction.</td>
</tr>
<tr>
<td>FF /3</td>
<td>CALL m16:32</td>
<td>Valid</td>
<td>Valid</td>
<td>In 64-bit mode: If selector points to a gate, then RIP = 64-bit displacement taken from gate; else RIP = zero extended 32-bit offset from far pointer referenced in the instruction.</td>
</tr>
<tr>
<td>REX.W + FF /3</td>
<td>CALL m16:64</td>
<td>Valid</td>
<td>N.E.</td>
<td>In 64-bit mode: If selector points to a gate, then RIP = 64-bit displacement taken from gate; else RIP = 64-bit offset from far pointer referenced in the instruction.</td>
</tr>
</tbody>
</table>

**Description**

Saves procedure linking information on the stack and branches to the called procedure specified using the target operand. The target operand specifies the address of
the first instruction in the called procedure. The operand can be an immediate value, a general-purpose register, or a memory location.

This instruction can be used to execute four types of calls:

• **Near Call** — A call to a procedure in the current code segment (the segment currently pointed to by the CS register), sometimes referred to as an intra-segment call.

• **Far Call** — A call to a procedure located in a different segment than the current code segment, sometimes referred to as an inter-segment call.

• **Inter-privilege-level far call** — A far call to a procedure in a segment at a different privilege level than that of the currently executing program or procedure.

• **Task switch** — A call to a procedure located in a different task.

The latter two call types (inter-privilege-level call and task switch) can only be executed in protected mode. See "Calling Procedures Using Call and RET" in Chapter 6 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for additional information on near, far, and inter-privilege-level calls. See Chapter 7, "Task Management," in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, for information on performing task switches with the CALL instruction.

**Near Call.** When executing a near call, the processor pushes the value of the EIP register (which contains the offset of the instruction following the CALL instruction) on the stack (for use later as a return-instruction pointer). The processor then branches to the address in the current code segment specified by the target operand. The target operand specifies either an absolute offset in the code segment (an offset from the base of the code segment) or a relative offset (a signed displacement relative to the current value of the instruction pointer in the EIP register; this value points to the instruction following the CALL instruction). The CS register is not changed on near calls.

For a near call absolute, an absolute offset is specified indirectly in a general-purpose register or a memory location (r/m16, r/m32, or r/m64). The operand-size attribute determines the size of the target operand (16, 32 or 64 bits). When in 64-bit mode, the operand size for near call (and all near branches) is forced to 64-bits. Absolute offsets are loaded directly into the EIP(RIP) register. If the operand size attribute is 16, the upper two bytes of the EIP register are cleared, resulting in a maximum instruction pointer size of 16 bits. When accessing an absolute offset indirectly using the stack pointer [ESP] as the base register, the base value used is the value of the ESP before the instruction executes.

A relative offset (rel16 or rel32) is generally specified as a label in assembly code. But at the machine code level, it is encoded as a signed, 16- or 32-bit immediate value. This value is added to the value in the EIP(RIP) register. In 64-bit mode the relative offset is always a 32-bit immediate value which is sign extended to 64-bits before it is added to the value in the RIP register for the target calculation. As with absolute offsets, the operand-size attribute determines the size of the target operand (16, 32,
or 64 bits). In 64-bit mode the target operand will always be 64-bits because the operand size is forced to 64-bits for near branches.

**Far Calls in Real-Address or Virtual-8086 Mode.** When executing a far call in real-address or virtual-8086 mode, the processor pushes the current value of both the CS and EIP registers on the stack for use as a return-instruction pointer. The processor then performs a “far branch” to the code segment and offset specified with the target operand for the called procedure. The target operand specifies an absolute far address either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). With the pointer method, the segment and offset of the called procedure is encoded in the instruction using a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address immediate. With the indirect method, the target operand specifies a memory location that contains a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address. The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The far address is loaded directly into the CS and EIP registers. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared.

**Far Calls in Protected Mode.** When the processor is operating in protected mode, the CALL instruction can be used to perform the following types of far calls:

- Far call to the same privilege level
- Far call to a different privilege level (inter-privilege level call)
- Task switch (far call to another task)

In protected mode, the processor always uses the segment selector part of the far address to access the corresponding descriptor in the GDT or LDT. The descriptor type (code segment, call gate, task gate, or TSS) and access rights determine the type of call operation to be performed.

If the selected descriptor is for a code segment, a far call to a code segment at the same privilege level is performed. (If the selected code segment is at a different privilege level and the code segment is non-conforming, a general-protection exception is generated.) A far call to the same privilege level in protected mode is very similar to one carried out in real-address or virtual-8086 mode. The target operand specifies an absolute far address either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The new code segment selector and its descriptor are loaded into CS register; the offset from the instruction is loaded into the EIP register.

A call gate (described in the next paragraph) can also be used to perform a far call to a code segment at the same privilege level. Using this mechanism provides an extra level of indirection and is the preferred method of making calls between 16-bit and 32-bit code segments.

When executing an inter-privilege-level far call, the code segment for the procedure being called must be accessed through a call gate. The segment selector specified by the target operand identifies the call gate. The target operand can specify the call gate segment selector either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). The processor obtains the
segment selector for the new code segment and the new instruction pointer (offset) from the call gate descriptor. (The offset from the target operand is ignored when a call gate is used.)

On inter-privilege-level calls, the processor switches to the stack for the privilege level of the called procedure. The segment selector for the new stack segment is specified in the TSS for the currently running task. The branch to the new code segment occurs after the stack switch. (Note that when using a call gate to perform a far call to a segment at the same privilege level, no stack switch occurs.) On the new stack, the processor pushes the segment selector and stack pointer for the calling procedure's stack, an optional set of parameters from the calling procedure's stack, and the segment selector and instruction pointer for the calling procedure's code segment. (A value in the call gate descriptor determines how many parameters to copy to the new stack.) Finally, the processor branches to the address of the procedure being called within the new code segment.

Executing a task switch with the CALL instruction is similar to executing a call through a call gate. The target operand specifies the segment selector of the task gate for the new task activated by the switch (the offset in the target operand is ignored). The task gate in turn points to the TSS for the new task, which contains the segment selectors for the task's code and stack segments. Note that the TSS also contains the EIP value for the next instruction that was to be executed before the calling task was suspended. This instruction pointer value is loaded into the EIP register to re-start the calling task.

The CALL instruction can also specify the segment selector of the TSS directly, which eliminates the indirection of the task gate. See Chapter 7, “Task Management,” in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, for information on the mechanics of a task switch.

When you execute a task switch with a CALL instruction, the nested task flag (NT) is set in the EFLAGS register and the new TSS's previous task link field is loaded with the old task's TSS selector. Code is expected to suspend this nested task by executing an IRET instruction which, because the NT flag is set, automatically uses the previous task link to return to the calling task. (See "Task Linking" in Chapter 7 of the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A*, for information on nested tasks.) Switching tasks with the CALL instruction differs in this regard from JMP instruction. JMP does not set the NT flag and therefore does not expect an IRET instruction to suspend the task.

**Mixing 16-Bit and 32-Bit Calls.** When making far calls between 16-bit and 32-bit code segments, use a call gate. If the far call is from a 32-bit code segment to a 16-bit code segment, the call should be made from the first 64 KBytes of the 32-bit code segment. This is because the operand-size attribute of the instruction is set to 16, so only a 16-bit return address offset can be saved. Also, the call should be made using a 16-bit call gate so that 16-bit values can be pushed on the stack. See Chapter 18, "Mixing 16-Bit and 32-Bit Code," in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A*, for more information.
Far Calls in Compatibility Mode. When the processor is operating in compatibility mode, the CALL instruction can be used to perform the following types of far calls:

- Far call to the same privilege level, remaining in compatibility mode
- Far call to the same privilege level, transitioning to 64-bit mode
- Far call to a different privilege level (inter-privilege level call), transitioning to 64-bit mode

Note that a CALL instruction can not be used to cause a task switch in compatibility mode since task switches are not supported in IA-32e mode.

In compatibility mode, the processor always uses the segment selector part of the far address to access the corresponding descriptor in the GDT or LDT. The descriptor type (code segment, call gate) and access rights determine the type of call operation to be performed.

If the selected descriptor is for a code segment, a far call to a code segment at the same privilege level is performed. (If the selected code segment is at a different privilege level and the code segment is non-conforming, a general-protection exception is generated.) A far call to the same privilege level in compatibility mode is very similar to one carried out in protected mode. The target operand specifies an absolute far address either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The new code segment selector and its descriptor are loaded into CS register and the offset from the instruction is loaded into the EIP register. The difference is that 64-bit mode may be entered. This specified by the L bit in the new code segment descriptor.

Note that a 64-bit call gate (described in the next paragraph) can also be used to perform a far call to a code segment at the same privilege level. However, using this mechanism requires that the target code segment descriptor have the L bit set, causing an entry to 64-bit mode.

When executing an inter-privilege-level far call, the code segment for the procedure being called must be accessed through a 64-bit call gate. The segment selector specified by the target operand identifies the call gate. The target operand can specify the call gate segment selector either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). The processor obtains the segment selector for the new code segment and the new instruction pointer (offset) from the 16-byte call gate descriptor. (The offset from the target operand is ignored when a call gate is used.)

On inter-privilege-level calls, the processor switches to the stack for the privilege level of the called procedure. The segment selector for the new stack segment is set to NULL. The new stack pointer is specified in the TSS for the currently running task. The branch to the new code segment occurs after the stack switch. (Note that when using a call gate to perform a far call to a segment at the same privilege level, an implicit stack switch occurs as a result of entering 64-bit mode. The SS selector is unchanged, but stack segment accesses use a segment base of 0x0, the limit is ignored, and the default stack size is 64-bits. The full value of RSP is used for the offset, of which the upper 32-bits are undefined.) On the new stack, the processor
pushes the segment selector and stack pointer for the calling procedure’s stack and the segment selector and instruction pointer for the calling procedure’s code segment. (Parameter copy is not supported in IA-32e mode.) Finally, the processor branches to the address of the procedure being called within the new code segment.

Near/(Far) Calls in 64-bit Mode. When the processor is operating in 64-bit mode, the CALL instruction can be used to perform the following types of far calls:

- Far call to the same privilege level, transitioning to compatibility mode
- Far call to the same privilege level, remaining in 64-bit mode
- Far call to a different privilege level (inter-privilege level call), remaining in 64-bit mode

Note that in this mode the CALL instruction can not be used to cause a task switch in 64-bit mode since task switches are not supported in IA-32e mode.

In 64-bit mode, the processor always uses the segment selector part of the far address to access the corresponding descriptor in the GDT or LDT. The descriptor type (code segment, call gate) and access rights determine the type of call operation to be performed.

If the selected descriptor is for a code segment, a far call to a code segment at the same privilege level is performed. (If the selected code segment is at a different privilege level and the code segment is non-conforming, a general-protection exception is generated.) A far call to the same privilege level in 64-bit mode is very similar to one carried out in compatibility mode. The target operand specifies an absolute far address indirectly with a memory location \((m16:16, m16:32\) or \(m16:64\)). The form of CALL with a direct specification of absolute far address is not defined in 64-bit mode. The operand-size attribute determines the size of the offset (16, 32, or 64 bits) in the far address. The new code segment selector and its descriptor are loaded into the CS register; the offset from the instruction is loaded into the EIP register. The new code segment may specify entry either into compatibility or 64-bit mode, based on the L bit value.

A 64-bit call gate (described in the next paragraph) can also be used to perform a far call to a code segment at the same privilege level. However, using this mechanism requires that the target code segment descriptor have the L bit set.

When executing an inter-privilege-level far call, the code segment for the procedure being called must be accessed through a 64-bit call gate. The segment selector specified by the target operand identifies the call gate. The target operand can only specify the call gate segment selector indirectly with a memory location \((m16:16, m16:32\) or \(m16:64\)). The processor obtains the segment selector for the new code segment and the new instruction pointer (offset) from the 16-byte call gate descriptor. (The offset from the target operand is ignored when a call gate is used.)

On inter-privilege-level calls, the processor switches to the stack for the privilege level of the called procedure. The segment selector for the new stack segment is set to NULL. The new stack pointer is specified in the TSS for the currently running task. The branch to the new code segment occurs after the stack switch.
Note that when using a call gate to perform a far call to a segment at the same privilege level, an implicit stack switch occurs as a result of entering 64-bit mode. The SS selector is unchanged, but stack segment accesses use a segment base of 0x0, the limit is ignored, and the default stack size is 64-bits. (The full value of RSP is used for the offset.) On the new stack, the processor pushes the segment selector and stack pointer for the calling procedure’s stack and the segment selector and instruction pointer for the calling procedure’s code segment. (Parameter copy is not supported in IA-32e mode.) Finally, the processor branches to the address of the procedure being called within the new code segment.

**Operation**

IF near call
    THEN IF near relative call
        THEN
            IF OperandSize = 64
                THEN
                    tempDEST ← SignExtend(DEST); (* DEST is rel32 *)
                    tempRIP ← RIP + tempDEST;
                    IF stack not large enough for a 8-byte return address
                        THEN #SS(0); Fi;
                    Push(RIP);
                    RIP ← tempRIP;
                    Fi;
            FI;
            IF OperandSize = 32
                THEN
                    tempEIP ← EIP + DEST; (* DEST is rel32 *)
                    IF tempEIP is not within code segment limit THEN #GP(0); Fi;
                    IF stack not large enough for a 4-byte return address
                        THEN #SS(0); Fi;
                    Push(EIP);
                    EIP ← tempEIP;
                    Fi;
            FI;
            IF OperandSize = 16
                THEN
                    tempEIP ← (EIP + DEST) AND 0000FFFFH; (* DEST is rel16 *)
                    IF tempEIP is not within code segment limit THEN #GP(0); Fi;
                    IF stack not large enough for a 2-byte return address
                        THEN #SS(0); Fi;
                    Push(IP);
                    EIP ← tempEIP;
                    Fi;
            ELSE (* Near absolute call *)
                IF OperandSize = 64
THEN
   tempRIP ← DEST; (* DEST is r/m64 *)
   IF stack not large enough for a 8-byte return address
      THEN #SS(0); FI;
   Push(RIP);
   RIP ← tempRIP;
   FI;
   IF OperandSize = 32
      THEN
         tempEIP ← DEST; (* DEST is r/m32 *)
         IF tempEIP is not within code segment limit THEN #GP(0); FI;
         IF stack not large enough for a 4-byte return address
            THEN #SS(0); FI;
         Push(EIP);
         EIP ← tempEIP;
      FI;
      IF OperandSize = 16
         THEN
            tempEIP ← DEST AND 0000FFFFH; (* DEST is r/m16 *)
            IF tempEIP is not within code segment limit THEN #GP(0); FI;
            IF stack not large enough for a 2-byte return address
               THEN #SS(0); FI;
            Push(IP);
            EIP ← tempEIP;
         FI;
      FI;
   IF far call and (PE = 0 or (PE = 1 and VM = 1)) (* Real-address or virtual-8086 mode *)
      THEN
         IF OperandSize = 32
            THEN
               IF stack not large enough for a 6-byte return address
                  THEN #SS(0); FI;
               IF DEST[31:16] is not zero THEN #GP(0); FI;
               Push(CS); (* Padded with 16 high-order bits *)
               Push(EIP);
               CS ← DEST[47:32]; (* DEST is ptr16:32 or [m16:32] *)
               EIP ← DEST[31:0]; (* DEST is ptr16:32 or [m16:32] *)
            ELSE (* OperandSize = 16 *)
               IF stack not large enough for a 4-byte return address
                  THEN #SS(0); FI;
               Push(CS);
   FI;rel/abs
   FI; near
Push(IP);
CS ← DEST[31:16]; (* DEST is \textit{ptr16:16} or \textit{[m16:16]} *)
EIP ← DEST[15:0]; (* DEST is \textit{ptr16:16} or \textit{[m16:16]}; clear upper 16 bits *)
FI;
FI;

IF far call and (PE = 1 and VM = 0) (* Protected mode or IA-32e Mode, not virtual-8086 mode*)
THEN
  IF segment selector in target operand NULL
  THEN #GP(0); FI;
  IF segment selector index not within descriptor table limits
  THEN #GP(new code segment selector); FI;
  Read type and access rights of selected segment descriptor;
  IF IA32_EFER.LMA = 0
  THEN
    IF segment type is not a conforming or nonconforming code segment, call
gate, task gate, or TSS
    THEN #GP(segment selector); FI;
  ELSE
    IF segment type is not a conforming or nonconforming code segment or
64-bit call gate,
    THEN #GP(segment selector); FI;
  FI;
  Depending on type and access rights:
  GO TO CONFORMING-CODE-SEGMENT;
  GO TO NONCONFORMING-CODE-SEGMENT;
  GO TO CALL-GATE;
  GO TO TASK-GATE;
  GO TO TASK-STATE-SEGMENT;
FI;

CONFORMING-CODE-SEGMENT:
  IF L-Bit = 1 and D-BIT = 1 and IA32_EFER.LMA = 1
  THEN GP(new code segment selector); FI;
  IF DPL > CPL
  THEN #GP(new code segment selector); FI;
  IF segment not present
  THEN #NP(new code segment selector); FI;
  IF stack not large enough for return address
  THEN #SS(0); FI;
  tempEIP ← DEST(Offset);
  IF OperandSize = 16
  THEN

CALL—Call Procedure
tempEIP ← tempEIP AND 0000FFFFH; Fl; (* Clear upper 16 bits *)
IF (EFER.LMA = 0 or target mode = Compatibility mode) and (tempEIP outside new code
segment limit)
    THEN #GP(O); Ff;
IF tempEIP is non-canonical
    THEN #GP(O); Ff;
IF OperandSize = 32
    THEN
        Push(CS); (* Padded with 16 high-order bits *)
        Push(EIP);
        CS ← DEST(CodeSegmentSelector);
        (* Segment descriptor information also loaded *)
        CS(RPL) ← CPL;
        EIP ← tempEIP;
    ELSE
        IF OperandSize = 16
            THEN
                Push(CS);
                Push(IP);
                CS ← DEST(CodeSegmentSelector);
                (* Segment descriptor information also loaded *)
                CS(RPL) ← CPL;
                EIP ← tempEIP;
            ELSE (* OperandSize = 64 *)
                Push(CS); (* Padded with 48 high-order bits *)
                Push(RIP);
                CS ← DEST(CodeSegmentSelector);
                (* Segment descriptor information also loaded *)
                CS(RPL) ← CPL;
                RIP ← tempEIP;
            FI;
        FI;
    END;

NONCONFORMING-CODE-SEGMENT:
    IF L-Bit = 1 and D-BIT = 1 and IA32_EFER.LMA = 1
        THEN GP(new code segment selector); Fl;
    IF (RPL > CPL) or (DPL ≠ CPL)
        THEN #GP(new code segment selector); Fl;
    IF segment not present
        THEN #NP(new code segment selector); Fl;
    IF stack not large enough for return address
        THEN #SS(O); Fl;
tempEIP ← DEST(Offset);
IF OperandSize = 16
    THEN tempEIP ← tempEIP AND 0000FFFFH; FI; (* Clear upper 16 bits *)
IF (EFER.LMA = 0 or target mode = Compatibility mode) and (tempEIP outside new code
    segment limit)
    THEN #GP(0); FI;
IF tempEIP is non-canonical
    THEN #GP(0); FI;
IF OperandSize = 32
    THEN
        Push(CS); (* Padded with 16 high-order bits *)
        Push(EIP);
        CS ← DEST(CodeSegmentSelector);
        (* Segment descriptor information also loaded *)
        CS(RPL) ← CPL;
        EIP ← tempEIP;
    ELSE
        IF OperandSize = 16
            THEN
                Push(CS);
                Push(IP);
                CS ← DEST(CodeSegmentSelector);
                (* Segment descriptor information also loaded *)
                CS(RPL) ← CPL;
                EIP ← tempEIP;
            ELSE (* OperandSize = 64 *)
                Push(CS); (* Padded with 48 high-order bits *)
                Push(RIP);
                CS ← DEST(CodeSegmentSelector);
                (* Segment descriptor information also loaded *)
                CS(RPL) ← CPL;
                RIP ← tempEIP;
        FI;
    FI;
END;

CALL-GATE:
    IF call gate (DPL < CPL) or (RPL > DPL)
        THEN #GP(call gate selector); FI;
    IF call gate not present
        THEN #NP(call gate selector); FI;
    IF call gate code-segment selector is NULL
        THEN #GP(0); FI;
    IF call gate code-segment selector index is outside descriptor table limits
THEN #GP(code segment selector); Fl;
Read code segment descriptor;
IF code-segment segment descriptor does not indicate a code segment
or code-segment segment descriptor DPL > CPL
THEN #GP(code segment selector); Fl;
IF IA32_EFER.LMA = 1 AND (code-segment segment descriptor is
not a 64-bit code segment or code-segment descriptor has both L-Bit and D-bit set)
THEN #GP(code segment selector); Fl;
IF code segment not present
THEN #NP(new code segment selector); Fl;
IF code segment is non-conforming and DPL < CPL
THEN go to MORE-PRIVILEGE;
ELSE go to SAME-PRIVILEGE;
Fl;
END;

MORE-PRIVILEGE:
IF current TSS is 32-bit TSS
THEN
    TSSstackAddress ← new code segment (DPL ∗ 8) + 4;
    IF (TSSstackAddress + 7) > TSS limit
        THEN #TS(current TSS selector); Fl;
    newSS ← TSSstackAddress + 4;
    newESP ← stack address;
    ELSE
        IF current TSS is 16-bit TSS
            THEN
                TSSstackAddress ← new code segment (DPL ∗ 4) + 2;
                IF (TSSstackAddress + 4) > TSS limit
                    THEN #TS(current TSS selector); Fl;
                newESP ← TSSstackAddress;
                newSS ← TSSstackAddress + 2;
            ELSE (* TSS is 64-bit *)
                TSSstackAddress ← new code segment (DPL ∗ 8) + 4;
                IF (TSSstackAddress + 8) > TSS limit
                    THEN #TS(current TSS selector); Fl;
                newESP ← TSSstackAddress;
                newSS ← CodeSegment (DPL);
                (* null selector with RPL = new CPL *)
            Fl;
        ELSE
            IF IA32_EFER.LMA = 0 and stack segment selector = NULL
                THEN #TS(stack segment selector); Fl;
            Read code segment descriptor;
IF IA32_EFER.LMA = 0 and (stack segment selector’s RPL ≠ DPL of code segment or stack segment DPL ≠ DPL of code segment or stack segment is not a writable data segment)  
   THEN #TS(SS selector); FI
IF IA32_EFER.LMA = 0 and stack segment not present  
   THEN #SS(SS selector); FI;
IF CallGateSize = 32  
   THEN  
      IF stack does not have room for parameters plus 16 bytes  
         THEN #SS(SS selector); FI;  
      IF CallGate(InstructionPointer) not within code segment limit  
         THEN #GP(0); FI;  
      SS ← newSS;  
         (* Segment descriptor information also loaded *)  
      ESP ← newESP;  
      CS:IP ← CallGate(CS:InstructionPointer);  
         (* Segment descriptor information also loaded *)  
      Push(oldSS:oldESP); (* From calling procedure *)  
      temp ← parameter count from call gate, masked to 5 bits;  
      Push(parameters from calling procedure's stack, temp)  
      Push(oldCS:oldEIP); (* Return address to calling procedure *)
ELSE
   IF CallGateSize = 16  
      THEN  
         IF stack does not have room for parameters plus 8 bytes  
            THEN #SS(SS selector); FI;  
         IF (CallGate(InstructionPointer) AND FFFFH) not in code segment limit  
            THEN #GP(0); FI;  
         SS ← newSS;  
            (* Segment descriptor information also loaded *)  
         ESP ← newESP;  
         CS:IP ← CallGate(CS:InstructionPointer);  
            (* Segment descriptor information also loaded *)  
         Push(oldSS:oldESP); (* From calling procedure *)  
         temp ← parameter count from call gate, masked to 5 bits;  
         Push(parameters from calling procedure’s stack, temp)  
         Push(oldCS:oldEIP); (* Return address to calling procedure *)
ELSE (* CallGateSize = 64 *)  
   IF pushing 32 bytes on the stack touches non-canonical addresses  
      THEN #SS(SS selector); FI;  
   IF (CallGate(InstructionPointer) is non-canonical)  
      THEN #GP(0); FI;  
   SS ← newSS; (* New SS is NULL)  
   RSP ← newESP;
CALL—Call Procedure

INSTRUCTION SET REFERENCE, A-M

CS:IP ← CallGate(CS:InstructionPointer);
(* Segment descriptor information also loaded *)
Push(oldSS:oldESP); (* From calling procedure *)
Push(oldCS:oldEIP); (* Return address to calling procedure *)

FI;
FI;
CPL ← CodeSegment(DPL)
CS(RPL) ← CPL
END;

SAME-PRIVILEGE:
IF CallGateSize = 32
THEN
IF stack does not have room for 8 bytes
THEN #SS(0); FI;
IF CallGate(InstructionPointer) not within code segment limit
THEN #GP(0); FI;
CS:EIP ← CallGate(CS:EIP) (* Segment descriptor information also loaded *)
Push(oldCS:oldEIP); (* Return address to calling procedure *)
ELSE
If CallGateSize = 16
THEN
IF stack does not have room for 4 bytes
THEN #SS(0); FI;
IF CallGate(InstructionPointer) not within code segment limit
THEN #GP(0); FI;
CS:IP ← CallGate(CS:instruction pointer);
(* Segment descriptor information also loaded *)
Push(oldCS:oldIP); (* Return address to calling procedure *)
ELSE (* CallGateSize = 64)
IF pushing 16 bytes on the stack touches non-canonical addresses
THEN #SS(0); FI;
IF RIP non-canonical
THEN #GP(0); FI;
CS:IP ← CallGate(CS:instruction pointer);
(* Segment descriptor information also loaded *)
Push(oldCS:oldIP); (* Return address to calling procedure *)
FI;
FI;
CS(RPL) ← CPL
END;

TASK-GATE:
CALL—Call Procedure

IF task gate DPL < CPL or RPL
    THEN #GP(task gate selector); Fl;
IF task gate not present
    THEN #NP(task gate selector); Fl;
Read the TSS segment selector in the task-gate descriptor;
IF TSS segment selector local/global bit is set to local
or index not within GDT limits
    THEN #GP(TSS selector); Fl;
Access TSS descriptor in GDT;
IF TSS descriptor specifies that the TSS is busy (low-order 5 bits set to 00001)
    THEN #GP(TSS selector); Fl;
IF TSS not present
    THEN #NP(TSS selector); Fl;
SWITCH-TASKS (with nesting) to TSS;
IF EIP not within code segment limit
    THEN #GP(0); Fl;
END;

TASK-STATE-SEGMENT:
IF TSS DPL < CPL or RPL
    or TSS descriptor indicates TSS not available
    THEN #GP(TSS selector); Fl;
IF TSS is not present
    THEN #NP(TSS selector); Fl;
SWITCH-TASKS (with nesting) to TSS;
IF EIP not within code segment limit
    THEN #GP(0); Fl;
END;

Flags Affected
All flags are affected if a task switch occurs; no flags are affected if a task switch does not occur.

Protected Mode Exceptions

#GP(0)  If the target offset in destination operand is beyond the new code segment limit.
        If the segment selector in the destination operand is NULL.
        If the code segment selector in the gate is NULL.
        If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#GP(selector) If a code segment or gate or TSS selector index is outside descriptor table limits.

If the segment descriptor pointed to by the segment selector in the destination operand is not for a conforming-code segment, nonconforming-code segment, call gate, task gate, or task state segment.

If the DPL for a nonconforming-code segment is not equal to the CPL or the RPL for the segment’s segment selector is greater than the CPL.

If the DPL for a conforming-code segment is greater than the CPL.

If the DPL from a call-gate, task-gate, or TSS segment descriptor is less than the CPL or than the RPL of the call-gate, task-gate, or TSS’s segment selector.

If the segment descriptor for a segment selector from a call gate does not indicate it is a code segment.

If the segment selector from a call gate is beyond the descriptor table limits.

If the DPL for a code-segment obtained from a call gate is greater than the CPL.

If the segment selector for a TSS has its local/global bit set for local.

If a TSS segment descriptor specifies that the TSS is busy or not available.

#SS(0) If pushing the return address, parameters, or stack segment pointer onto the stack exceeds the bounds of the stack segment, when no stack switch occurs.

If a memory operand effective address is outside the SS segment limit.

#SS(selector) If pushing the return address, parameters, or stack segment pointer onto the stack exceeds the bounds of the stack segment, when a stack switch occurs.

If the SS register is being loaded as part of a stack switch and the segment pointed to is marked not present.

If stack segment does not have room for the return address, parameters, or stack segment pointer, when stack switch occurs.

#NP(selector) If a code segment, data segment, stack segment, call gate, task gate, or TSS is not present.

#TS(selector) If the new stack segment selector and ESP are beyond the end of the TSS.
If the new stack segment selector is NULL.
If the RPL of the new stack segment selector in the TSS is not equal to the DPL of the code segment being accessed.
If DPL of the stack segment descriptor for the new stack segment is not equal to the DPL of the code segment descriptor.
If the new stack segment is not a writable data segment.
If segment-selector index for stack segment is outside descriptor table limits.

#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the target offset is beyond the code segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the target offset is beyond the code segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
#GP(selector) If a memory address accessed by the selector is in non-canonical space.
#GP(0) If the target offset in the destination operand is non-canonical.

64-Bit Mode Exceptions
#GP(0) If a memory address is non-canonical.
If target offset in destination operand is non-canonical.
If the segment selector in the destination operand is NULL.
If the code segment selector in the 64-bit gate is NULL.
#GP(selector) If code segment or 64-bit call gate is outside descriptor table limits.
If code segment or 64-bit call gate overlaps non-canonical space.
If the segment descriptor pointed to by the segment selector in the destination operand is not for a conforming-code segment, nonconforming-code segment, or 64-bit call gate.
If the segment descriptor pointed to by the segment selector in the destination operand is a code segment and has both the D-bit and the L-bit set.
If the DPL for a nonconforming-code segment is not equal to the CPL, or the RPL for the segment’s segment selector is greater than the CPL.
If the DPL for a conforming-code segment is greater than the CPL.
If the DPL from a 64-bit call-gate is less than the CPL or than the RPL of the 64-bit call-gate.
If the upper type field of a 64-bit call gate is not 0x0.
If the segment selector from a 64-bit call gate is beyond the descriptor table limits.
If the DPL for a code-segment obtained from a 64-bit call gate is greater than the CPL.
If the code segment descriptor pointed to by the selector in the 64-bit gate doesn’t have the L-bit set and the D-bit clear.
If the segment descriptor for a segment selector from the 64-bit call gate does not indicate it is a code segment.

#SS(0) If pushing the return offset or CS selector onto the stack exceeds the bounds of the stack segment when no stack switch occurs.
If a memory operand effective address is outside the SS segment limit.
If the stack address is in a non-canonical form.

#SS(selector) If pushing the old values of SS selector, stack pointer, EFLAGS, CS selector, offset, or error code onto the stack violates the canonical boundary when a stack switch occurs.

#NP(selector) If a code segment or 64-bit call gate is not present.
#TS(selector) If the load of the new RSP exceeds the limit of the TSS.
#UD (64-bit mode only) If a far call is direct to an absolute address in memory.
If the LOCK prefix is used.

#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
**CBW/CWDE/CDQE—Convert Byte to Word/Convert Word to Doubleword/Convert Doubleword to Quadword**

**Description**

Double the size of the source operand by means of sign extension. The CBW (convert byte to word) instruction copies the sign (bit 7) in the source operand into every bit in the AH register. The CWDE (convert word to doubleword) instruction copies the sign (bit 15) of the word in the AX register into the high 16 bits of the EAX register.

CBW and CWDE reference the same opcode. The CBW instruction is intended for use when the operand-size attribute is 16; CWDE is intended for use when the operand-size attribute is 32. Some assemblers may force the operand size. Others may treat these two mnemonics as synonyms (CBW/CWDE) and use the setting of the operand-size attribute to determine the size of values to be converted.

In 64-bit mode, the default operation size is the size of the destination register. Use of the REX.W prefix promotes this instruction (CDQE when promoted) to operate on 64-bit operands. In which case, CDQE copies the sign (bit 31) of the doubleword in the EAX register into the high 32 bits of RAX.

**Operation**

IF OperandSize = 16 (* Instruction = CBW *)

THEN

\[ AX \leftarrow \text{SignExtend}(AL); \]

ELSE IF (OperandSize = 32, Instruction = CWDE)

\[ EAX \leftarrow \text{SignExtend}(AX); \]

ELSE (* 64-Bit Mode, OperandSize = 64, Instruction = CDQE*)

\[ RAX \leftarrow \text{SignExtend}(EAX); \]

FI;

**Flags Affected**

None.

**Exceptions (All Operating Modes)**

#UD If the LOCK prefix is used.
CLC—Clear Carry Flag

Description
Clears the CF flag in the EFLAGS register. Operation is the same in all non-64-bit modes and 64-bit mode.

Operation
CF ← 0;

Flags Affected
The CF flag is set to 0. The OF, ZF, SF, AF, and PF flags are unaffected.

Exceptions (All Operating Modes)
#UD If the LOCK prefix is used.
CLD—Clear Direction Flag

Description
Clears the DF flag in the EFLAGS register. When the DF flag is set to 0, string operations increment the index registers (ESI and/or EDI). Operation is the same in all non-64-bit modes and 64-bit mode.

Operation
DF ← 0;

Flags Affected
The DF flag is set to 0. The CF, OF, ZF, SF, AF, and PF flags are unaffected.

Exceptions (All Operating Modes)
#UD If the LOCK prefix is used.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC</td>
<td>CLD</td>
<td>Valid</td>
<td>Valid</td>
<td>Clear DF flag.</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-M

CLFLUSH—Flush Cache Line

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AE /7</td>
<td>CLFLUSH m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Flushes cache line containing m8.</td>
</tr>
</tbody>
</table>

**Description**

Invalidates the cache line that contains the linear address specified with the source operand from all levels of the processor cache hierarchy (data and instruction). The invalidation is broadcast throughout the cache coherence domain. If, at any level of the cache hierarchy, the line is inconsistent with memory (dirty) it is written to memory before invalidation. The source operand is a byte memory location.

The availability of CLFLUSH is indicated by the presence of the CPUID feature flag CLFSH (bit 19 of the EDX register, see “CPUID—CPU Identification” in this chapter). The aligned cache line size affected is also indicated with the CPUID instruction (bits 8 through 15 of the EBX register when the initial value in the EAX register is 1).

The memory attribute of the page containing the affected line has no effect on the behavior of this instruction. It should be noted that processors are free to speculatively fetch and cache data from system memory regions assigned a memory-type allowing for speculative reads (such as, the WB, WC, and WT memory types). PREFETCHh instructions can be used to provide the processor with hints for this speculative behavior. Because this speculative fetching can occur at any time and is not tied to instruction execution, the CLFLUSH instruction is not ordered with respect to PREFETCHh instructions or any of the speculative fetching mechanisms (that is, data can be speculatively loaded into a cache line just before, during, or after the execution of a CLFLUSH instruction that references the cache line).

CLFLUSH is only ordered by the MFENCE instruction. It is not guaranteed to be ordered by any other fencing or serializing instructions or by another CLFLUSH instruction. For example, software can use an MFENCE instruction to insure that previous stores are included in the write-back.

The CLFLUSH instruction can be used at all privilege levels and is subject to all permission checking and faults associated with a byte load (and in addition, a CLFLUSH instruction is allowed to flush a linear address in an execute-only segment). Like a load, the CLFLUSH instruction sets the A bit but not the D bit in the page tables.

The CLFLUSH instruction was introduced with the SSE2 extensions; however, because it has its own CPUID feature flag, it can be implemented in IA-32 processors that do not include the SSE2 extensions. Also, detecting the presence of the SSE2 extensions with the CPUID instruction does not guarantee that the CLFLUSH instruction is implemented in the processor.

CLFLUSH operation is the same in non-64-bit modes and 64-bit mode.
Instruction Set Reference, A-M

Operation
Flush_Cache_Line(SRC);

Intel C/C++ Compiler Intrinsic Equivalents
CLFLUSH void _mm_clflush(void const *p)

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS,
ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#UD If CPUID.01H:EDX.CLF[bit 19] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address
space from 0 to FFFFH.
#UD If CPUID.01H:EDX.CLF[bit 19] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-
canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#UD If CPUID.01H:EDX.CLF[bit 19] = 0.
If the LOCK prefix is used.
CLI — Clear Interrupt Flag

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FA</td>
<td>CLI</td>
<td>Valid</td>
<td>Valid</td>
<td>Clear interrupt flag; interrupts disabled when interrupt flag cleared.</td>
</tr>
</tbody>
</table>

**Description**

If protected-mode virtual interrupts are not enabled, CLI clears the IF flag in the EFLAGS register. No other flags are affected. Clearing the IF flag causes the processor to ignore maskable external interrupts. The IF flag and the CLI and STI instruction have no affect on the generation of exceptions and NMI interrupts.

When protected-mode virtual interrupts are enabled, CPL is 3, and IOPL is less than 3; CLI clears the VIF flag in the EFLAGS register, leaving IF unaffected. Table 3-14 indicates the action of the CLI instruction depending on the processor operating mode and the CPL/IOPL of the running program or procedure.

CLI operation is the same in non-64-bit modes and 64-bit mode.

**Table 3-14. Decision Table for CLI Results**

<table>
<thead>
<tr>
<th>PE</th>
<th>VM</th>
<th>IOPL</th>
<th>CPL</th>
<th>PVI</th>
<th>VIP</th>
<th>VME</th>
<th>CLI Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>IF = 0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>≥ CPL</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>IF = 0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>3</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>VIF = 0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>GP Fault</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>GP Fault</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>IF = 0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>VIF = 0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>GP Fault</td>
</tr>
</tbody>
</table>

**NOTES:**

* X = This setting has no impact.

**Operation**

IF PE = 0
THEN
  IF ← 0; (* Reset Interrupt Flag *)
ELSE
  IF VM = 0;
  THEN
Flags Affected

If protected-mode virtual interrupts are not enabled, IF is set to 0 if the CPL is equal to or less than the IOPL; otherwise, it is not affected. The other flags in the EFLAGS register are unaffected.

When protected-mode virtual interrupts are enabled, CPL is 3, and IOPL is less than 3; CLI clears the VIF flag in the EFLAGS register, leaving IF unaffected.

Protected Mode Exceptions

#GP(0) If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#UD If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0) If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0) If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.

#UD If the LOCK prefix is used.
CLTS—Clear Task-Switched Flag in CR0

Description
Clears the task-switched (TS) flag in the CR0 register. This instruction is intended for use in operating-system procedures. It is a privileged instruction that can only be executed at a CPL of 0. It is allowed to be executed in real-address mode to allow initialization for protected mode.

The processor sets the TS flag every time a task switch occurs. The flag is used to synchronize the saving of FPU context in multitasking applications. See the description of the TS flag in the section titled “Control Registers” in Chapter 2 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, for more information about this flag.

CLTS operation is the same in non-64-bit modes and 64-bit mode.

See Chapter 22, “VMX Non-Root Operation,” of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*, for more information about the behavior of this instruction in VMX non-root operation.

Operation

```
CR0.TS[bit 3] ← 0;
```

Flags Affected

The TS flag in CR0 register is cleared.

Protected Mode Exceptions

- #GP(0) If the current privilege level is not 0.
- #UD If the LOCK prefix is used.

Real-Address Mode Exceptions

- #UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

- #GP(0) CLTS is not recognized in virtual-8086 mode.
- #UD If the LOCK prefix is used.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 06</td>
<td>CLTS</td>
<td>Valid</td>
<td>Valid</td>
<td>Clears TS flag in CR0.</td>
</tr>
</tbody>
</table>
CLTS—Clear Task-Switched Flag in CR0

INSTRUCTION SET REFERENCE, A-M

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

- **#GP(0)**  
  If the CPL is greater than 0.
- **#UD**  
  If the LOCK prefix is used.
CMC—Complement Carry Flag

Description
Complements the CF flag in the EFLAGS register. CMC operation is the same in non-64-bit modes and 64-bit mode.

Operation
EFLAGS.CF[bit 0] ← NOT EFLAGS.CF[bit 0];

Flags Affected
The CF flag contains the complement of its original value. The OF, ZF, SF, AF, and PF flags are unaffected.

Exceptions (All Operating Modes)
#UD If the LOCK prefix is used.
### CMOVcc—Conditional Move

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 47 /r</td>
<td>CMOVA r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>0F 47 /r</td>
<td>CMOVA r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 47 /r</td>
<td>CMOVA r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>0F 43 /r</td>
<td>CMOVAE r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if above or equal (CF=0).</td>
</tr>
<tr>
<td>0F 43 /r</td>
<td>CMOVAE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if above or equal (CF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 43 /r</td>
<td>CMOVAE r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if above or equal (CF=0).</td>
</tr>
<tr>
<td>0F 42 /r</td>
<td>CMOVB r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below (CF=1).</td>
</tr>
<tr>
<td>0F 42 /r</td>
<td>CMOVB r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below (CF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 42 /r</td>
<td>CMOVB r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if below (CF=1).</td>
</tr>
<tr>
<td>0F 46 /r</td>
<td>CMOVBE r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>0F 46 /r</td>
<td>CMOVBE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 46 /r</td>
<td>CMOVBE r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>0F 42 /r</td>
<td>CMOV C r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if carry (CF=1).</td>
</tr>
<tr>
<td>0F 42 /r</td>
<td>CMOV C r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if carry (CF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 42 /r</td>
<td>CMOV C r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if carry (CF=1).</td>
</tr>
<tr>
<td>0F 44 /r</td>
<td>CMOVE r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if equal (ZF=1).</td>
</tr>
<tr>
<td>0F 44 /r</td>
<td>CMOVE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if equal (ZF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 44 /r</td>
<td>CMOVE r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if equal (ZF=1).</td>
</tr>
<tr>
<td>0F 4F /r</td>
<td>CMOVG r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if greater (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>0F 4F /r</td>
<td>CMOVG r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if greater (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>REX.W + 0F 4F /r</td>
<td>CMOVG r64, r/m64</td>
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<td>N.E.</td>
<td>Move if greater (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>0F 4D /r</td>
<td>CMOVGE r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if greater or equal (SF=OF).</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>64-Bit Mode</td>
<td>Compat/ Leg Mode</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>-------------------</td>
<td>-------------</td>
<td>------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>0F 4D  /r</td>
<td>CMOVGE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if greater or equal (SF=OF).</td>
</tr>
<tr>
<td>REX.W + 0F 4D /r</td>
<td>CMOVGE r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if greater or equal (SF=OF).</td>
</tr>
<tr>
<td>0F 4C  /r</td>
<td>CMOVL r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if less (SF≠ OF).</td>
</tr>
<tr>
<td>0F 4C  /r</td>
<td>CMOVL r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if less (SF≠ OF).</td>
</tr>
<tr>
<td>REX.W + 0F 4C /r</td>
<td>CMOVL r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if less (SF≠ OF).</td>
</tr>
<tr>
<td>0F 4E  /r</td>
<td>CMOVLE r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if less or equal (ZF=1 or SF≠ OF).</td>
</tr>
<tr>
<td>0F 4E  /r</td>
<td>CMOVLE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if less or equal (ZF=1 or SF≠ OF).</td>
</tr>
<tr>
<td>REX.W + 0F 4E /r</td>
<td>CMOVLE r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if less or equal (ZF=1 or SF≠ OF).</td>
</tr>
<tr>
<td>0F 46  /r</td>
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<td>Valid</td>
<td>Valid</td>
<td>Move if not above (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>0F 46  /r</td>
<td>CMOVNA r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not above (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 46 /r</td>
<td>CMOVNA r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not above (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>0F 42  /r</td>
<td>CMOVNAE r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not above or equal (CF=1).</td>
</tr>
<tr>
<td>0F 42  /r</td>
<td>CMOVNAE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not above or equal (CF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 42 /r</td>
<td>CMOVNAE r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not above or equal (CF=1).</td>
</tr>
<tr>
<td>0F 43  /r</td>
<td>CMOVNB r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not below (CF=0).</td>
</tr>
<tr>
<td>0F 43  /r</td>
<td>CMOVNB r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not below (CF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 43 /r</td>
<td>CMOVNB r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not below (CF=0).</td>
</tr>
<tr>
<td>0F 47  /r</td>
<td>CMOVNBE r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not below or equal (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>0F 47  /r</td>
<td>CMOVNBE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not below or equal (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 47 /r</td>
<td>CMOVNBE r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not below or equal (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>64-Bit Mode</td>
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<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>----------------</td>
<td>-------------</td>
<td>-----------------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>0F 43 /r</td>
<td>CMOVNC r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not carry (CF=0).</td>
</tr>
<tr>
<td>0F 43 /r</td>
<td>CMOVNC r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not carry (CF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 43 /r</td>
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<td>Valid</td>
<td>N.E.</td>
<td>Move if not carry (CF=0).</td>
</tr>
<tr>
<td>0F 45 /r</td>
<td>CMOVNE r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not equal (ZF=0).</td>
</tr>
<tr>
<td>0F 45 /r</td>
<td>CMOVNE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not equal (ZF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 45 /r</td>
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<td>Valid</td>
<td>N.E.</td>
<td>Move if not equal (ZF=0).</td>
</tr>
<tr>
<td>0F 4E /r</td>
<td>CMOVNG r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not greater (ZF=1 or SF≠OF).</td>
</tr>
<tr>
<td>0F 4E /r</td>
<td>CMOVNG r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not greater (ZF=1 or SF≠OF).</td>
</tr>
<tr>
<td>REX.W + 0F 4E /r</td>
<td>CMOVNG r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not greater (ZF=1 or SF≠OF).</td>
</tr>
<tr>
<td>0F 4C /r</td>
<td>CMOVNGE r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not greater or equal (SF≠OF).</td>
</tr>
<tr>
<td>0F 4C /r</td>
<td>CMOVNGE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not greater or equal (SF≠OF).</td>
</tr>
<tr>
<td>REX.W + 0F 4C /r</td>
<td>CMOVNGE r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not greater or equal (SF≠OF).</td>
</tr>
<tr>
<td>0F 4D /r</td>
<td>CMOVNL r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not less (SF=OF).</td>
</tr>
<tr>
<td>0F 4D /r</td>
<td>CMOVNL r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not less (SF=OF).</td>
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<tr>
<td>REX.W + 0F 4D /r</td>
<td>CMOVNL r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not less (SF=OF).</td>
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<tr>
<td>0F 4F /r</td>
<td>CMOVNLE r16, r/m16</td>
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<td>Valid</td>
<td>Move if not less or equal (ZF=0 and SF=OF).</td>
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<tr>
<td>0F 4F /r</td>
<td>CMOVNLE r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not less or equal (ZF=0 and SF=OF).</td>
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<tr>
<td>REX.W + 0F 4F /r</td>
<td>CMOVNLE r64, r/m64</td>
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<td>N.E.</td>
<td>Move if not less or equal (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>0F 41 /r</td>
<td>CMOVNO r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not overflow (OF=0).</td>
</tr>
<tr>
<td>0F 41 /r</td>
<td>CMOVNO r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not overflow (OF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 41 /r</td>
<td>CMOVNO r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not overflow (OF=0).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVNP r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not parity (PF=0).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVNP r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not parity (PF=0).</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>64-Bit Mode</td>
<td>Compat/Leg Mode</td>
<td>Description</td>
</tr>
<tr>
<td>----------------</td>
<td>-----------------</td>
<td>-------------</td>
<td>-----------------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>REX.W + 0F 4B/r</td>
<td>CMOVNP r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not parity (PF=0).</td>
</tr>
<tr>
<td>0F 49 /r</td>
<td>CMOVNS r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not sign (SF=0).</td>
</tr>
<tr>
<td>0F 49 /r</td>
<td>CMOVNS r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not sign (SF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 49/r</td>
<td>CMOVNS r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not sign (SF=0).</td>
</tr>
<tr>
<td>0F 45 /r</td>
<td>CMOVNZ r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not zero (ZF=0).</td>
</tr>
<tr>
<td>0F 45 /r</td>
<td>CMOVNZ r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not zero (ZF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 45/r</td>
<td>CMOVNZ r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not zero (ZF=0).</td>
</tr>
<tr>
<td>0F 40 /r</td>
<td>CMOVNZ r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if overflow (OF=0).</td>
</tr>
<tr>
<td>0F 40 /r</td>
<td>CMOVNZ r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if overflow (OF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 40/r</td>
<td>CMOVNZ r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if overflow (OF=0).</td>
</tr>
<tr>
<td>0F 44 /r</td>
<td>CMOVPO r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity (PF=1).</td>
</tr>
<tr>
<td>0F 44 /r</td>
<td>CMOVPO r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity (PF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 44/r</td>
<td>CMOVPO r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if parity (PF=1).</td>
</tr>
<tr>
<td>0F 48 /r</td>
<td>CMOVPO r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity even (PF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 48/r</td>
<td>CMOVPO r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if parity even (PF=1).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVPO r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity odd (PF=0).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVPO r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity odd (PF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 4B/r</td>
<td>CMOVPO r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if parity odd (PF=0).</td>
</tr>
<tr>
<td>0F 48 /r</td>
<td>CMOVS r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if sign (SF=1).</td>
</tr>
<tr>
<td>0F 48 /r</td>
<td>CMOVS r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if sign (SF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 48/r</td>
<td>CMOVS r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if sign (SF=1).</td>
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<tr>
<td>0F 44 /r</td>
<td>CMOVZ r16, r/m16</td>
<td>Valid</td>
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</tr>
<tr>
<td>0F 44 /r</td>
<td>CMOVZ r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if zero (ZF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 44/r</td>
<td>CMOVZ r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if zero (ZF=1).</td>
</tr>
</tbody>
</table>
Description
The CMOVcc instructions check the state of one or more of the status flags in the EFLAGS register (CF, OF, PF, SF, and ZF) and perform a move operation if the flags are in a specified state (or condition). A condition code (cc) is associated with each instruction to indicate the condition being tested for. If the condition is not satisfied, a move is not performed and execution continues with the instruction following the CMOVcc instruction.

These instructions can move 16-bit, 32-bit or 64-bit values from memory to a general-purpose register or from one general-purpose register to another. Conditional moves of 8-bit register operands are not supported.

The condition for each CMOVcc mnemonic is given in the description column of the above table. The terms “less” and “greater” are used for comparisons of signed integers and the terms “above” and “below” are used for unsigned integers.

Because a particular state of the status flags can sometimes be interpreted in two ways, two mnemonics are defined for some opcodes. For example, the CMOVA (conditional move if above) instruction and the CMOVNBE (conditional move if not below or equal) instruction are alternate mnemonics for the opcode 0F 47H.

The CMOVcc instructions were introduced in P6 family processors; however, these instructions may not be supported by all IA-32 processors. Software can determine if the CMOVcc instructions are supported by checking the processor’s feature information with the CPUID instruction (see “CPUID—CPU Identification” in this chapter).

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

\[ \text{temp} \leftarrow \text{SRC} \]

\[ \text{IF (64-Bit Mode)} \]
\[ \text{THEN} \]
\[ \quad \text{IF condition TRUE} \]
\[ \quad \text{THEN} \]
\[ \quad \quad \text{IF (OperandSize = 64)} \]
\[ \quad \quad \text{THEN} \]
\[ \quad \quad \quad \text{DEST} \leftarrow \text{temp}; \]
\[ \quad \quad \text{ELSE} \]
\[ \quad \quad \quad \text{DEST} \leftarrow \text{temp AND 0x00000000_FFFFFFFF}; \]
\[ \quad \text{FI}; \]
\[ \text{ELSE} \]
\[ \quad \text{IF condition TRUE} \]
\[ \quad \text{THEN} \]

CMOVcc—Conditional Move
DEST ← temp;
F1;
F1;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0)   If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)   If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0)   If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD      If the LOCK prefix is used.
## CMP—Compare Two Operands

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3C ib</td>
<td>CMP AL, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm8 with AL.</td>
</tr>
<tr>
<td>3D iw</td>
<td>CMP AX, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm16 with AX.</td>
</tr>
<tr>
<td>3D id</td>
<td>CMP EAX, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm32 with EAX.</td>
</tr>
<tr>
<td>REX.W + 3D id</td>
<td>CMP RAX, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare imm32 sign-extended to 64-bits with RAX.</td>
</tr>
<tr>
<td>80 ib</td>
<td>CMP r/m8, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm8 with r/m8.</td>
</tr>
<tr>
<td>REX + 80 ib</td>
<td>CMP r/m8, *, imm8</td>
<td>N.E.</td>
<td></td>
<td>Compare imm8 with r/m8.</td>
</tr>
<tr>
<td>81 iw</td>
<td>CMP r/m16, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm16 with r/m16.</td>
</tr>
<tr>
<td>81 id</td>
<td>CMP r/m32, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm32 with r/m32.</td>
</tr>
<tr>
<td>REX.W + 81 id</td>
<td>CMP r/m64, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare imm32 sign-extended to 64-bits with r/m64.</td>
</tr>
<tr>
<td>83 ib</td>
<td>CMP r/m16, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm8 with r/m16.</td>
</tr>
<tr>
<td>REX.W + 83 ib</td>
<td>CMP r/m64, imm8</td>
<td>N.E.</td>
<td></td>
<td>Compare imm8 with r/m64.</td>
</tr>
<tr>
<td>38 l/r</td>
<td>CMP r/m8, r8</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r8 with r/m8.</td>
</tr>
<tr>
<td>REX + 38 l/r</td>
<td>CMP r/m8, *, r8</td>
<td>N.E.</td>
<td></td>
<td>Compare r8 with r/m8.</td>
</tr>
<tr>
<td>39 l/r</td>
<td>CMP r/m16, r16</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r16 with r/m16.</td>
</tr>
<tr>
<td>39 l/r</td>
<td>CMP r/m32, r32</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r32 with r/m32.</td>
</tr>
<tr>
<td>REX.W + 39 l/r</td>
<td>CMP r/m64, r64</td>
<td>N.E.</td>
<td></td>
<td>Compare r64 with r/m64.</td>
</tr>
<tr>
<td>3A l/r</td>
<td>CMP r8, r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r/m64 with r8.</td>
</tr>
<tr>
<td>REX + 3A l/r</td>
<td>CMP r8, r/m8, r8</td>
<td>N.E.</td>
<td></td>
<td>Compare r/m8 with r/m8.</td>
</tr>
<tr>
<td>3B l/r</td>
<td>CMP r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r/m16 with r16.</td>
</tr>
<tr>
<td>3B l/r</td>
<td>CMP r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r/m32 with r32.</td>
</tr>
<tr>
<td>REX.W + 3B l/r</td>
<td>CMP r/m64, r64</td>
<td>N.E.</td>
<td></td>
<td>Compare r/m64 with r/m64.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
Description

Compares the first source operand with the second source operand and sets the status flags in the EFLAGS register according to the results. The comparison is performed by subtracting the second operand from the first operand and then setting the status flags in the same manner as the SUB instruction. When an immediate value is used as an operand, it is sign-extended to the length of the first operand.

The condition codes used by the Jcc, CMOVcc, and SETcc instructions are based on the results of a CMP instruction. Appendix B, “EFLAGS Condition Codes,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, shows the relationship of the status flags and the condition codes.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

temp ← SRC1 – SignExtend(SRC2);
ModifyStatusFlags; (* Modify status flags in the same manner as the SUB instruction*)

Flags Affected

The CF, OF, SF, ZF, AF, and PF flags are set according to the result.

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
CMPPD—Compare Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F C2 /r ib</td>
<td>CMPPD xmm1, xmm2/m128, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare packed double-precision floating-point values in xmm2/m128 and xmm1 using imm8 as comparison predicate.</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD compare of the two packed double-precision floating-point values in the source operand (second operand) and the destination operand (first operand) and returns the results of the comparison to the destination operand. The comparison predicate operand (third operand) specifies the type of comparison performed on each of the pairs of packed values. The result of each comparison is a quadword mask of all 1s (comparison true) or all 0s (comparison false).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The comparison predicate operand is an 8-bit immediate, the first 3 bits of which define the type of comparison to be made (see Table 3-15). Bits 3 through 7 of the immediate are reserved.

**Table 3-15. Comparison Predicate for CMPPD and CMPPS Instructions**

<table>
<thead>
<tr>
<th>Predicate</th>
<th>imm8 Encoding</th>
<th>Description</th>
<th>Relation where: A Is 1st Operand B Is 2nd Operand</th>
<th>Emulation</th>
<th>Result if NaN Operand</th>
<th>QNaN Oper-and Signals Invalid</th>
</tr>
</thead>
<tbody>
<tr>
<td>EQ</td>
<td>000B</td>
<td>Equal</td>
<td>A = B</td>
<td>False</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>LT</td>
<td>001B</td>
<td>Less-than</td>
<td>A &lt; B</td>
<td>False</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>LE</td>
<td>010B</td>
<td>Less-than-or-equal</td>
<td>A ≤ B</td>
<td>False</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Greater than</td>
<td>A &gt; B</td>
<td>Swap Operands, Use LT</td>
<td>False</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Greater-than-or-equal</td>
<td>A ≥ B</td>
<td>Swap Operands, Use LE</td>
<td>False</td>
<td>Yes</td>
</tr>
<tr>
<td>UNORD</td>
<td>011B</td>
<td>Unordered</td>
<td>A, B = Unordered</td>
<td>True</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>NEQ</td>
<td>100B</td>
<td>Not-equal</td>
<td>A ≠ B</td>
<td>True</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>NLT</td>
<td>101B</td>
<td>Not-less-than</td>
<td>NOT(A &lt; B)</td>
<td>True</td>
<td>Yes</td>
<td></td>
</tr>
</tbody>
</table>
The unordered relationship is true when at least one of the two source operands being compared is a NaN; the ordered relationship is true when neither source operand is a NaN.

A subsequent computational instruction that uses the mask result in the destination operand as an input operand will not generate an exception, because a mask of all 0s corresponds to a floating-point value of +0.0 and a mask of all 1s corresponds to a QNaN.

Note that the processor does not implement the greater-than, greater-than-or-equal, not-greater-than, and not-greater-than-or-equal relations. These comparisons can be made either by using the inverse relationship (that is, use the "not-less-than-or-equal" to make a "greater-than" comparison) or by using software emulation. When using software emulation, the program must swap the operands (copying registers when necessary to protect the data that will now be in the destination), and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in Table 3-15 under the heading Emulation.

Compilers and assemblers may implement the following two-operand pseudo-ops in addition to the three-operand CMPPD instruction. See Table 3-8.

### Table 3-15. Comparison Predicate for CMPPD and CMPPS Instructions  (Contd.)

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPPD Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPEQPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 0</td>
</tr>
<tr>
<td>CMPLTPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 1</td>
</tr>
<tr>
<td>CMPEPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 2</td>
</tr>
<tr>
<td>CMPUNORDPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 3</td>
</tr>
<tr>
<td>CMPNEQPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 4</td>
</tr>
<tr>
<td>CMPNLTPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 5</td>
</tr>
</tbody>
</table>

The unordered relationship is true when at least one of the two source operands being compared is a NaN; the ordered relationship is true when neither source operand is a NaN.

A subsequent computational instruction that uses the mask result in the destination operand as an input operand will not generate an exception, because a mask of all 0s corresponds to a floating-point value of +0.0 and a mask of all 1s corresponds to a QNaN.

Note that the processor does not implement the greater-than, greater-than-or-equal, not-greater-than, and not-greater-than-or-equal relations. These comparisons can be made either by using the inverse relationship (that is, use the "not-less-than-or-equal" to make a "greater-than" comparison) or by using software emulation. When using software emulation, the program must swap the operands (copying registers when necessary to protect the data that will now be in the destination), and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in Table 3-15 under the heading Emulation.

Compilers and assemblers may implement the following two-operand pseudo-ops in addition to the three-operand CMPPD instruction. See Table 3-8.

### Table 3-16. Pseudo-Op and CMPPD Implementation

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPPD Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPEQPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 0</td>
</tr>
<tr>
<td>CMPLTPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 1</td>
</tr>
<tr>
<td>CMPEPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 2</td>
</tr>
<tr>
<td>CMPUNORDPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 3</td>
</tr>
<tr>
<td>CMPNEQPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 4</td>
</tr>
<tr>
<td>CMPNLTPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 5</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-M

Table 3-16. Pseudo-Op and CMPPD Implementation

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPPD Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPNLEPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 6</td>
</tr>
<tr>
<td>CMPORDPD xmm1, xmm2</td>
<td>CMPPD xmm1, xmm2, 7</td>
</tr>
</tbody>
</table>

The greater-than relations that the processor does not implement require more than one instruction to emulate in software and therefore should not be implemented as pseudo-ops. (For these, the programmer should reverse the operands of the corresponding less than relations and use move instructions to ensure that the mask is moved to the correct destination register and that the source operand is left intact.)

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

CASE (COMPARISON PREDICATE) OF
  0:   OP ← EQ;
  1:   OP ← LT;
  2:   OP ← LE;
  3:   OP ← UNORD;
  4:   OP ← NEQ;
  5:   OP ← NLT;
  6:   OP ← NLE;
  7:   OP ← ORD;
DEFAULT: Reserved;

CMP0 ← DEST[63:0] OP SRC[63:0];
CMP1 ← DEST[127:64] OP SRC[127:64];
IF CMP0 = TRUE
  THEN DEST[63:0] ← FFFFFFFF0000000000000000H; Fl;
ELSE DEST[63:0] ← 000000000000000000000000H; Fi;
IF CMP1 = TRUE
  THEN DEST[127:64] ← FFFFFFFFFFFFFFFF00000000000000H; Fl;
ELSE DEST[127:64] ← 000000000000000000000000H; Fi;

Intel C/C++ Compiler Intrinsic Equivalents

CMPPD for equality       _m128d_mm_cmpeq_pd(_m128d a, _m128d b)
CMPPD for less-than      _m128d_mm_cmplt_pd(_m128d a, _m128d b)
CMPPD for less-than-or-equal _m128d_mm_cmple_pd(_m128d a, _m128d b)
CMPPD for greater-than   _m128d_mm_cmpgt_pd(_m128d a, _m128d b)
CMPPD for greater-than-or-equal _m128d_mm_cmple_pd(_m128d a, _m128d b)

CMPPD—Compare Packed Double-Precision Floating-Point Values
CMPPD for inequality  __m128d _mm_cmpneq_pd(__m128d a, __m128d b)
CMPPD for not-less-than  __m128d _mm_cmpnlt_pd(__m128d a, __m128d b)
CMPPD for not-greater-than  __m128d _mm_cmpngt_pd(__m128d a, __m128d b)
CMPPD for not-greater-than-or-equal  __m128d _mm_cmpnge_pd(__m128d a, __m128d b)
CMPPD for ordered  __m128d _mm_cmpord_pd(__m128d a, __m128d b)
CMPPD for unordered  __m128d _mm_cmpunord_pd(__m128d a, __m128d b)
CMPPD for not-less-than-or-equal  __m128d _mm_cmpnle_pd(__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Invalid if SNaN operand and invalid if QNaN and predicate as listed in above table, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD  
If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

Same exceptions as in real address mode.

#PF(fault-code)  
For a page fault.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0)  
If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  
If the memory address is in a non-canonical form.
  If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code)  
For a page fault.

#NM  
If CR0.TS[bit 3] = 1.

#XM  

#UD  
If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.
CMPPS—Compare Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F C2 /r ib</td>
<td>CMPPS xmm1, xmm2/m128, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare packed single-precision floating-point values in xmm2/mem and xmm1 using imm8 as comparison predicate.</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD compare of the four packed single-precision floating-point values in the source operand (second operand) and the destination operand (first operand) and returns the results of the comparison to the destination operand. The comparison predicate operand (third operand) specifies the type of comparison performed on each of the pairs of packed values. The result of each comparison is a doubleword mask of all 1s (comparison true) or all 0s (comparison false).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The comparison predicate operand is an 8-bit immediate, the first 3 bits of which define the type of comparison to be made (see Table 3-15). Bits 3 through 7 of the immediate are reserved.

The unordered relationship is true when at least one of the two source operands being compared is a NaN; the ordered relationship is true when neither source operand is a NaN.

A subsequent computational instruction that uses the mask result in the destination operand as an input operand will not generate a fault, because a mask of all 0s corresponds to a floating-point value of +0.0 and a mask of all 1s corresponds to a QNaN.

Some of the comparisons listed in Table 3-15 (such as the greater-than, greater-than-or-equal, not-greater-than, and not-greater-than-or-equal relations) can be made only through software emulation. For these comparisons the program must swap the operands (copying registers when necessary to protect the data that will now be in the destination), and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in Table 3-15 under the heading Emulation.

Compilers and assemblers may implement the following two-operand pseudo-ops in addition to the three-operand CMPPS instruction. See Table 3-17.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
The greater-than relations not implemented by the processor require more than one instruction to emulate in software and therefore should not be implemented as pseudo-ops. (For these, the programmer should reverse the operands of the corresponding less than relations and use move instructions to ensure that the mask is moved to the correct destination register and that the source operand is left intact.)

**Table 3-17. Pseudo-Ops and CMPPS**

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPEQPS xmm1, xmm2</td>
<td>CMPPS xmm1, xmm2, 0</td>
</tr>
<tr>
<td>CMPLTPS xmm1, xmm2</td>
<td>CMPPS xmm1, xmm2, 1</td>
</tr>
<tr>
<td>CMPLEPS xmm1, xmm2</td>
<td>CMPPS xmm1, xmm2, 2</td>
</tr>
<tr>
<td>CMPPUNORDPS xmm1, xmm2</td>
<td>CMPPS xmm1, xmm2, 3</td>
</tr>
<tr>
<td>CMPPNEQPS xmm1, xmm2</td>
<td>CMPPS xmm1, xmm2, 4</td>
</tr>
<tr>
<td>CMPPNLTPS xmm1, xmm2</td>
<td>CMPPS xmm1, xmm2, 5</td>
</tr>
<tr>
<td>CMPPNLEPS xmm1, xmm2</td>
<td>CMPPS xmm1, xmm2, 6</td>
</tr>
<tr>
<td>CMPPORDPS xmm1, xmm2</td>
<td>CMPPS xmm1, xmm2, 7</td>
</tr>
</tbody>
</table>

**Operation**

```plaintext
CASE (COMPARISON PREDICATE) OF
  0:  OP ← EQ;
  1:  OP ← LT;
  2:  OP ← LE;
  3:  OP ← UNORD;
  4:  OP ← NE;
  5:  OP ← NLT;
  6:  OP ← NLE;
  7:  OP ← ORD;
EASC;

CMPO ← DEST[31:0] OP SRC[31:0];
CMP1 ← DEST[63:32] OP SRC[63:32];
CMP2 ← DEST[95:64] OP SRC[95:64];
CMP3 ← DEST[127:96] OP SRC[127:96];

IF CMPO = TRUE
  THEN DEST[31:0] ← FFFFFFFFH;
  ELSE DEST[31:0] ← 00000000H; Fl;
IF CMP1 = TRUE
  THEN DEST[63:32] ← FFFFFFFFH;
  ELSE DEST[63:32] ← 00000000H; Fl;
IF CMP2 = TRUE
```

**CMPPS—Compare Packed Single-Precision Floating-Point Values**
THEN DEST[95:64] ← FFFFFFFFH;
ELSE DEST[95:64] ← 00000000H; F;

IF CMP3 = TRUE
THEN DEST[127:96] ← FFFFFFFFH;
ELSE DEST[127:96] ← 00000000H; F;

Intel C/C++ Compiler Intrinsic Equivalents
CMPPS for equality
__m128 _mm_cmpeq_ps(__m128 a, __m128 b)
CMPPS for less-than
__m128 _mm_cmplt_ps(__m128 a, __m128 b)
CMPPS for less-than-or-equal
__m128 _mm_cmple_ps(__m128 a, __m128 b)
CMPPS for greater-than
__m128 _mm_cmpgt_ps(__m128 a, __m128 b)
CMPPS for greater-than-or-equal
__m128 _mm_cmpge_ps(__m128 a, __m128 b)
CMPPS for inequality
__m128 _mm_cmpneq_ps(__m128 a, __m128 b)
CMPPS for not-less-than
__m128 _mm_cmpnlt_ps(__m128 a, __m128 b)
CMPPS for not-greater-than
__m128 _mm_cmpngt_ps(__m128 a, __m128 b)
CMPPS for not-greater-than-or-equal
__m128 _mm_cmpnge_ps(__m128 a, __m128 b)
CMPPS for ordered
__m128 _mm_cmppord_ps(__m128 a, __m128 b)
CMPPS for unordered
__m128 _mm_cmpunord_ps(__m128 a, __m128 b)
CMPPS for not-less-than-or-equal
__m128 _mm_cmpnle_ps(__m128 a, __m128 b)

SIMD Floating-Point Exceptions
Invalid if SNaN operand and invalid if QNaN and predicate as listed in above table, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD

If an unmasked SIMD floating-point exception and CR4.OSXM-
MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
## CMPS/CMPSB/CMPSW/CMPSD/CMPSQ—Compare String Operands

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A6</td>
<td>CMPS m8, m8</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare byte at address DS:(E)SI with byte at address ES:(E)DI; For 64-bit mode compare byte at address (R</td>
</tr>
<tr>
<td>A7</td>
<td>CMPS m16, m16</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare word at address DS:(E)SI with word at address ES:(E)DI; For 64-bit mode compare word at address (R</td>
</tr>
<tr>
<td>A7</td>
<td>CMPS m32, m32</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare dword at address DS:(E)SI at dword at address ES:(E)DI; For 64-bit mode compare dword at address (R</td>
</tr>
<tr>
<td>REX.W + A7</td>
<td>CMPS m64, m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compares quadword at address (R</td>
</tr>
<tr>
<td>A6</td>
<td>CMPSB</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare byte at address DS:(E)SI with byte at address ES:(E)DI; For 64-bit mode compare byte at address (R</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-M

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A7</td>
<td>CMPSW</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare word at address DS:(E)SI with word at address ES:(E)DI; For 64-bit mode compare word at address (R</td>
</tr>
<tr>
<td>A7</td>
<td>CMPSD</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare dword at address DS:(E)SI with dword at address ES:(E)DI; For 64-bit mode compare dword at address (R</td>
</tr>
<tr>
<td>REX.W + A7</td>
<td>CMPSQ</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compares quadword at address (R</td>
</tr>
</tbody>
</table>

Description

Compares the byte, word, doubleword, or quadword specified with the first source operand with the byte, word, doubleword, or quadword specified with the second source operand and sets the status flags in the EFLAGS register according to the results.

Both source operands are located in memory. The address of the first source operand is read from DS:SI, DS:ESI or RSI (depending on the address-size attribute of the instruction is 16, 32, or 64, respectively). The address of the second source operand is read from ES:DI, ES:EDI or RDI (again depending on the address-size attribute of the instruction is 16, 32, or 64). The DS segment may be overridden with a segment override prefix, but the ES segment cannot be overridden.

At the assembly-code level, two forms of this instruction are allowed: the "explicit-operands" form and the "no-operands" form. The explicit-operands form (specified with the CMPS mnemonic) allows the two source operands to be specified explicitly. Here, the source operands should be symbols that indicate the size and location of the source values. This explicit-operand form is provided to allow documentation. However, note that the documentation provided by this form can be misleading. That is, the source operand symbols must specify the correct type (size) of the operands (bytes, words, or doublewords, quadwords), but they do not have to specify the correct location. Locations of the source operands are always specified by the DS:(E)SI (or RSI) and ES:(E)DI (or RDI) registers, which must be loaded correctly before the compare string instruction is executed.

The no-operands form provides "short forms" of the byte, word, and doubleword versions of the CMPS instructions. Here also the DS:(E)SI (or RSI) and ES:(E)DI (or
INSTRUCTION SET REFERENCE, A-M

CMPS/CMPSB/CMPSW/CMPSD/CMPSQ—Compare String Operands

RDI) registers are assumed by the processor to specify the location of the source operands. The size of the source operands is selected with the mnemonic: CMPSB (byte comparison), CMPSW (word comparison), CMPSD (doubleword comparison), or CMPSQ (quadword comparison using REX.W).

After the comparison, the (E/R)SI and (E/R)DI registers increment or decrement automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the (E/R)SI and (E/R)DI registers increment; if the DF flag is 1, the registers decrement.) The registers increment or decrement by 1 for byte operations, by 2 for word operations, 4 for doubleword operations. If operand size is 64, RSI and RDI registers increment by 8 for quadword operations.

The CMPS, CMPSB, CMPSW, CMPSD, and CMPSQ instructions can be preceded by the REP prefix for block comparisons. More often, however, these instructions will be used in a LOOP construct that takes some action based on the setting of the status flags before the next comparison is made. See “RDTSCP—Read Time-Stamp Counter and Processor ID” in Chapter 4, in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B, for a description of the REP prefix.

In 64-bit mode, the instruction’s default address size is 64 bits, 32 bit address size is supported using the prefix 67H. Use of the REX.W prefix promotes doubleword operation to 64 bits (see CMPSQ). See the summary chart at the beginning of this section for encoding data and limits.

Operation

temp SRC1 - SRC2;
SetStatusFlags(temp);

IF (64-Bit Mode) THEN
    IF (Byte comparison) THEN IF DF = 0 THEN (R|E)SI ← (R|E)SI + 1;
        (R|E)DI ← (R|E)DI + 1;
    ELSE
        (R|E)SI ← (R|E)SI - 1;
        (R|E)DI ← (R|E)DI - 1;
    FI;
    ELSE IF (Word comparison) THEN IF DF = 0 THEN (R|E)SI ← (R|E)SI + 2;
        (R|E)DI ← (R|E)DI + 2;
    ELSE
        (R|E)SI ← (R|E)SI - 2;

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(R|E)DI ← (R|E)DI - 2;
FI;
ELSE IF (Doubleword comparison)
THEN IF DF = 0
THEN
(R|E)SI ← (R|E)SI + 4;
(R|E)DI ← (R|E)DI + 4;
ELSE
(R|E)SI ← (R|E)SI - 4;
(R|E)DI ← (R|E)DI - 4;
FI;
ELSE (* Quadword comparison *)
THEN IF DF = 0
(R|E)SI ← (R|E)SI + 8;
(R|E)DI ← (R|E)DI + 8;
ELSE
(R|E)SI ← (R|E)SI - 8;
(R|E)DI ← (R|E)DI - 8;
FI;
FI;
ELSE (* Non-64-bit Mode *)
IF (byte comparison)
THEN IF DF = 0
THEN
(E)SI ← (E)SI + 1;
(E)DI ← (E)DI + 1;
ELSE
(E)SI ← (E)SI - 1;
(E)DI ← (E)DI - 1;
FI;
ELSE IF (word comparison)
THEN IF DF = 0
(E)SI ← (E)SI + 2;
(E)DI ← (E)DI + 2;
ELSE
(E)SI ← (E)SI - 2;
(E)DI ← (E)DI - 2;
FI;
ELSE (* Doubleword comparison *)
THEN IF DF = 0
(E)SI ← (E)SI + 4;
(E)DI ← (E)DI + 4;
ELSE
(E)SI ← (E)SI - 4;
(E)DI ← (E)DI - 4;
FI;
FI;
FI;

Flags Affected
The CF, OF, SF, ZF, AF, and PF flags are set according to the temporary result of the comparison.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-M

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.
**CMPSD—Compare Scalar Double-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F C2 /r ib</td>
<td>CMPSD xmm1, xmm2/m64, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare low double-precision floating-point value in xmm2/m64 and xmm1 using imm8 as comparison predicate.</td>
</tr>
</tbody>
</table>

**Description**

Compares the low double-precision floating-point values in the source operand (second operand) and the destination operand (first operand) and returns the results of the comparison to the destination operand. The comparison predicate operand (third operand) specifies the type of comparison performed. The comparison result is a quadword mask of all 1s (comparison true) or all 0s (comparison false).

The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. The result is stored in the low quadword of the destination operand; the high quadword remains unchanged. The comparison predicate operand is an 8-bit immediate, the first 3 bits of which define the type of comparison to be made (see Table 3-15). Bits 3 through 7 of the immediate are reserved.

The unordered relationship is true when at least one of the two source operands being compared is a NaN; the ordered relationship is true when neither source operand is a NaN.

A subsequent computational instruction that uses the mask result in the destination operand as an input operand will not generate a fault, because a mask of all 0s corresponds to a floating-point value of +0.0 and a mask of all 1s corresponds to a QNaN.

Some of the comparisons listed in Table 3-15 can be achieved only through software emulation. For these comparisons the program must swap the operands (copying registers when necessary to protect the data that will now be in the destination operand), and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in Table 3-15 under the heading Emulation.

Compilers and assemblers may implement the following two-operand pseudo-ops in addition to the three-operand CMPSD instruction. See Table 3-18.

**Table 3-18. Pseudo-Ops and CMPSD**

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPEQSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 0</td>
</tr>
<tr>
<td>CMLTSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 1</td>
</tr>
<tr>
<td>CMPLESD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 2</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-M

Table 3-18. Pseudo-Ops and CMPSD (Contd.)

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 3</td>
</tr>
<tr>
<td>CMPSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 4</td>
</tr>
<tr>
<td>CMPSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 5</td>
</tr>
<tr>
<td>CMPSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 6</td>
</tr>
<tr>
<td>CMPSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 7</td>
</tr>
</tbody>
</table>

The greater-than relations not implemented in the processor require more than one instruction to emulate in software and therefore should not be implemented as pseudo-ops. (For these, the programmer should reverse the operands of the corresponding less than relations and use move instructions to ensure that the mask is moved to the correct destination register and that the source operand is left intact.)

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

CASE (COMPARISON PREDICATE) OF
  0: OP ← EQ;
  1: OP ← LT;
  2: OP ← LE;
  3: OP ← UNORD;
  4: OP ← NEQ;
  5: OP ← NLT;
  6: OP ← NLE;
  7: OP ← ORD;
DEFAULT: Reserved;

CMP0 ← DEST[63:0] OP SRC[63:0];

IF CMP0 = TRUE
  THEN DEST[63:0] ← FFFFFFFFFFFFFFFFFH;
  ELSE DEST[63:0] ← 0000000000000000H; Fi;
(* DEST[127:64] unchanged *)

Intel C/C++ Compiler Intrinsic Equivalents

| CMPSD for equality  | __m128d _mm_cmpeq_sd(__m128d a, __m128d b) |
| CMPSD for less-than | __m128d _mm_cmplt_sd(__m128d a, __m128d b) |
| CMPSD for less-than-or-equal | __m128d _mm_cmple_sd(__m128d a, __m128d b) |
| CMPSD for greater-than | __m128d _mm_cmpgt_sd(__m128d a, __m128d b) |
CMPSD for greater-than-or-equal __m128d _mm_cmpge_sd(__m128d a, __m128d b)
CMPSD for inequality __m128d _mm_cmpneq_sd(__m128d a, __m128d b)
CMPSD for not-less-than __m128d _mm_cmpnlt_sd(__m128d a, __m128d b)
CMPSD for not-greater-than __m128d _mm_cmpngt_sd(__m128d a, __m128d b)
CMPSD for not-greater-than-or-equal __m128d _mm_cmpnge_sd(__m128d a, __m128d b)
CMPSD for ordered __m128d _mm_cmpord_sd(__m128d a, __m128d b)
CMPSD for unordered __m128d _mm_cmpunord_sd(__m128d a, __m128d b)
CMPSD for not-less-than-or-equal __m128d _mm_cmpnle_sd(__m128d a, __m128d b)

**SIMD Floating-Point Exceptions**

Invalid if SNaN operand, Invalid if QNaN and predicate as listed in above table, Denormal.

**Protected Mode Exceptions**

- #GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- #SS(0) For an illegal address in the SS segment.
- #PF(fault-code) For a page fault.
- #NM If CR0.TS[bit 3] = 1.
- #UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
- #UD If the LOCK prefix is used.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- #GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
- #NM If CR0.TS[bit 3] = 1.
- #UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
CMPSD—Compare Scalar Double-Precision Floating-Point Values

If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CMPSS—Compare Scalar Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F C2 /r ib</td>
<td>CMPSS xmm1, xmm2/m32, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare low single-precision floating-point value in xmm2/m32 and xmm1 using imm8 as comparison predicate.</td>
</tr>
</tbody>
</table>

**Description**

Compares the low single-precision floating-point values in the source operand (second operand) and the destination operand (first operand) and returns the results of the comparison to the destination operand. The comparison predicate operand (third operand) specifies the type of comparison performed. The comparison result is a doubleword mask of all 1s (comparison true) or all 0s (comparison false).

The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. The result is stored in the low doubleword of the destination operand; the 3 high-order doublewords remain unchanged. The comparison predicate operand is an 8-bit immediate, the first 3 bits of which define the type of comparison to be made (see Table 3-15). Bits 3 through 7 of the immediate are reserved.

The unordered relationship is true when at least one of the two source operands being compared is a NaN; the ordered relationship is true when neither source operand is a NaN.

A subsequent computational instruction that uses the mask result in the destination operand as an input operand will not generate a fault, since a mask of all 0s corresponds to a floating-point value of +0.0 and a mask of all 1s corresponds to a QNaN.

Some of the comparisons listed in Table 3-15 can be achieved only through software emulation. For these comparisons the program must swap the operands (copying registers when necessary to protect the data that will now be in the destination operand), and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in Table 3-15 under the heading Emulation.

Compilers and assemblers may implement the following two-operand pseudo-ops in addition to the three-operand CMPSS instruction. See Table 3-19.
The greater-than relations not implemented in the processor require more than one instruction to emulate in software and therefore should not be implemented as pseudo-ops. (For these, the programmer should reverse the operands of the corresponding less than relations and use move instructions to ensure that the mask is moved to the correct destination register and that the source operand is left intact.) In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Table 3-19. Pseudo-Ops and CMPSS**

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPSS Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPEQSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 0</td>
</tr>
<tr>
<td>CMPLTSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 1</td>
</tr>
<tr>
<td>CMPLESS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 2</td>
</tr>
<tr>
<td>CMPUNORDSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 3</td>
</tr>
<tr>
<td>CMPNEQSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 4</td>
</tr>
<tr>
<td>CMPNLTSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 5</td>
</tr>
<tr>
<td>CMPNLESS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 6</td>
</tr>
<tr>
<td>CMPOORDSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 7</td>
</tr>
</tbody>
</table>

**Operation**

CASE (COMPARISON PREDICATE) OF

0: OP ← EQ;
1: OP ← LT;
2: OP ← LE;
3: OP ← UNORD;
4: OP ← NEQ;
5: OP ← NLT;
6: OP ← NLE;
7: OP ← ORD;
DEFAULT: Reserved;

CMP0 ← DEST[31:0] OP SRC[31:0];

IF CMP0 = TRUE
    THEN DEST[31:0] ← FFFFFFFFH;
ELSE DEST[31:0] ← 00000000H; Fl;
(* DEST[127:32] unchanged *)

**Intel C/C++ Compiler Intrinsic Equivalents**

CMPSS for equality  __m128 _mm_cmpeq_ss(__m128 a, __m128 b)
CMPSS for less-than  \_m128\_mm_cmplt\_ss(\_m128 a, \_m128 b)
CMPSS for less-than-or-equal \_m128\_mm_cmple\_ss(\_m128 a, \_m128 b)
CMPSS for greater-than \_m128\_mm_cmpgt\_ss(\_m128 a, \_m128 b)
CMPSS for greater-than-or-equal \_m128\_mm_cmpge\_ss(\_m128 a, \_m128 b)
CMPSS for inequality \_m128\_mm_cmpneq\_ss(\_m128 a, \_m128 b)
CMPSS for not-less-than \_m128\_mm_cmpnlt\_ss(\_m128 a, \_m128 b)
CMPSS for not-greater-than \_m128\_mm_cmplt\_ss(\_m128 a, \_m128 b)
CMPSS for not-greater-than-or-equal \_m128\_mm_cmple\_ss(\_m128 a, \_m128 b)
CMPSS for ordered \_m128\_mm_cmpord\_ss(\_m128 a, \_m128 b)
CMPSS for unordered \_m128\_mm_cmpunord\_ss(\_m128 a, \_m128 b)
CMPSS for not-less-than-or-equal \_m128\_mm_cmplt\_ss(\_m128 a, \_m128 b)

**SIMD Floating-Point Exceptions**

Invalid if SNaN operand, Invalid if QNaN and predicate as listed in above table, Denormal.

**Protected Mode Exceptions**

- #GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- #SS(0) For an illegal address in the SS segment.
- #PF(fault-code) For a page fault.
- #NM If CR0.TS[bit 3] = 1.
- #UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
- #UD If the LOCK prefix is used.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- #GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
- #NM If CR0.TS[bit 3] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
**CMPXCHG—Compare and Exchange**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F B0/r</td>
<td>CMPXCHG r/m8, r8</td>
<td>Valid</td>
<td>Valid*</td>
<td>Compare AL with r/m8. If equal, ZF is set and r8 is loaded into r/m8. Else, clear ZF and load r/m8 into AL.</td>
</tr>
<tr>
<td>REX + 0F B0/r</td>
<td>CMPXCHG r/m8**, r8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare AL with r/m8. If equal, ZF is set and r8 is loaded into r/m8. Else, clear ZF and load r/m8 into AL.</td>
</tr>
<tr>
<td>0F B1/r</td>
<td>CMPXCHG r/m16, r16</td>
<td>Valid</td>
<td>Valid*</td>
<td>Compare AX with r/m16. If equal, ZF is set and r16 is loaded into r/m16. Else, clear ZF and load r/m16 into AX.</td>
</tr>
<tr>
<td>0F B1/r</td>
<td>CMPXCHG r/m32, r32</td>
<td>Valid</td>
<td>Valid*</td>
<td>Compare EAX with r/m32. If equal, ZF is set and r32 is loaded into r/m32. Else, clear ZF and load r/m32 into EAX.</td>
</tr>
<tr>
<td>REX.W + 0F B1/r</td>
<td>CMPXCHG r/m64, r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare RAX with r/m64. If equal, ZF is set and r64 is loaded into r/m64. Else, clear ZF and load r/m64 into RAX.</td>
</tr>
</tbody>
</table>

**NOTES:**
* See the IA-32 Architecture Compatibility section below.
** In 64-bit mode, r/m8 cannot be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Description**

Compares the value in the AL, AX, EAX, or RAX register with the first operand (destination operand). If the two values are equal, the second operand (source operand) is loaded into the destination operand. Otherwise, the destination operand is loaded into the AL, AX, EAX or RAX register. RAX register is available only in 64-bit mode.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically. To simplify the interface to the processor’s bus, the destination operand receives a write cycle without regard to the result of the comparison. The destination operand is written back if the comparison fails; otherwise, the source operand is written into the destination. (The processor never produces a locked read without also producing a locked write.)
INSTRUCTION SET REFERENCE, A-M

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

IA-32 Architecture Compatibility
This instruction is not supported on Intel processors earlier than the Intel486 processors.

Operation
(* Accumulator = AL, AX, EAX, or RAX depending on whether a byte, word, doubleword, or quadword comparison is being performed *)

IF accumulator = DEST
    THEN
        ZF ← 1;
        DEST ← SRC;
    ELSE
        ZF ← 0;
        accumulator ← DEST;
FI;

Flags Affected
The ZF flag is set if the values in the destination operand and register AL, AX, or EAX are equal; otherwise it is cleared. The CF, PF, AF, SF, and OF flags are set according to the results of the comparison operation.

Protected Mode Exceptions
#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.
Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.
CMPXCHG8B/CMPXCHG16B—Compare and Exchange Bytes

**Description**

Compares the 64-bit value in EDX:EAX (or 128-bit value in RDX:RAX if operand size is 128 bits) with the operand (destination operand). If the values are equal, the 64-bit value in ECX:EBX (or 128-bit value in RCX:RBX) is stored in the destination operand. Otherwise, the value in the destination operand is loaded into EDX:EAX (or RDX:RAX). The destination operand an 8-byte memory location (or 16-byte memory location if operand size is 128 bits). For the EDX:EAX and ECX:EBX register pairs, EDX and ECX contain the high-order 32 bits and EAX and EBX contain the low-order 32 bits of a 64-bit value. For the RDX:RAX and RCX:RBX register pairs, RDX and RCX contain the high-order 64 bits and RAX and RBX contain the low-order 64 bits of a 128-bit value.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically. To simplify the interface to the processor’s bus, the destination operand receives a write cycle without regard to the result of the comparison. The destination operand is written back if the comparison fails; otherwise, the source operand is written into the destination. (The processor never produces a locked read without also producing a locked write.)

In 64-bit mode, default operation size is 64 bits. Use of the REX.W prefix promotes operation to 128 bits. Note that CMPXCHG16B requires that the destination (memory) operand be 16-byte aligned. See the summary chart at the beginning of this section for encoding data and limits. For information on the CPUID flag that indicates CMPXCHG16B, see page 3-195.

**IA-32 Architecture Compatibility**

This instruction encoding is not supported on Intel processors earlier than the Pentium processors.
Operation

IF (64-Bit Mode and OperandSize = 64)
THEN
   IF (RDX:RAX = DEST)
      ZF ← 1;
      DEST ← RCX:RBX;
   ELSE
      ZF ← 0;
      RDX:RAX ← DEST;
   FI
ELSE
   IF (EDX:EAX = DEST)
      ZF ← 1;
      DEST ← ECX:EBX;
   ELSE
      ZF ← 0;
      EDX:EAX ← DEST;
   FI;
FI;

Flags Affected

The ZF flag is set if the destination operand and EDX:EAX are equal; otherwise it is cleared. The CF, PF, AF, SF, and OF flags are unaffected.

Protected Mode Exceptions

#UD If the destination is not a memory operand.
#GP(0) If the destination is located in a non-writable segment.
   If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#UD If the destination operand is not a memory location.
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
INSTRUCTION SET REFERENCE, A-M

#SS If a memory operand effective address is outside the SS segment limit.

Virtual-8086 Mode Exceptions
#UD If the destination operand is not a memory location.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand for CMPXCHG16B is not aligned on a 16-byte boundary.
If CPUID.01H:ECX.CMPXCHG16B[bit 13] = 0.
#UD If the destination operand is not a memory location.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
COMISD—Compare Scalar Ordered Double-Precision Floating-Point Values and Set EFLAGS

**Description**

Compares the double-precision floating-point values in the low quadwords of operand 1 (first operand) and operand 2 (second operand), and sets the ZF, PF, and CF flags in the EFLAGS register according to the result (unordered, greater than, less than, or equal). The OF, SF and AF flags in the EFLAGS register are set to 0. The unordered result is returned if either source operand is a NaN (QNaN or SNaN).

Operand 1 is an XMM register; operand 2 can be an XMM register or a 64 bit memory location.

The COMISD instruction differs from the UCOMISD instruction in that it signals a SIMD floating-point invalid operation exception (#I) when a source operand is either a QNaN or SNaN. The UCOMISD instruction signals an invalid numeric exception only if a source operand is an SNaN.

The EFLAGS register is not updated if an unmasked SIMD floating-point exception is generated.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

RESULT ← OrderedCompare(DEST[63:0] <> SRC[63:0])

(* Set EFLAGS *) CASE (RESULT) OF
  UNORDERED:  ZF, PF, CF ← 111;
  GREATER_THAN:  ZF, PF, CF ← 000;
  LESS_THAN:  ZF, PF, CF ← 001;
  EQUAL:  ZF, PF, CF ← 100;
ESAC;

OF, AF, SF ← 0;

**Intel C/C++ Compiler Intrinsic Equivalents**

```c
int _mm_comieq_sd (__m128d a, __m128d b)
```

**Opcode Instruction 64-Bit Mode Compat/ Leg Mode Description**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 2F /r</td>
<td>COMISD xmm1, xmm2/m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare low double-precision floating-point values in xmm1 and xmm2/mem64 and set the EFLAGS flags accordingly.</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-M

int _mm_comilt_sd (__m128d a, __m128d b)
int _mm_comile_sd (__m128d a, __m128d b)
int _mm_comigt_sd (__m128d a, __m128d b)
int _mm_comige_sd (__m128d a, __m128d b)
int _mm_comineq_sd (__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Invalid (if SNaN or QNaN operands), Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS,
ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-
MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory
reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address
space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-
MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.

#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
COMISS—Compare Scalar Ordered Single-Precision Floating-Point Values and Set EFLAGS

Description

Compares the single-precision floating-point values in the low doublewords of operand 1 (first operand) and operand 2 (second operand), and sets the ZF, PF, and CF flags in the EFLAGS register according to the result (unordered, greater than, less than, or equal). The OF, SF, and AF flags in the EFLAGS register are set to 0. The unordered result is returned if either source operand is a NaN (QNaN or SNaN).

Operand 1 is an XMM register; Operand 2 can be an XMM register or a 32 bit memory location.

The COMISS instruction differs from the UCOMISS instruction in that it signals a SIMD floating-point invalid operation exception (#I) when a source operand is either a QNaN or SNaN. The UCOMISS instruction signals an invalid numeric exception only if a source operand is an SNaN.

The EFLAGS register is not updated if an unmasked SIMD floating-point exception is generated.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

RESULT ← OrderedCompare(SRC1[31:0] <> SRC2[31:0])
(* Set EFLAGS *) CASE (RESULT) OF
    UNORDERED: ZF,PF,CF ← 111;
    GREATER_THAN: ZF,PF,CF ← 000;
    LESS_THAN: ZF,PF,CF ← 001;
    EQUAL: ZF,PF,CF ← 100;
ESAC;
OF,AF,SF ← 0;

Intel C/C++ Compiler Intrinsic Equivalents

int _mm_comieq_ss (__m128 a, __m128 b)
int _mm_comilt_ss (__m128 a, __m128 b)
int _mm_cmile_ss (__m128 a, __m128 b)
int _mm_comigt_ss (__m128 a, __m128 b)
int _mm_comige_ss (__m128 a, __m128 b)
int _mm_comineq_ss (__m128 a, __m128 b)

**SIMD Floating-Point Exceptions**
Invalid (if SNaN or QNaN operands), Denormal.

**Protected Mode Exceptions**
- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- **#SS(0)** For an illegal address in the SS segment.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**
- **GP** If any part of the operand lies outside the effective address space from 0 to FFFFH.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.
Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CPUID—CPU Identification

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F A2</td>
<td>CPUID</td>
<td>Valid</td>
<td>Valid</td>
<td>Returns processor identification and feature information to the EAX, EBX, ECX, and EDX registers, as determined by input entered in EAX (in some cases, ECX as well).</td>
</tr>
</tbody>
</table>

**Description**

The ID flag (bit 21) in the EFLAGS register indicates support for the CPUID instruction. If a software procedure can set and clear this flag, the processor executing the procedure supports the CPUID instruction. This instruction operates the same in non-64-bit modes and 64-bit mode.

CPUID returns processor identification and feature information in the EAX, EBX, ECX, and EDX registers. The instruction’s output is dependent on the contents of the EAX register upon execution (in some cases, ECX as well). For example, the following pseudocode loads EAX with 00H and causes CPUID to return a Maximum Return Value and the Vendor Identification String in the appropriate registers:

```assembly
MOV EAX, 00H
CPUID
```

Table 3-20 shows information returned, depending on the initial value loaded into the EAX register. Table 3-21 shows the maximum CPUID input value recognized for each family of IA-32 processors on which CPUID is implemented.

Two types of information are returned: basic and extended function information. If a value entered for CPUID.EAX is higher than the maximum input value for basic or extended function for that processor then the data for the highest basic information leaf is returned. For example, using the Intel Core i7 processor, the following is true:

- CPUID.EAX = 05H (* Returns MONITOR/MWAIT leaf. *)
- CPUID.EAX = 0AH (* Returns Architectural Performance Monitoring leaf. *)
- CPUID.EAX = 0BH (* Returns Extended Topology Enumeration leaf. *)
- CPUID.EAX = 0CH (* INVALID: Returns the same information as CPUID.EAX = 0BH. *)
- CPUID.EAX = 80000008H (* Returns linear/physical address size data. *)
- CPUID.EAX = 8000000AH (* INVALID: Returns same information as CPUID.EAX = 0BH. *)

If a value entered for CPUID.EAX is less than or equal to the maximum input value and the leaf is not supported on that processor then 0 is returned in all the registers. For example, using the Intel Core i7 processor, the following is true:

**1.** On Intel 64 processors, CPUID clears the high 32 bits of the RAX/RBX/RCX/RDX registers in all modes.
CPUID.EAX = 07H (*Returns EAX=EBX=ECX=EDX=0. *)

When CPUID returns the highest basic leaf information as a result of an invalid input EAX value, any dependence on input ECX value in the basic leaf is honored.

CPUID can be executed at any privilege level to serialize instruction execution. Serializing instruction execution guarantees that any modifications to flags, registers, and memory for previous instructions are completed before the next instruction is fetched and executed.

See also:

“Serializing Instructions” in Chapter 8, “Multiple-Processor Management,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A

“Caching Translation Information” in Chapter 4, “Paging,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A

Table 3-20. Information Returned by CPUID Instruction

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0H</td>
<td>Basic CPUID Information</td>
</tr>
<tr>
<td>EAX</td>
<td>Maximum Input Value for Basic CPUID Information (see Table 3-21)</td>
</tr>
<tr>
<td>EBX</td>
<td>“Genu”</td>
</tr>
<tr>
<td>ECX</td>
<td>“intel”</td>
</tr>
<tr>
<td>EDX</td>
<td>“intel”</td>
</tr>
<tr>
<td>01H</td>
<td>Version Information: Type, Family, Model, and Stepping ID (see Figure 3-6)</td>
</tr>
<tr>
<td>EAX</td>
<td>Bits 7-0: Brand Index</td>
</tr>
<tr>
<td></td>
<td>Bits 15-8: CLFLUSH line size (Value * 8 = cache line size in bytes)</td>
</tr>
<tr>
<td></td>
<td>Bits 23-16: Maximum number of addressable IDs for logical processors in this physical package*</td>
</tr>
<tr>
<td></td>
<td>Bits 31-24: Initial APIC ID</td>
</tr>
<tr>
<td>EBX</td>
<td>Feature Information (see Figure 3-7 and Table 3-23)</td>
</tr>
<tr>
<td>ECX</td>
<td>Feature Information (see Figure 3-8 and Table 3-24)</td>
</tr>
<tr>
<td>EDX</td>
<td>Feature Information (see Figure 3-8 and Table 3-24)</td>
</tr>
<tr>
<td>NOTES:</td>
<td>* The nearest power-of-two integer that is not smaller than EBX[23:16] is the number of unique initial APIC IDs reserved for addressing different logical processors in a physical package.</td>
</tr>
<tr>
<td>02H</td>
<td>Cache and TLB Information (see Table 3-25)</td>
</tr>
<tr>
<td>EAX</td>
<td>Cache and TLB Information</td>
</tr>
<tr>
<td>EBX</td>
<td>Cache and TLB Information</td>
</tr>
<tr>
<td>ECX</td>
<td>Cache and TLB Information</td>
</tr>
<tr>
<td>EDX</td>
<td>Cache and TLB Information</td>
</tr>
</tbody>
</table>
### Table 3-20. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>03H</td>
<td></td>
</tr>
<tr>
<td>EAX</td>
<td>Reserved.</td>
</tr>
<tr>
<td>EBX</td>
<td>Reserved.</td>
</tr>
<tr>
<td>ECX</td>
<td>Bits 00-31 of 96 bit processor serial number. (Available in Pentium III processor only; otherwise, the value in this register is reserved.)</td>
</tr>
<tr>
<td>EDX</td>
<td>Bits 32-63 of 96 bit processor serial number. (Available in Pentium III processor only; otherwise, the value in this register is reserved.)</td>
</tr>
</tbody>
</table>

**NOTES:**
Processor serial number (PSN) is not supported in the Pentium 4 processor or later. On all models, use the PSN flag (returned using CPUID) to check for PSN support before accessing the feature.

See AP-485, *Intel Processor Identification and the CPUID Instruction* (Order Number 241618) for more information on PSN.

CPUID leaves $> 3 < 80000000$ are visible only when IA32_MISC_ENABLES.BOOT_NT4[bit 22] = 0 (default).

#### Deterministic Cache Parameters Leaf

<table>
<thead>
<tr>
<th>EAX Bits 4-0: Cache Type Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 = Null - No more caches</td>
</tr>
<tr>
<td>1 = Data Cache</td>
</tr>
<tr>
<td>2 = Instruction Cache</td>
</tr>
<tr>
<td>3 = Unified Cache</td>
</tr>
<tr>
<td>4-31 = Reserved</td>
</tr>
</tbody>
</table>

Bits 7-5: Cache Level (starts at 1)
Bits 8: Self Initializing cache level (does not need SW initialization)
Bits 9: Fully Associative cache

Bits 13-10: Reserved

Bits 25-14: Maximum number of addressable IDs for logical processors sharing this cache*, **

Bits 31-26: Maximum number of addressable IDs for processor cores in the physical package*, ***, ****

| EBX Bits 11-00: L = System Coherency Line Size* |
|-------|---------------------------------------------|
| Bits 21-12: P = Physical Line partitions*       |
| Bits 31-22: W = Ways of associativity*          |
### Table 3-20. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECX</td>
<td>Bits 31-00: $S = \text{Number of Sets}$*</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>EDX</th>
<th>Bit 0: Write-Back Invalidate/Invalidate</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 = WBINVD/INVD from threads sharing this cache acts upon lower level caches for threads sharing this cache</td>
</tr>
<tr>
<td></td>
<td>1 = WBINVD/INVD is not guaranteed to act upon lower level caches of non-originating threads sharing this cache.</td>
</tr>
<tr>
<td></td>
<td>Bit 1: Cache Inclusiveness</td>
</tr>
<tr>
<td></td>
<td>0 = Cache is not inclusive of lower cache levels.</td>
</tr>
<tr>
<td></td>
<td>1 = Cache is inclusive of lower cache levels.</td>
</tr>
<tr>
<td></td>
<td>Bits 31-02: Reserved = 0</td>
</tr>
</tbody>
</table>

**NOTES:**

* Add one to the return value to get the result.

** The nearest power-of-2 integer that is not smaller than $(1 + EAX[25:14])$ is the number of unique initial APIC IDs reserved for addressing different logical processors sharing this cache.

*** The nearest power-of-2 integer that is not smaller than $(1 + EAX[31:26])$ is the number of unique Core_IDs reserved for addressing different processor cores in a physical package. Core ID is a subset of bits of the initial APIC ID.

**** The returned value is constant for valid initial values in ECX. Valid ECX values start from 0.

### MONITOR/MWAIT Leaf

<table>
<thead>
<tr>
<th>05H</th>
<th>EAX</th>
<th>Bits 15-00: Smallest monitor-line size in bytes (default is processor's monitor granularity)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Bits 31-16: Reserved = 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>EBX</th>
<th>Bits 15-00: Largest monitor-line size in bytes (default is processor's monitor granularity)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Bits 31-16: Reserved = 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ECX</th>
<th>Bit 00: Enumeration of Monitor-Mwait extensions (beyond EAX and EBX registers) supported</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Bit 01: Supports treating interrupts as break-event for MWAIT, even when interrupts disabled</td>
</tr>
<tr>
<td></td>
<td>Bits 31 - 02: Reserved</td>
</tr>
</tbody>
</table>

---
Table 3-20. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
</table>
| EDX               | Bits 03 - 00: Number of C0* sub C-states supported using MWAIT  
|                   | Bits 07 - 04: Number of C1* sub C-states supported using MWAIT  
|                   | Bits 11 - 08: Number of C2* sub C-states supported using MWAIT  
|                   | Bits 15 - 12: Number of C3* sub C-states supported using MWAIT  
|                   | Bits 19 - 16: Number of C4* sub C-states supported using MWAIT  
|                   | Bits 31 - 20: Reserved = 0  
| NOTE:             | * The definition of C0 through C4 states for MWAIT extension are processor-specific C-states, not ACPI C-states. |
| Thermal and Power Management Leaf | |
| 06H EAX           | Bit 00: Digital temperature sensor is supported if set  
|                   | Bit 01: Intel Turbo Boost Technology Available (see description of IA32_MISC_ENABLES[38]).  
|                   | Bit 02: ARAT. APIC-Timer-always-running feature is supported if set.  
|                   | Bits 31 - 03: Reserved  
| EBX               | Bits 03 - 00: Number of Interrupt Thresholds in Digital Thermal Sensor  
|                   | Bits 31 - 04: Reserved  
| ECX               | Bit 00: Hardware Coordination Feedback Capability (Presence of IA32_MPERF and IA32_APERF). The capability to provide a measure of delivered processor performance (since last reset of the counters), as a percentage of expected processor performance at frequency specified in CPUID Brand String  
|                   | Bits 02 - 01: Reserved = 0  
|                   | Bit 03: The processor supports performance-energy bias preference if CPUID.06H.ECX.SETBH[bit 3] is set and it also implies the presence of a new architectural MSR called IA32_ENERGY_PERF_BIAS (1B0H)  
| EDX               | Bits 31 - 04: Reserved = 0  
| Direct Cache Access Information Leaf | |
| 09H EAX           | Value of bits [31:0] of IA32_PLATFORM_DCA_CAP MSR (address 1F8H)  
| EBX               | Reserved  
| ECX               | Reserved  
| EDX               | Reserved  
<p>| Architectural Performance Monitoring Leaf | |</p>
<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0AH EAX</td>
<td>Bits 07 - 00: Version ID of architectural performance monitoring Bits 15- 08: Number of general-purpose performance monitoring counter per logical processor Bits 23 - 16: Bit width of general-purpose, performance monitoring counter Bits 31 - 24: Length of EBX bit vector to enumerate architectural performance monitoring events</td>
</tr>
<tr>
<td>EBX</td>
<td>Bit 0: Core cycle event not available if 1 Bit 1: Instruction retired event not available if 1 Bit 2: Reference cycles event not available if 1 Bit 3: Last-level cache reference event not available if 1 Bit 4: Last-level cache misses event not available if 1 Bit 5: Branch instruction retired event not available if 1 Bit 6: Branch mispredict retired event not available if 1 Bits 31 - 07: Reserved = 0</td>
</tr>
<tr>
<td>ECX</td>
<td>Reserved = 0</td>
</tr>
<tr>
<td>EDX</td>
<td>Bits 04 - 00: Number of fixed-function performance counters (if Version ID &gt; 1) Bits 12- 05: Bit width of fixed-function performance counters (if Version ID &gt; 1) Reserved = 0</td>
</tr>
</tbody>
</table>

**Extended Topology Enumeration Leaf**

| 0BH EAX           | Bits 4-0: Number of bits to shift right on x2APIC ID to get a unique topology ID of the next level type*. All logical processors with the same next level ID share current level. Bits 31-5: Reserved. |
| EBX               | Bits 15 - 00: Number of logical processors at this level type. The number reflects configuration as shipped by Intel**. Bits 31 - 16: Reserved. |
| ECX               | Bits 07 - 00: Level number. Same value in ECX input Bits 15 - 08: Level type***. Bits 31 - 16: Reserved. |

**NOTES:**
1. Most of Leaf 0BH output depends on the initial value in ECX.
2. EDX output do not vary with initial value in ECX.
3. ECX[7:0] output always reflect initial value in ECX.
4. All other output value for an invalid initial value in ECX are 0.
5. Leaf 0BH exists if EBX[15:0] is not zero.
**CPUID—CPU Identification**

**NOTES:**

* Software should use this field (EAX[4:0]) to enumerate processor topology of the system.

** Software must not use EBX[15:0] to enumerate processor topology of the system. This value in this field (EBX[15:0]) is only intended for display/diagnostic purposes. The actual number of logical processors available to BIOS/OS/Applications may be different from the value of EBX[15:0], depending on software and platform hardware configurations.

*** The value of the “level type” field is not related to level numbers in any way, higher “level type” values do not mean higher levels. Level type field has the following encoding:

- 0 : invalid
- 1 : SMT
- 2 : Core
- 3-255 : Reserved

### Table 3-20. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EDX</strong></td>
<td>Bits 31-0: x2APIC ID the current logical processor.</td>
</tr>
<tr>
<td><strong>NOTES:</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>* Software should use this field (EAX[4:0]) to enumerate processor topology of the system.</td>
</tr>
<tr>
<td></td>
<td>** Software must not use EBX[15:0] to enumerate processor topology of the system. This value in this field (EBX[15:0]) is only intended for display/diagnostic purposes. The actual number of logical processors available to BIOS/OS/Applications may be different from the value of EBX[15:0], depending on software and platform hardware configurations.</td>
</tr>
<tr>
<td></td>
<td>*** The value of the “level type” field is not related to level numbers in any way, higher “level type” values do not mean higher levels. Level type field has the following encoding:</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 : invalid</td>
</tr>
<tr>
<td></td>
<td>1 : SMT</td>
</tr>
<tr>
<td></td>
<td>2 : Core</td>
</tr>
<tr>
<td></td>
<td>3-255 : Reserved</td>
</tr>
</tbody>
</table>

**Processor Extended State Enumeration Main Leaf (EAX = ODH, ECX = 0)**

<table>
<thead>
<tr>
<th><strong>0DH</strong></th>
<th><strong>NOTES:</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EAX</strong></td>
<td>Leaf ODH main leaf (ECX = 0).</td>
</tr>
<tr>
<td><strong>EBX</strong></td>
<td>Bits 31-0: Reports the valid bit fields of the lower 32 bits of the XFEATURE_ENABLED_MASK register (XCR0). If a bit is 0, the corresponding bit field in XCR0 is reserved.</td>
</tr>
<tr>
<td><strong>ECX</strong></td>
<td>Bits 31-0: Maximum size (bytes) required by enabled features in XFEATURE_ENABLED_MASK (XCR0). May be different than ECX when features at the end of the save area are not enabled.</td>
</tr>
<tr>
<td><strong>EDX</strong></td>
<td>Bit 31-0: Maximum size (bytes) of the XSAVE/XRSTOR save area required by all supported features in the processor, i.e all the valid bit fields in XFEATURE_ENABLED_MASK. This includes the size needed for the XSAVE.HEADER.</td>
</tr>
<tr>
<td><strong>NOTES:</strong></td>
<td></td>
</tr>
</tbody>
</table>

**Processor Extended State Enumeration Sub-leaf (EAX = ODH, ECX = 1)**
<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>EAX</td>
<td>Reserved</td>
</tr>
<tr>
<td>EBX</td>
<td>Reserved</td>
</tr>
<tr>
<td>ECX</td>
<td>Reserved</td>
</tr>
<tr>
<td>EDX</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Processor Extended State Enumeration Sub-leaves (EAX = 0DH, ECX = n, n > 1)**

**NOTES:**
- Leaf 0DH output depends on the initial value in ECX.
- If ECX contains an invalid sub leaf index, EAX/EBX/ECX/EDX return 0.

**EAX**
- Bits 31-0: The size in bytes of the save area for an extended state feature associated with a valid sub-leaf index, \( n \). Each valid sub-leaf index maps to a valid bit in the XFEATURE_ENABLED_MASK register (XCR0) starting at bit position 2. This field reports 0 if the sub-leaf index, \( n \), is invalid*.

**EBX**
- Bits 31-0: The offset in bytes of the save area from the beginning of the XSAVE/XRSTOR area. This field reports 0 if the sub-leaf index, \( n \), is invalid*.

**ECX**
- This field reports 0 if the sub-leaf index, \( n \), is invalid*; otherwise it is reserved.

**EDX**
- This field reports 0 if the sub-leaf index, \( n \), is invalid*; otherwise it is reserved.

**Unimplemented CPUID Leaf Functions**

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>40000000H -</td>
<td>Invalid. No existing or future CPU will return processor identification or feature information if the initial EAX value is in the range 40000000H to 4FFFFFFFFH.</td>
</tr>
<tr>
<td>4FFFFFFFFF</td>
<td>H</td>
</tr>
</tbody>
</table>

**Extended Function CPUID Information**

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>80000000H</td>
<td>Maximum Input Value for Extended Function CPUID Information (see Table 3-21).</td>
</tr>
<tr>
<td>EAX</td>
<td>Reserved</td>
</tr>
<tr>
<td>EBX</td>
<td>Reserved</td>
</tr>
<tr>
<td>ECX</td>
<td>Reserved</td>
</tr>
<tr>
<td>EDX</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Table 3-20. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>80000001H</td>
<td>EAX: Extended Processor Signature and Feature Bits.</td>
</tr>
<tr>
<td></td>
<td>EBX: Reserved</td>
</tr>
<tr>
<td></td>
<td>ECX: Bit 0: LAHF/SAHF available in 64-bit mode</td>
</tr>
<tr>
<td></td>
<td>Bits 31-1 Reserved</td>
</tr>
<tr>
<td></td>
<td>EDX: Bits 10-0: Reserved</td>
</tr>
<tr>
<td></td>
<td>Bit 11: SYSCALL/SYSRET available (when in 64-bit mode)</td>
</tr>
<tr>
<td></td>
<td>Bits 19-12: Reserved</td>
</tr>
<tr>
<td></td>
<td>Bit 20: Execute Disable Bit available</td>
</tr>
<tr>
<td></td>
<td>Bits 26-21: Reserved</td>
</tr>
<tr>
<td></td>
<td>Bit 27: RDTSCP and IA32_TSC_AUX are available if 1</td>
</tr>
<tr>
<td></td>
<td>Bits 28: Reserved</td>
</tr>
<tr>
<td></td>
<td>Bit 29: Intel® 64 Architecture available if 1</td>
</tr>
<tr>
<td></td>
<td>Bits 31-30: Reserved</td>
</tr>
<tr>
<td>80000002H</td>
<td>EAX: Processor Brand String</td>
</tr>
<tr>
<td></td>
<td>EBX: Processor Brand String Continued</td>
</tr>
<tr>
<td></td>
<td>ECX: Processor Brand String Continued</td>
</tr>
<tr>
<td></td>
<td>EDX: Processor Brand String Continued</td>
</tr>
<tr>
<td>80000003H</td>
<td>EAX: Processor Brand String Continued</td>
</tr>
<tr>
<td></td>
<td>EBX: Processor Brand String Continued</td>
</tr>
<tr>
<td></td>
<td>ECX: Processor Brand String Continued</td>
</tr>
<tr>
<td></td>
<td>EDX: Processor Brand String Continued</td>
</tr>
<tr>
<td>80000004H</td>
<td>EAX: Processor Brand String Continued</td>
</tr>
<tr>
<td></td>
<td>EBX: Processor Brand String Continued</td>
</tr>
<tr>
<td></td>
<td>ECX: Processor Brand String Continued</td>
</tr>
<tr>
<td></td>
<td>EDX: Processor Brand String Continued</td>
</tr>
<tr>
<td>80000005H</td>
<td>EAX: Reserved = 0</td>
</tr>
<tr>
<td></td>
<td>EBX: Reserved = 0</td>
</tr>
<tr>
<td></td>
<td>ECX: Reserved = 0</td>
</tr>
<tr>
<td></td>
<td>EDX: Reserved = 0</td>
</tr>
<tr>
<td>80000006H</td>
<td>EAX: Reserved = 0</td>
</tr>
<tr>
<td></td>
<td>EBX: Reserved = 0</td>
</tr>
<tr>
<td></td>
<td>ECX: Bits 7-0: Cache Line size in bytes</td>
</tr>
<tr>
<td></td>
<td>Bits 15-12: L2 Associativity field *</td>
</tr>
<tr>
<td></td>
<td>Bits 31-16: Cache size in 1K units</td>
</tr>
<tr>
<td></td>
<td>EDX: Reserved = 0</td>
</tr>
</tbody>
</table>
INPUT EAX = 0: Returns CPUID's Highest Value for Basic Processor Information and the Vendor Identification String

When CPUID executes with EAX set to 0, the processor returns the highest value the CPUID recognizes for returning basic processor information. The value is returned in the EAX register (see Table 3-21) and is processor specific.

A vendor identification string is also returned in EBX, EDX, and ECX. For Intel processors, the string is “GenuineIntel” and is expressed:

EBX ← 756e6547h (* “Genu”, with G in the low four bits of BL *)
EDX ← 49656e69h (* “ineI”, with i in the low four bits of DL *)
ECX ← 6c65746eh (* “ntel”, with n in the low four bits of CL *)

INPUT EAX = 80000008H: Returns CPUID's Highest Value for Extended Processor

### Table 3-20. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NOTES:</strong></td>
<td></td>
</tr>
<tr>
<td>* L2 associativity field encodings:</td>
<td></td>
</tr>
<tr>
<td>00H - Disabled</td>
<td></td>
</tr>
<tr>
<td>01H - Direct mapped</td>
<td></td>
</tr>
<tr>
<td>02H - 2-way</td>
<td></td>
</tr>
<tr>
<td>04H - 4-way</td>
<td></td>
</tr>
<tr>
<td>06H - 8-way</td>
<td></td>
</tr>
<tr>
<td>08H - 16-way</td>
<td></td>
</tr>
<tr>
<td>0FH - Fully associative</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>80000007H</th>
<th>EAX</th>
<th>EBX</th>
<th>ECX</th>
<th>EDX</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Reserved = 0</td>
<td>Reserved = 0</td>
<td>Reserved = 0</td>
<td>Bits 7-0: Reserved = 0</td>
</tr>
<tr>
<td></td>
<td>Bit 8: Invariant TSC available if 1</td>
<td>Bits 31-9: Reserved = 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>80000008H</th>
<th>EAX</th>
<th>EBX</th>
<th>ECX</th>
<th>EDX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear/Physical Address size</td>
<td>Reserved = 0</td>
<td>Reserved = 0</td>
<td>Reserved = 0</td>
<td></td>
</tr>
<tr>
<td>Bits 7-0: #Physical Address Bits*</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits 15-8: #Linear Address Bits</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits 31-16: Reserved = 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

* If CPUID.80000008H:EAX[7:0] is supported, the maximum physical address number supported should come from this field.

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CPUID—CPU Identification
Information
When CPUID executes with EAX set to 0, the processor returns the highest value the processor recognizes for returning extended processor information. The value is returned in the EAX register (see Table 3-21) and is processor specific.

<table>
<thead>
<tr>
<th>Intel 64 or IA-32 Processors</th>
<th>Highest Value in EAX</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Basic Information</td>
</tr>
<tr>
<td>Earlier Intel486 Processors</td>
<td>CPUID Not Implemented</td>
</tr>
<tr>
<td>Later Intel486 Processors and Pentium Processors</td>
<td>01H</td>
</tr>
<tr>
<td>Pentium Pro and Pentium II Processors, Intel® Celeron® Processors</td>
<td>02H</td>
</tr>
<tr>
<td>Pentium III Processors</td>
<td>03H</td>
</tr>
<tr>
<td>Pentium 4 Processors</td>
<td>02H</td>
</tr>
<tr>
<td>Intel Xeon Processors</td>
<td>02H</td>
</tr>
<tr>
<td>Pentium M Processor</td>
<td>02H</td>
</tr>
<tr>
<td>Pentium 4 Processor supporting Hyper-Threading Technology</td>
<td>05H</td>
</tr>
<tr>
<td>Pentium D Processor (8xx)</td>
<td>05H</td>
</tr>
<tr>
<td>Pentium D Processor (9xx)</td>
<td>06H</td>
</tr>
<tr>
<td>Intel Core Duo Processor</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Core 2 Duo Processor</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Xeon Processor 3000, 5100, 5200, 5300, 5400 Series</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Core 2 Duo Processor 8000 Series</td>
<td>0DH</td>
</tr>
<tr>
<td>Intel Xeon Processor 5200, 5400 Series</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Atom Processor</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Core i7 Processor</td>
<td>0BH</td>
</tr>
</tbody>
</table>
IA32_BIOS_SIGN_ID Returns Microcode Update Signature

For processors that support the microcode update facility, the IA32_BIOS_SIGN_ID MSR is loaded with the update signature whenever CPUID executes. The signature is returned in the upper DWORD. For details, see Chapter 9 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*.

**INPUT EAX = 1: Returns Model, Family, Stepping Information**

When CPUID executes with EAX set to 1, version information is returned in EAX (see Figure 3-6). For example: model, family, and processor type for the Intel Xeon processor 5100 series is as follows:

- Model — 1111B
- Family — 0101B
- Processor Type — 00B

See Table 3-22 for available processor type values. Stepping IDs are provided as needed.

![Figure 3-6. Version Information Returned by CPUID in EAX](image)

**Table 3-22. Processor Type Field**

<table>
<thead>
<tr>
<th>Type</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original OEM Processor</td>
<td>00B</td>
</tr>
<tr>
<td>Intel OverDrive Processor</td>
<td>01B</td>
</tr>
</tbody>
</table>
**INSTRUCTION SET REFERENCE, A-M**

**Table 3-22. Processor Type Field**

<table>
<thead>
<tr>
<th>Type</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual processor (not applicable to Intel486 processors)</td>
<td>10B</td>
</tr>
<tr>
<td>Intel reserved</td>
<td>11B</td>
</tr>
</tbody>
</table>

**NOTE**

See Chapter 14 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for information on identifying earlier IA-32 processors.

The Extended Family ID needs to be examined only when the Family ID is 0FH. Integrate the fields into a display using the following rule:

\[
\text{IF Family\_ID} \neq 0FH \\
\text{THEN Displayed\_Family} = \text{Family\_ID}; \\
\text{ELSE Displayed\_Family} = \text{Extended\_Family\_ID} + \text{Family\_ID}; \\
\text{* Right justify and zero-extend 4-bit field. *}
\]

\[
\text{FI}; \\
\text{(* Show Display\_Family as HEX field. *)}
\]

The Extended Model ID needs to be examined only when the Family ID is 06H or 0FH. Integrate the field into a display using the following rule:

\[
\text{IF (Family\_ID} = 06H \text{or Family\_ID} = 0FH) \\
\text{THEN Displayed\_Model} = (\text{Extended\_Model\_ID} \ll 4) + \text{Model\_ID}; \\
\text{* Right justify and zero-extend 4-bit field; display Model\_ID as HEX field. *}
\]

\[
\text{ELSE Displayed\_Model} = \text{Model\_ID}; \\
\text{FI}; \\
\text{(* Show Display\_Model as HEX field. *)}
\]

**INPUT EAX = 1: Returns Additional Information in EBX**

When CPUID executes with EAX set to 1, additional information is returned to the EBX register:

- Brand index (low byte of EBX) — this number provides an entry into a brand string table that contains brand strings for IA-32 processors. More information about this field is provided later in this section.
- CLFLUSH instruction cache line size (second byte of EBX) — this number indicates the size of the cache line flushed with CLFLUSH instruction in 8-byte increments. This field was introduced in the Pentium 4 processor.
- Local APIC ID (high byte of EBX) — this number is the 8-bit ID that is assigned to the local APIC on the processor during power up. This field was introduced in the Pentium 4 processor.
**INPUT EAX = 1: Returns Feature Information in ECX and EDX**

When CPUID executes with EAX set to 1, feature information is returned in ECX and EDX.

- Figure 3-7 and Table 3-23 show encodings for ECX.
- Figure 3-8 and Table 3-24 show encodings for EDX.

For all feature flags, a 1 indicates that the feature is supported. Use Intel to properly interpret feature flags.

**NOTE**

Software must confirm that a processor feature is present using feature flags returned by CPUID prior to using the feature. Software should not depend on future offerings retaining all features.

![Figure 3-7. Feature Information Returned in the ECX Register](OM16524b)
### Table 3-23. Feature Information Returned in the ECX Register

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SSE3</td>
<td><strong>Streaming SIMD Extensions 3 (SSE3)</strong>: A value of 1 indicates the processor supports this technology.</td>
</tr>
<tr>
<td>1</td>
<td>PCLMULQDQ</td>
<td><strong>PCLMULQDQ</strong>: A value of 1 indicates the processor supports the PCLMULQDQ instruction</td>
</tr>
<tr>
<td>2</td>
<td>DTES64</td>
<td><strong>64-bit DS Area</strong>: A value of 1 indicates the processor supports DS area using 64-bit layout</td>
</tr>
<tr>
<td>3</td>
<td>MONITOR</td>
<td><strong>MONITOR/MWAIT</strong>: A value of 1 indicates the processor supports this feature.</td>
</tr>
<tr>
<td>4</td>
<td>DS-CPL</td>
<td><strong>CPL Qualified Debug Store</strong>: A value of 1 indicates the processor supports the extensions to the Debug Store feature to allow for branch message storage qualified by CPL.</td>
</tr>
<tr>
<td>5</td>
<td>VMX</td>
<td>Virtual Machine Extensions. A value of 1 indicates that the processor supports this technology</td>
</tr>
<tr>
<td>6</td>
<td>SMX</td>
<td><strong>Safer Mode Extensions</strong>: A value of 1 indicates that the processor supports this technology. See Chapter 6, “Safer Mode Extensions Reference”.</td>
</tr>
<tr>
<td>7</td>
<td>EST</td>
<td><strong>Enhanced Intel SpeedStep® technology</strong>: A value of 1 indicates that the processor supports this technology.</td>
</tr>
<tr>
<td>8</td>
<td>TM2</td>
<td><strong>Thermal Monitor 2</strong>: A value of 1 indicates whether the processor supports this technology.</td>
</tr>
<tr>
<td>9</td>
<td>SSSE3</td>
<td>A value of 1 indicates the presence of the Supplemental Streaming SIMD Extensions 3 (SSSE3). A value of 0 indicates the instruction extensions are not present in the processor</td>
</tr>
<tr>
<td>10</td>
<td>CNXT-ID</td>
<td><strong>L1 Context ID</strong>: A value of 1 indicates the L1 data cache mode can be set to either adaptive mode or shared mode. A value of 0 indicates this feature is not supported. See definition of the IA32_MISC_ENABLE MSR Bit 24 (L1 Data Cache Context Mode) for details.</td>
</tr>
<tr>
<td>11-12</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>13</td>
<td>CMPXCHG16B</td>
<td><strong>CMPXCHG16B Available</strong>: A value of 1 indicates that the feature is available. See the &quot;CMPXCHG16B/CMPXCHG16B—Compare and Exchange Bytes&quot; section in this chapter for a description.</td>
</tr>
<tr>
<td>14</td>
<td>xTPR Update Control</td>
<td><strong>xTPR Update Control</strong>: A value of 1 indicates that the processor supports changing IA32_MISC_ENABLES[bit 23].</td>
</tr>
<tr>
<td>15</td>
<td>PDCM</td>
<td><strong>Perfmon and Debug Capability</strong>: A value of 1 indicates the processor supports the performance and debug feature indication MSR IA32_PERF_CAPABILITIES.</td>
</tr>
<tr>
<td>16-17</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>Bit #</td>
<td>Mnemonic</td>
<td>Description</td>
</tr>
<tr>
<td>-------</td>
<td>----------</td>
<td>-------------</td>
</tr>
<tr>
<td>18</td>
<td>DCA</td>
<td>A value of 1 indicates the processor supports the ability to prefetch data from a memory mapped device.</td>
</tr>
<tr>
<td>19</td>
<td>SSE4.1</td>
<td>A value of 1 indicates that the processor supports SSE4.1.</td>
</tr>
<tr>
<td>20</td>
<td>SSE4.2</td>
<td>A value of 1 indicates that the processor supports SSE4.2.</td>
</tr>
<tr>
<td>21</td>
<td>x2APIC</td>
<td>A value of 1 indicates that the processor supports x2APIC feature.</td>
</tr>
<tr>
<td>22</td>
<td>MOVBE</td>
<td>A value of 1 indicates that the processor supports MOVBE instruction.</td>
</tr>
<tr>
<td>23</td>
<td>POPCNT</td>
<td>A value of 1 indicates that the processor supports the POPCNT instruction.</td>
</tr>
<tr>
<td>24</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>25</td>
<td>AES</td>
<td>A value of 1 indicates that the processor supports the AES instruction extensions.</td>
</tr>
<tr>
<td>26</td>
<td>XSAVE</td>
<td>A value of 1 indicates that the processor supports the XSAVE/XRSTOR processor extended states feature, the XSETBV/XGETBV instructions, and the XFEATURE_ENABLED_MASK register (XCR0).</td>
</tr>
<tr>
<td>27</td>
<td>OSXSAVE</td>
<td>A value of 1 indicates that the OS has enabled XSETBV/XGETBV instructions to access the XFEATURE_ENABLED_MASK register (XCR0), and support for processor extended state management using XSAVE/XRSTOR.</td>
</tr>
<tr>
<td>30-28</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>31</td>
<td>Not Used</td>
<td>Always return 0</td>
</tr>
</tbody>
</table>
Figure 3-8. Feature Information Returned in the EDX Register
**Table 3-24. More on Feature Information Returned in the EDX Register**

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>FPU</td>
<td><strong>Floating Point Unit On-Chip.</strong> The processor contains an x87 FPU.</td>
</tr>
<tr>
<td>1</td>
<td>VME</td>
<td><strong>Virtual 8086 Mode Enhancements.</strong> Virtual 8086 mode enhancements, including CR4.VME for controlling the feature, CR4.PVI for protected mode virtual interrupts, software interrupt indirection, expansion of the TSS with the software indirection bitmap, and EFLAGS.VIF and EFLAGS.VIP flags.</td>
</tr>
<tr>
<td>2</td>
<td>DE</td>
<td><strong>Debugging Extensions.</strong> Support for I/O breakpoints, including CR4.DE for controlling the feature, and optional trapping of accesses to DR4 and DR5.</td>
</tr>
<tr>
<td>3</td>
<td>PSE</td>
<td><strong>Page Size Extension.</strong> Large pages of size 4 MByte are supported, including CR4.PSE for controlling the feature, the defined dirty bit in PDE (Page Directory Entries), optional reserved bit trapping in CR3, PDEs, and PTEs.</td>
</tr>
<tr>
<td>4</td>
<td>TSC</td>
<td><strong>Time Stamp Counter.</strong> The RDTSC instruction is supported, including CR4.TSD for controlling privilege.</td>
</tr>
<tr>
<td>5</td>
<td>MSR</td>
<td><strong>Model Specific Registers RDMSR and WRMSR Instructions.</strong> The RDMSR and WRMSR instructions are supported. Some of the MSRs are implementation dependent.</td>
</tr>
<tr>
<td>6</td>
<td>PAE</td>
<td><strong>Physical Address Extension.</strong> Physical addresses greater than 32 bits are supported: extended page table entry formats, an extra level in the page translation tables is defined, 2-MByte pages are supported instead of 4 Mbyte pages if PAE bit is 1.</td>
</tr>
<tr>
<td>7</td>
<td>MCE</td>
<td><strong>Machine Check Exception.</strong> Exception 18 is defined for Machine Checks, including CR4.MCE for controlling the feature. This feature does not define the model-specific implementations of machine-check error logging, reporting, and processor shutdowns. Machine Check exception handlers may have to depend on processor version to do model specific processing of the exception, or test for the presence of the Machine Check feature.</td>
</tr>
<tr>
<td>8</td>
<td>CXB</td>
<td><strong>CMPXCHG8B Instruction.</strong> The compare-and-exchange 8 bytes (64 bits) instruction is supported (implicitly locked and atomic).</td>
</tr>
<tr>
<td>9</td>
<td>APIC</td>
<td><strong>APIC On-Chip.</strong> The processor contains an Advanced Programmable Interrupt Controller (APIC), responding to memory mapped commands in the physical address range FFFE0000H to FFFE0FFFH (by default - some processors permit the APIC to be relocated).</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>11</td>
<td>SEP</td>
<td><strong>SYSENTER and SYSEXIT Instructions.</strong> The SYSENTER and SYSEXIT and associated MSRs are supported.</td>
</tr>
<tr>
<td>12</td>
<td>MTRR</td>
<td><strong>Memory Type Range Registers.</strong> MTRRs are supported. The MTRRcap MSR contains feature bits that describe what memory types are supported, how many variable MTRRs are supported, and whether fixed MTRRs are supported.</td>
</tr>
</tbody>
</table>
Table 3-24. More on Feature Information Returned in the EDX Register (Contd.)

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>PGE</td>
<td><strong>Page Global Bit.</strong> The global bit is supported in paging-structure entries (PDEs and PTEs) that map a page, indicating TLB entries that are common to different processes and need not be flushed. The CR4.PGE bit controls this feature.</td>
</tr>
<tr>
<td>14</td>
<td>MCA</td>
<td><strong>Machine Check Architecture.</strong> The Machine Check Architecture, which provides a compatible mechanism for error reporting in P6 family, Pentium 4, Intel Xeon processors, and future processors, is supported. The MCG_CAP MSR contains feature bits describing how many banks of error reporting MSRs are supported.</td>
</tr>
<tr>
<td>15</td>
<td>CMOV</td>
<td><strong>Conditional Move Instructions.</strong> The conditional move instruction CMOV is supported. In addition, if x87 FPU is present as indicated by the CPUID.FPU feature bit, then the FCOMI and FCMOV instructions are supported.</td>
</tr>
<tr>
<td>16</td>
<td>PAT</td>
<td><strong>Page Attribute Table.</strong> Page Attribute Table is supported. This feature augments the Memory Type Range Registers (MTRRs), allowing an operating system to specify attributes of memory accessed through a linear address on a 4KB granularity.</td>
</tr>
<tr>
<td>17</td>
<td>PSE-36</td>
<td><strong>36-Bit Page Size Extension.</strong> 4-MByte pages addressing physical memory beyond 4 GBytes are supported with 32-bit paging. This feature indicates that upper bits of the physical address of a 4-MByte page are encoded in bits 20:13 of the page-directory entry. Such physical addresses are limited by MAXPHYADDR and may be up to 40 bits in size.</td>
</tr>
<tr>
<td>18</td>
<td>PSN</td>
<td><strong>Processor Serial Number.</strong> The processor supports the 96-bit processor identification number feature and the feature is enabled.</td>
</tr>
<tr>
<td>19</td>
<td>CLFSH</td>
<td><strong>CLFLUSH Instruction.</strong> CLFLUSH Instruction is supported.</td>
</tr>
<tr>
<td>20</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>21</td>
<td>DS</td>
<td><strong>Debug Store.</strong> The processor supports the ability to write debug information into a memory resident buffer. This feature is used by the branch trace store (BTS) and precise event-based sampling (PEBS) facilities (see Chapter 20, &quot;Introduction to Virtual-Machine Extensions,&quot; in the Intel 64 and IA-32 Architectures Software Developer's Manual, Volume 3B).</td>
</tr>
<tr>
<td>22</td>
<td>ACPI</td>
<td><strong>Thermal Monitor and Software Controlled Clock Facilities.</strong> The processor implements internal MSRs that allow processor temperature to be monitored and processor performance to be modulated in predefined duty cycles under software control.</td>
</tr>
<tr>
<td>23</td>
<td>MMX</td>
<td><strong>Intel MMX Technology.</strong> The processor supports the Intel MMX technology.</td>
</tr>
</tbody>
</table>
When CPUID executes with EAX set to 2, the processor returns information about the processor’s internal TLBs, cache and prefetch hardware in the EAX, EBX, ECX, and EDX registers. The information is reported in encoded form and fall into the following categories:

- The least-significant byte in register EAX (register AL) indicates the number of times the CPUID instruction must be executed with an input value of 2 to get a complete description of the processor’s TLB/Cache/Prefetch hardware. The Intel Xeon processor 7400 series will return a 1.
- The most significant bit (bit 31) of each register indicates whether the register contains valid information (set to 0) or is reserved (set to 1).
- If a register contains valid information, the information is contained in 1 byte descriptors. There are four types of encoding values for the byte descriptor, the encoding type is noted in the second column of Table 3-25. Table 3-25 lists the encoding of these descriptors. Note that the order of descriptors in the EAX, EBX, ECX, and EDX registers is not defined; that is, specific bytes are not designated to contain descriptors for specific cache, prefetch, or TLB types. The descriptors

---

**Table 3-24. More on Feature Information Returned in the EDX Register (Contd.)**

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>FXSR</td>
<td><strong>FXSAVE and FXRSTOR Instructions.</strong> The FXSAVE and FXRSTOR instructions are supported for fast save and restore of the floating point context. Presence of this bit also indicates that CR4.OSFXSR is available for an operating system to indicate that it supports the FXSAVE and FXRSTOR instructions.</td>
</tr>
<tr>
<td>25</td>
<td>SSE</td>
<td><strong>SSE.</strong> The processor supports the SSE extensions.</td>
</tr>
<tr>
<td>26</td>
<td>SSE2</td>
<td><strong>SSE2.</strong> The processor supports the SSE2 extensions.</td>
</tr>
<tr>
<td>27</td>
<td>SS</td>
<td><strong>Self Snoop.</strong> The processor supports the management of conflicting memory types by performing a snoop of its own cache structure for transactions issued to the bus.</td>
</tr>
<tr>
<td>28</td>
<td>HTT</td>
<td><strong>Multi-Threading.</strong> The physical processor package is capable of supporting more than one logical processor.</td>
</tr>
<tr>
<td>29</td>
<td>TM</td>
<td><strong>Thermal Monitor.</strong> The processor implements the thermal monitor automatic thermal control circuitry (TCC).</td>
</tr>
<tr>
<td>30</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>31</td>
<td>PBE</td>
<td><strong>Pending Break Enable.</strong> The processor supports the use of the FERR#/PBE# pin when the processor is in the stop-clock state (STPCLK# is asserted) to signal the processor that an interrupt is pending and that the processor should return to normal operation to handle the interrupt. Bit 10 (PBE enable) in the IA32_MISC_ENABLE MSR enables this capability.</td>
</tr>
</tbody>
</table>
may appear in any order. Note also a processor may report a general descriptor type (FFH) and not report any byte descriptor of "cache type" via CPUID leaf 2.

### Table 3-25. Encoding of CPUID Leaf 2 Descriptors

<table>
<thead>
<tr>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00H</td>
<td>General</td>
<td>Null descriptor, this byte contains no information</td>
</tr>
<tr>
<td>01H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte pages, 4-way set associative, 32 entries</td>
</tr>
<tr>
<td>02H</td>
<td>TLB</td>
<td>Instruction TLB: 4 MByte pages, fully associative, 2 entries</td>
</tr>
<tr>
<td>03H</td>
<td>TLB</td>
<td>Data TLB: 4 KByte pages, 4-way set associative, 64 entries</td>
</tr>
<tr>
<td>04H</td>
<td>TLB</td>
<td>Data TLB: 4 MByte pages, 4-way set associative, 8 entries</td>
</tr>
<tr>
<td>05H</td>
<td>TLB</td>
<td>Data TLB: 4 MByte pages, 4-way set associative, 32 entries</td>
</tr>
<tr>
<td>06H</td>
<td>Cache</td>
<td>1st-level instruction cache: 8 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>08H</td>
<td>Cache</td>
<td>1st-level instruction cache: 16 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>09H</td>
<td>Cache</td>
<td>1st-level instruction cache: 32KBytes, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>0AH</td>
<td>Cache</td>
<td>1st-level data cache: 8 KBytes, 2-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>0BH</td>
<td>TLB</td>
<td>Instruction TLB: 4 MByte pages, 4-way set associative, 4 entries</td>
</tr>
<tr>
<td>0CH</td>
<td>Cache</td>
<td>1st-level data cache: 16 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>0DH</td>
<td>Cache</td>
<td>1st-level data cache: 16 KBytes, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>0EH</td>
<td>Cache</td>
<td>1st-level data cache: 24 KBytes, 6-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>21H</td>
<td>Cache</td>
<td>2nd-level cache: 256 KBytes, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>22H</td>
<td>Cache</td>
<td>3rd-level cache: 512 KBytes, 4-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>23H</td>
<td>Cache</td>
<td>3rd-level cache: 1 MBytes, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>25H</td>
<td>Cache</td>
<td>3rd-level cache: 2 MBytes, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>29H</td>
<td>Cache</td>
<td>3rd-level cache: 4 MBytes, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>2CH</td>
<td>Cache</td>
<td>1st-level data cache: 32 KBytes, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>30H</td>
<td>Cache</td>
<td>1st-level instruction cache: 32 KBytes, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>40H</td>
<td>Cache</td>
<td>No 2nd-level cache or, if processor contains a valid 2nd-level cache, no 3rd-level cache</td>
</tr>
<tr>
<td>41H</td>
<td>Cache</td>
<td>2nd-level cache: 128 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>42H</td>
<td>Cache</td>
<td>2nd-level cache: 256 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>43H</td>
<td>Cache</td>
<td>2nd-level cache: 512 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>44H</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 4-way set associative, 32 byte line size</td>
</tr>
</tbody>
</table>
## Table 3-25. Encoding of CPUID Leaf 2 Descriptors (Contd.)

<table>
<thead>
<tr>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>45H</td>
<td>Cache</td>
<td>2nd-level cache: 2 MByte, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>46H</td>
<td>Cache</td>
<td>3rd-level cache: 4 MByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>47H</td>
<td>Cache</td>
<td>3rd-level cache: 8 MByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>48H</td>
<td>Cache</td>
<td>3rd-level cache: 3MByte, 12-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>49H</td>
<td>Cache</td>
<td>3rd-level cache: 4MB, 16-way set associative, 64-byte line size (Intel Xeon processor MP, Family 0FH, Model 06H); 2nd-level cache: 4 MByte, 16-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4AH</td>
<td>Cache</td>
<td>3rd-level cache: 6MByte, 12-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4BH</td>
<td>Cache</td>
<td>3rd-level cache: 8MByte, 16-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4CH</td>
<td>Cache</td>
<td>3rd-level cache: 12MByte, 12-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4DH</td>
<td>Cache</td>
<td>3rd-level cache: 16MByte, 16-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4EH</td>
<td>Cache</td>
<td>2nd-level cache: 6MByte, 24-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4FH</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte pages, 32 entries</td>
</tr>
<tr>
<td>50H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte and 2-MByte or 4-MByte pages, 64 entries</td>
</tr>
<tr>
<td>51H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte and 2-MByte or 4-MByte pages, 128 entries</td>
</tr>
<tr>
<td>52H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte and 2-MByte or 4-MByte pages, 256 entries</td>
</tr>
<tr>
<td>55H</td>
<td>TLB</td>
<td>Instruction TLB: 2-MByte or 4-MByte pages, fully associative, 7 entries</td>
</tr>
<tr>
<td>56H</td>
<td>TLB</td>
<td>Data TLB0: 4 MByte pages, 4-way set associative, 16 entries</td>
</tr>
<tr>
<td>57H</td>
<td>TLB</td>
<td>Data TLB0: 4 KByte pages, 4-way associative, 16 entries</td>
</tr>
<tr>
<td>59H</td>
<td>TLB</td>
<td>Data TLB0: 4 KByte pages, fully associative, 16 entries</td>
</tr>
<tr>
<td>5AH</td>
<td>TLB</td>
<td>Data TLB0: 2-MByte or 4 MByte pages, 4-way set associative, 32 entries</td>
</tr>
<tr>
<td>5BH</td>
<td>TLB</td>
<td>Data TLB: 4 KByte and 4 MByte pages, 64 entries</td>
</tr>
<tr>
<td>5CH</td>
<td>TLB</td>
<td>Data TLB: 4 KByte and 4 MByte pages,128 entries</td>
</tr>
<tr>
<td>5DH</td>
<td>TLB</td>
<td>Data TLB: 4 KByte and 4 MByte pages,256 entries</td>
</tr>
<tr>
<td>60H</td>
<td>Cache</td>
<td>1st-level data cache: 16 KByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>66H</td>
<td>Cache</td>
<td>1st-level data cache: 8 KByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>67H</td>
<td>Cache</td>
<td>1st-level data cache: 16 KByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>68H</td>
<td>Cache</td>
<td>1st-level data cache: 32 KByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>70H</td>
<td>Cache</td>
<td>Trace cache: 12 K-μop, 8-way set associative</td>
</tr>
<tr>
<td>71H</td>
<td>Cache</td>
<td>Trace cache: 16 K-μop, 8-way set associative</td>
</tr>
<tr>
<td>72H</td>
<td>Cache</td>
<td>Trace cache: 32 K-μop, 8-way set associative</td>
</tr>
<tr>
<td>78H</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 4-way set associative, 64 byte line size</td>
</tr>
</tbody>
</table>
### Table 3-25. Encoding of CPUID Leaf 2 Descriptors (Contd.)

<table>
<thead>
<tr>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>79H</td>
<td>Cache</td>
<td>2nd-level cache: 128 KByte, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>7AH</td>
<td>Cache</td>
<td>2nd-level cache: 256 KByte, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>7BH</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>7CH</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>7DH</td>
<td>Cache</td>
<td>2nd-level cache: 2 MByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>7FH</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 2-way set associative, 64-byte line size</td>
</tr>
<tr>
<td>80H</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 8-way set associative, 64-byte line size</td>
</tr>
<tr>
<td>82H</td>
<td>Cache</td>
<td>2nd-level cache: 256 KByte, 8-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>83H</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 8-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>84H</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 8-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>85H</td>
<td>Cache</td>
<td>2nd-level cache: 2 MByte, 8-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>86H</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>87H</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>B0H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte pages, 4-way set associative, 128 entries</td>
</tr>
<tr>
<td>B1H</td>
<td>TLB</td>
<td>Instruction TLB: 2M pages, 4-way, 8 entries or 4M pages, 4-way, 4 entries</td>
</tr>
<tr>
<td>B2H</td>
<td>TLB</td>
<td>Instruction TLB: 4KByte pages, 4-way set associative, 64 entries</td>
</tr>
<tr>
<td>B3H</td>
<td>TLB</td>
<td>Data TLB: 4 KByte pages, 4-way set associative, 128 entries</td>
</tr>
<tr>
<td>B4H</td>
<td>TLB</td>
<td>Data TLB1: 4 KByte pages, 4-way associative, 256 entries</td>
</tr>
<tr>
<td>BAH</td>
<td>TLB</td>
<td>Data TLB1: 4 KByte pages, 4-way associative, 64 entries</td>
</tr>
<tr>
<td>C0H</td>
<td>TLB</td>
<td>Data TLB: 4 KByte and 4 MByte pages, 4-way associative, 8 entries</td>
</tr>
<tr>
<td>CAH</td>
<td>STLB</td>
<td>Shared 2nd-Level TLB: 4 KByte pages, 4-way associative, 512 entries</td>
</tr>
<tr>
<td>E4H</td>
<td>Cache</td>
<td>3rd-level cache: 8 MByte, 16-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>F0H</td>
<td>Prefetch</td>
<td>64-Byte prefetching</td>
</tr>
<tr>
<td>F1H</td>
<td>Prefetch</td>
<td>128-Byte prefetching</td>
</tr>
<tr>
<td>FFH</td>
<td>General</td>
<td>CPUID leaf 2 does not report cache descriptor information, use CPUID leaf 4 to query cache parameters</td>
</tr>
</tbody>
</table>

#### Example 3-1. Example of Cache and TLB Interpretation

The first member of the family of Pentium 4 processors returns the following information about caches and TLBs when the CPUID executes with an input value of 2:
EAX  66 5B 50 01H
EBX  0H
ECX  0H
EDX  00 7A 70 00H

Which means:
• The least-significant byte (byte 0) of register EAX is set to 01H. This indicates that CPUID needs to be executed once with an input value of 2 to retrieve complete information about caches and TLBs.
• The most-significant bit of all four registers (EAX, EBX, ECX, and EDX) is set to 0, indicating that each register contains valid 1-byte descriptors.
• Bytes 1, 2, and 3 of register EAX indicate that the processor has:
  — 50H - a 64-entry instruction TLB, for mapping 4-KByte and 2-MByte or 4-MByte pages.
  — 5BH - a 64-entry data TLB, for mapping 4-KByte and 4-MByte pages.
  — 66H - an 8-KByte 1st level data cache, 4-way set associative, with a 64-Byte cache line size.
• The descriptors in registers EBX and ECX are valid, but contain NULL descriptors.
• Bytes 0, 1, 2, and 3 of register EDX indicate that the processor has:
  — 00H - NULL descriptor.
  — 70H - Trace cache: 12 K-μop, 8-way set associative.
  — 7AH - a 256-KByte 2nd level cache, 8-way set associative, with a sectored, 64-byte cache line size.
  — 00H - NULL descriptor.

INPUT EAX = 04H: Returns Deterministic Cache Parameters for Each Level

When CPUID executes with EAX set to 04H and ECX contains an index value, the processor returns encoded data that describe a set of deterministic cache parameters (for the cache level associated with the input in ECX). Valid index values start from 0.

Software can enumerate the deterministic cache parameters for each level of the cache hierarchy starting with an index value of 0, until the parameters report the value associated with the cache type field is 0. The architecturally defined fields reported by deterministic cache parameters are documented in Table 3-20.

This Cache Size in Bytes
\[= (\text{Ways} + 1) \times (\text{Partitions} + 1) \times (\text{Line Size} + 1) \times (\text{Sets} + 1)\]
\[= (\text{EBX}[31:22] + 1) \times (\text{EBX}[21:12] + 1) \times (\text{EBX}[11:0] + 1) \times (\text{EXC} + 1)\]
The CPUID leaf 04H also reports data that can be used to derive the topology of processor cores in a physical package. This information is constant for all valid index values. Software can query the raw data reported by executing CPUID with EAX=04H and ECX=0 and use it as part of the topology enumeration algorithm described in Chapter 8, “Multiple-Processor Management,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

**INPUT EAX = 05H: Returns MONITOR and MWAIT Features**

When CPUID executes with EAX set to 05H, the processor returns information about features available to MONITOR/MWAIT instructions. The MONITOR instruction is used for address-range monitoring in conjunction with MWAIT instruction. The MWAIT instruction optionally provides additional extensions for advanced power management. See Table 3-20.

**INPUT EAX = 06H: Returns Thermal and Power Management Features**

When CPUID executes with EAX set to 06H, the processor returns information about thermal and power management features. See Table 3-20.

**INPUT EAX = 09H: Returns Direct Cache Access Information**

When CPUID executes with EAX set to 09H, the processor returns information about Direct Cache Access capabilities. See Table 3-20.

**INPUT EAX = 0AH: Returns Architectural Performance Monitoring Features**

When CPUID executes with EAX set to 0AH, the processor returns information about support for architectural performance monitoring capabilities. Architectural performance monitoring is supported if the version ID (see Table 3-20) is greater than Pn 0. See Table 3-20.

For each version of architectural performance monitoring capability, software must enumerate this leaf to discover the programming facilities and the architectural performance events available in the processor. The details are described in Chapter 20, “Introduction to Virtual-Machine Extensions,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B.

**INPUT EAX = 0BH: Returns Extended Topology Information**

When CPUID executes with EAX set to 0BH, the processor returns information about extended topology enumeration data. Software must detect the presence of CPUID leaf 0BH by verifying (a) the highest leaf index supported by CPUID is >= 0BH, and (b) CPUID.0BH:EBX[15:0] reports a non-zero value. See Table 3-20.

**INPUT EAX = 0DH: Returns Processor Extended States Enumeration Information**

When CPUID executes with EAX set to 0DH and ECX = 0, the processor returns information about the bit-vector representation of all processor state extensions that are
supported in the processor and storage size requirements of the XSAVE/XRSTOR area. See Table 3-20.

When CPUID executes with EAX set to 0DH and ECX = n (n > 1, and is a valid sub-leaf index), the processor returns information about the size and offset of each processor extended state save area within the XSAVE/XRSTOR area. See Table 3-20. Software can use the forward-extendable technique depicted below to query the valid sub-leaves and obtain size and offset information for each processor extended state save area:

For i = 2 to 62 // sub-leaf 1 is reserved
    IF (CPUID.(EAX=0DH, ECX=0):VECTOR[i] = 1 ) // VECTOR is the 64-bit value of EDX:EAX
        Execute CPUID.(EAX=0DH, ECX = i) to examine size and offset for sub-leaf i;
    FI;

METHODS FOR RETURNING BRANDING INFORMATION

Use the following techniques to access branding information:

1. Processor brand string method; this method also returns the processor’s maximum operating frequency
2. Processor brand index; this method uses a software supplied brand string table.

These two methods are discussed in the following sections. For methods that are available in early processors, see Section: “Identification of Earlier IA-32 Processors” in Chapter 14 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

The Processor Brand String Method

Figure 3-9 describes the algorithm used for detection of the brand string. Processor brand identification software should execute this algorithm on all Intel 64 and IA-32 processors.

This method (introduced with Pentium 4 processors) returns an ASCII brand identification string and the maximum operating frequency of the processor to the EAX, EBX, ECX, and EDX registers.
How Brand Strings Work

To use the brand string method, execute CPUID with EAX input of 8000002H through 80000004H. For each input value, CPUID returns 16 ASCII characters using EAX, EBX, ECX, and EDX. The returned string will be NULL-terminated.

Table 3-26 shows the brand string that is returned by the first processor in the Pentium 4 processor family.
Table 3-26. Processor Brand String Returned with Pentium 4 Processor

<table>
<thead>
<tr>
<th>EAX Input Value</th>
<th>Return Values</th>
<th>ASCII Equivalent</th>
</tr>
</thead>
<tbody>
<tr>
<td>80000002H</td>
<td>EAX = 20202020H</td>
<td>&quot; &quot;</td>
</tr>
<tr>
<td></td>
<td>EBX = 20202020H</td>
<td>&quot; &quot;</td>
</tr>
<tr>
<td></td>
<td>ECX = 20202020H</td>
<td>&quot; &quot;</td>
</tr>
<tr>
<td></td>
<td>EDX = 6E492020H</td>
<td>&quot;nl &quot;</td>
</tr>
<tr>
<td>80000003H</td>
<td>EAX = 286C6574H</td>
<td>&quot;(let&quot;</td>
</tr>
<tr>
<td></td>
<td>EBX = 50202952H</td>
<td>&quot;P )R&quot;</td>
</tr>
<tr>
<td></td>
<td>ECX = 69746E65H</td>
<td>&quot;itne&quot;</td>
</tr>
<tr>
<td></td>
<td>EDX = 52286D75H</td>
<td>&quot;R(mu&quot;</td>
</tr>
<tr>
<td>80000004H</td>
<td>EAX = 20342029H</td>
<td>&quot; 4 )&quot;</td>
</tr>
<tr>
<td></td>
<td>EBX = 20555043H</td>
<td>&quot; UPC&quot;</td>
</tr>
<tr>
<td></td>
<td>ECX = 30303531H</td>
<td>&quot;0051&quot;</td>
</tr>
<tr>
<td></td>
<td>EDX = 007A484DH</td>
<td>&quot;\0zHM&quot;</td>
</tr>
</tbody>
</table>

Extracting the Maximum Processor Frequency from Brand Strings

Figure 3-10 provides an algorithm which software can use to extract the maximum processor operating frequency from the processor brand string.

**NOTE**

When a frequency is given in a brand string, it is the maximum qualified frequency of the processor, not the frequency at which the processor is currently running.
The Processor Brand Index Method

The brand index method (introduced with Pentium® III Xeon® processors) provides an entry point into a brand identification table that is maintained in memory by system software and is accessible from system- and user-level code. In this table, each brand index is associated with an ASCII brand identification string that identifies the official Intel family and model number of a processor.

When CPUID executes with EAX set to 1, the processor returns a brand index to the low byte in EBX. Software can then use this index to locate the brand identification string for the processor in the brand identification table. The first entry (brand index 0) in this table is reserved, allowing for backward compatibility with processors that...
do not support the brand identification feature. Starting with processor signature family ID = 0FH, model = 03H, brand index method is no longer supported. Use brand string method instead.

Table 3-27 shows brand indices that have identification strings associated with them.

**Table 3-27. Mapping of Brand Indices; and Intel 64 and IA-32 Processor Brand Strings**

<table>
<thead>
<tr>
<th>Brand Index</th>
<th>Brand String</th>
</tr>
</thead>
<tbody>
<tr>
<td>00H</td>
<td>This processor does not support the brand identification feature</td>
</tr>
<tr>
<td>01H</td>
<td>Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>02H</td>
<td>Intel(R) Pentium(R) III processor¹</td>
</tr>
<tr>
<td>03H</td>
<td>Intel(R) Pentium(R) III Xeon(R) processor; If processor signature = 000006B1h, then Intel(R) Celeron(R) processor</td>
</tr>
<tr>
<td>04H</td>
<td>Intel(R) Pentium(R) III processor</td>
</tr>
<tr>
<td>06H</td>
<td>Mobile Intel(R) Pentium(R) III processor-M</td>
</tr>
<tr>
<td>07H</td>
<td>Mobile Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>08H</td>
<td>Intel(R) Pentium(R) 4 processor</td>
</tr>
<tr>
<td>09H</td>
<td>Intel(R) Pentium(R) 4 processor</td>
</tr>
<tr>
<td>0AH</td>
<td>Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>0BH</td>
<td>Intel(R) Xeon(R) processor; If processor signature = 00000F13h, then Intel(R) Xeon(R) processor MP</td>
</tr>
<tr>
<td>0CH</td>
<td>Intel(R) Xeon(R) processor MP</td>
</tr>
<tr>
<td>0EH</td>
<td>Mobile Intel(R) Pentium(R) 4 processor-M; If processor signature = 00000F13h, then Intel(R) Xeon(R) processor</td>
</tr>
<tr>
<td>0FH</td>
<td>Mobile Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>11H</td>
<td>Mobile Genuine Intel(R) processor</td>
</tr>
<tr>
<td>12H</td>
<td>Intel(R) Celeron(R) M processor</td>
</tr>
<tr>
<td>13H</td>
<td>Mobile Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>14H</td>
<td>Intel(R) Celeron(R) processor</td>
</tr>
<tr>
<td>15H</td>
<td>Mobile Genuine Intel(R) processor</td>
</tr>
<tr>
<td>16H</td>
<td>Intel(R) Pentium(R) M processor</td>
</tr>
<tr>
<td>17H</td>
<td>Mobile Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>18H – 0FFH</td>
<td>RESERVED</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Indicates versions of these processors that were introduced after the Pentium III
IA-32 Architecture Compatibility

CPUID is not supported in early models of the Intel486 processor or in any IA-32 processor earlier than the Intel486 processor.

Operation

IA32_BIOS_SIGN_ID MSR ← Update with installed microcode revision number;

CASE (EAX) OF

EAX = 0:
    EAX ← Highest basic function input value understood by CPUID;
    EBX ← Vendor identification string;
    EDX ← Vendor identification string;
    ECX ← Vendor identification string;
    BREAK;

EAX = 1H:
    EAX[3:0] ← Stepping ID;
    EAX[7:4] ← Model;
    EAX[11:8] ← Family;
    EAX[13:12] ← Processor type;
    EAX[15:14] ← Reserved;
    EAX[19:16] ← Extended Model;
    EAX[27:20] ← Extended Family;
    EAX[31:28] ← Reserved;
    EBX[7:0] ← Brand Index; (* Reserved if the value is zero. *)
    EBX[15:8] ← CLFLUSH Line Size;
    EBX[16:23] ← Reserved; (* Number of threads enabled = 2 if MT enable fuse set. *)
    EBX[24:31] ← Initial APIC ID;
    ECX ← Feature flags; (* See Figure 3-7. *)
    EDX ← Feature flags; (* See Figure 3-8. *)
    BREAK;

EAX = 2H:
    EAX ← Cache and TLB information;
    EBX ← Cache and TLB information;
    ECX ← Cache and TLB information;
    EDX ← Cache and TLB information;
    BREAK;

EAX = 3H:
    EAX ← Reserved;
    EBX ← Reserved;
    ECX ← ProcessorSerialNumber[31:0];
    (* Pentium III processors only, otherwise reserved. *)
    EDX ← ProcessorSerialNumber[63:32];
    (* Pentium III processors only, otherwise reserved. *
BREAK
EAX = 4H:
    EAX ← Deterministic Cache Parameters Leaf; (* See Table 3-20. *)
    EBX ← Deterministic Cache Parameters Leaf;
    ECX ← Deterministic Cache Parameters Leaf;
    EDX ← Deterministic Cache Parameters Leaf;
BREAK;
EAX = 5H:
    EAX ← MONITOR/MWAIT Leaf; (* See Table 3-20. *)
    EBX ← MONITOR/MWAIT Leaf;
    ECX ← MONITOR/MWAIT Leaf;
    EDX ← MONITOR/MWAIT Leaf;
BREAK;
EAX = 6H:
    EAX ← Thermal and Power Management Leaf; (* See Table 3-20. *)
    EBX ← Thermal and Power Management Leaf;
    ECX ← Thermal and Power Management Leaf;
    EDX ← Thermal and Power Management Leaf;
BREAK;
EAX = 7H or 8H:
    EAX ← Reserved = 0;
    EBX ← Reserved = 0;
    ECX ← Reserved = 0;
    EDX ← Reserved = 0;
BREAK;
EAX = 9H:
    EAX ← Direct Cache Access Information Leaf; (* See Table 3-20. *)
    EBX ← Direct Cache Access Information Leaf;
    ECX ← Direct Cache Access Information Leaf;
    EDX ← Direct Cache Access Information Leaf;
BREAK;
EAX = AH:
    EAX ← Architectural Performance Monitoring Leaf; (* See Table 3-20. *)
    EBX ← Architectural Performance Monitoring Leaf;
    ECX ← Architectural Performance Monitoring Leaf;
    EDX ← Architectural Performance Monitoring Leaf;
BREAK
EAX = BH:
    EAX ← Extended Topology Enumeration Leaf; (* See Table 3-20. *)
    EBX ← Extended Topology Enumeration Leaf;
    ECX ← Extended Topology Enumeration Leaf;
    EDX ← Extended Topology Enumeration Leaf;
BREAK;
EAX = CH:
    EAX ← Reserved = 0;
    EBX ← Reserved = 0;
    ECX ← Reserved = 0;
    EDX ← Reserved = 0;
    BREAK;

EAX = DH:
    EAX ← Processor Extended State Enumeration Leaf; (* See Table 3-20. *)
    EBX ← Processor Extended State Enumeration Leaf;
    ECX ← Processor Extended State Enumeration Leaf;
    EDX ← Processor Extended State Enumeration Leaf;
    BREAK;
    BREAK;

EAX = 80000000H:
    EAX ← Highest extended function input value understood by CPUID;
    EBX ← Reserved;
    ECX ← Reserved;
    EDX ← Reserved;
    BREAK;

EAX = 80000001H:
    EAX ← Reserved;
    EBX ← Reserved;
    ECX ← Extended Feature Bits (* See Table 3-20.*);
    EDX ← Extended Feature Bits (* See Table 3-20.*);
    BREAK;

EAX = 80000002H:
    EAX ← Processor Brand String;
    EBX ← Processor Brand String, continued;
    ECX ← Processor Brand String, continued;
    EDX ← Processor Brand String, continued;
    BREAK;

EAX = 80000003H:
    EAX ← Processor Brand String, continued;
    EBX ← Processor Brand String, continued;
    ECX ← Processor Brand String, continued;
    EDX ← Processor Brand String, continued;
    BREAK;

EAX = 80000004H:
    EAX ← Processor Brand String, continued;
    EBX ← Processor Brand String, continued;
    ECX ← Processor Brand String, continued;
    EDX ← Processor Brand String, continued;
    BREAK;
**INSTRUCTION SET REFERENCE, A-M**

EAX = 80000005H:
  EAX ← Reserved = 0;
  EBX ← Reserved = 0;
  ECX ← Reserved = 0;
  EDX ← Reserved = 0;
BREAK;

EAX = 80000006H:
  EAX ← Reserved = 0;
  EBX ← Reserved = 0;
  ECX ← Cache information;
  EDX ← Reserved = 0;
BREAK;

EAX = 80000007H:
  EAX ← Reserved = 0;
  EBX ← Reserved = 0;
  ECX ← Reserved = 0;
  EDX ← Reserved = Misc Feature Flags;
BREAK;

EAX = 80000008H:
  EAX ← Reserved = Physical Address Size Information;
  EBX ← Reserved = Virtual Address Size Information;
  ECX ← Reserved = 0;
  EDX ← Reserved = 0;
BREAK;

EAX >= 40000000H and EAX <= 40FFFFFFH:
DEFAULT: (* EAX = Value outside of recognized range for CPUID. *)
  (* If the highest basic information leaf data depend on ECX input value, ECX is honored.*)
  EAX ← Reserved; (* Information returned for highest basic information leaf. *)
  EBX ← Reserved; (* Information returned for highest basic information leaf. *)
  ECX ← Reserved; (* Information returned for highest basic information leaf. *)
  EDX ← Reserved; (* Information returned for highest basic information leaf. *)
BREAK;
ESAC;

**Flags Affected**
None.

**Exceptions (All Operating Modes)**

#UD If the LOCK prefix is used.

In earlier IA-32 processors that do not support the CPUID instruction, execution of the instruction results in an invalid opcode (#UD) exception being generated.
**CRC32 — Accumulate CRC32 Value**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 38 F0 /r</td>
<td>CRC32 r32, r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Accumulate CRC32 on r/m8.</td>
</tr>
<tr>
<td>F2 REX 0F 38 F0 /r</td>
<td>CRC32 r32, r/m8*</td>
<td>Valid</td>
<td>N.E.</td>
<td>Accumulate CRC32 on r/m8.</td>
</tr>
<tr>
<td>F2 0F 38 F1 /r</td>
<td>CRC32 r32, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Accumulate CRC32 on r/m16.</td>
</tr>
<tr>
<td>F2 0F 38 F1 /r</td>
<td>CRC32 r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Accumulate CRC32 on r/m32.</td>
</tr>
<tr>
<td>F2 REX.W 0F 38 F0 /r</td>
<td>CRC32 r64, r/m8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Accumulate CRC32 on r/m8.</td>
</tr>
<tr>
<td>F2 REX.W 0F 38 F1 /r</td>
<td>CRC32 r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Accumulate CRC32 on r/m64.</td>
</tr>
</tbody>
</table>

**NOTES:**
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Description**

Starting with an initial value in the first operand (destination operand), accumulates a CRC32 (polynomial 0x11EDC6F41) value for the second operand (source operand) and stores the result in the destination operand. The source operand can be a register or a memory location. The destination operand must be an r32 or r64 register. If the destination is an r64 register, then the 32-bit result is stored in the least significant double word and 00000000H is stored in the most significant double word of the r64 register.

The initial value supplied in the destination operand is a double word integer stored in the r32 register or the least significant double word of the r64 register. To incrementally accumulate a CRC32 value, software retains the result of the previous CRC32 operation in the destination operand, then executes the CRC32 instruction again with new input data in the source operand. Data contained in the source operand is processed in reflected bit order. This means that the most significant bit of the source operand is treated as the least significant bit of the quotient, and so on, for all the bits of the source operand. Likewise, the result of the CRC operation is stored in the destination operand in reflected bit order. This means that the most significant bit of the resulting CRC (bit 31) is stored in the least significant bit of the destination operand (bit 0), and so on, for all the bits of the CRC.
INSTRUCTION SET REFERENCE, A-M

Operation

Notes:

BIT_REFLECT64: DST[63-0] = SRC[0-63]
BIT_REFLECT32: DST[31-0] = SRC[0-31]
BIT_REFLECT16: DST[15-0] = SRC[0-15]
BIT_REFLECT8: DST[7-0] = SRC[0-7]
MOD2: Remainder from Polynomial division modulus 2

CRC32 instruction for 64-bit source operand and 64-bit destination operand:

TEMP1[63-0] ← BIT_REFLECT64 (SRC[63-0])
TEMP2[31-0] ← BIT_REFLECT32 (DEST[31-0])
TEMP3[95-0] ← TEMP1[63-0] << 32
TEMP4[95-0] ← TEMP2[31-0] << 64
TEMP5[95-0] ← TEMP3[95-0] XOR TEMP4[95-0]
TEMP6[31-0] ← TEMP5[95-0] MOD2 11EDC6F41H
DEST[31-0] ← BIT_REFLECT (TEMP6[31-0])
DEST[63-32] ← 00000000H

CRC32 instruction for 32-bit source operand and 32-bit destination operand:

TEMP1[31-0] ← BIT_REFLECT32 (SRC[31-0])
TEMP2[31-0] ← BIT_REFLECT32 (DEST[31-0])
TEMP3[63-0] ← TEMP1[31-0] << 32
TEMP4[63-0] ← TEMP2[31-0] << 32
TEMP5[63-0] ← TEMP3[63-0] XOR TEMP4[63-0]
TEMP6[31-0] ← TEMP5[63-0] MOD2 11EDC6F41H
DEST[31-0] ← BIT_REFLECT (TEMP6[31-0])

CRC32 instruction for 16-bit source operand and 32-bit destination operand:

TEMP1[15-0] ← BIT_REFLECT16 (SRC[15-0])
TEMP2[31-0] ← BIT_REFLECT32 (DEST[31-0])
TEMP3[47-0] ← TEMP1[15-0] << 32
TEMP4[47-0] ← TEMP2[31-0] << 16
TEMP5[47-0] ← TEMP3[47-0] XOR TEMP4[47-0]
TEMP6[31-0] ← TEMP5[47-0] MOD2 11EDC6F41H
DEST[31-0] ← BIT_REFLECT (TEMP6[31-0])

CRC32 instruction for 8-bit source operand and 64-bit destination operand:

TEMP1[7-0] ← BIT_REFLECT8 (SRC[7-0])
TEMP2[31-0] ← BIT_REFLECT32 (DEST[31-0])
TEMP3[39-0] ← TEMP1[7-0] << 32
TEMP4[39-0] ← TEMP2[31-0] << 8
TEMP5[39-0] ← TEMP3[39-0] XOR TEMP4[39-0]
CRC32 — Accumulate CRC32 Value

```
TEMP6[31-0] ← TEMP5[39-0] MOD2 11EDC6F41H
DEST[31-0] ← BIT_REFLECT (TEMP6[31-0])
DEST[63-32] ← 00000000H
```

CRC32 instruction for 8-bit source operand and 32-bit destination operand:

```
TEMP1[7-0] ← BIT_REFLECT8(SRC[7-0])
TEMP2[31-0] ← BIT_REFLECT32 (DEST[31-0])
TEMP3[39-0] ← TEMP1[7-0] << 32
TEMP4[39-0] ← TEMP2[31-0] << 8
TEMP5[39-0] ← TEMP3[39-0] XOR TEMP4[39-0]
TEMP6[31-0] ← TEMP5[39-0] MOD2 11EDC6F41H
DEST[31-0] ← BIT_REFLECT (TEMP6[31-0])
```

**Flags Affected**

None

**Intel C/C++ Compiler Intrinsic Equivalent**

unsigned int _mm_crc32_u8( unsigned int crc, unsigned char data )
unsigned int _mm_crc32_u16( unsigned int crc, unsigned short data )
unsigned int _mm_crc32_u32( unsigned int crc, unsigned int data )
unsigned __int64 _mm_crc32_u64( unsigned __int64 crc, unsigned __int64 data )

**SIMD Floating Point Exceptions**

None

**Protected Mode Exceptions**

- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS or GS segments.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#PF (fault-code)**: For a page fault.
- **#UD**: If CPUID.01H:ECX.SSE4_2 [Bit 20] = 0.
  - If LOCK prefix is used.
  - If REP (F3H) prefix is used.

**Real Mode Exceptions**

- **#GP(0)**: If any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#UD**: If CPUID.01H:ECX.SSE4_2 [Bit 20] = 0.
If LOCK prefix is used.
If REP (F3H) prefix is used.

**Virtual 8086 Mode Exceptions**

#GP(0)  If any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF (fault-code)  For a page fault.
#UD  If CPUID.01H:ECX.SSE4_2 [Bit 20] = 0.
     If LOCK prefix is used.
     If REP (F3H) prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in Protected Mode.

**64-Bit Mode Exceptions**

#GP(0)  If the memory address is in a non-canonical form.
#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#PF (fault-code)  For a page fault.
#UD  If CPUID.01H:ECX.SSE4_2 [Bit 20] = 0.
     If LOCK prefix is used.
     If REP (F3H) prefix is used.
CVTDQ2PD—Convert Packed Dword Integers to Packed Double-Precision FP Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F E6</td>
<td>CVTDQ2PD xmm1, xmm2/m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert two packed signed doubleword integers from xmm2/m128 to two packed double-precision floating-point values in xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Converts two packed signed doubleword integers in the source operand (second operand) to two packed double-precision floating-point values in the destination operand (first operand).

The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. When the source operand is an XMM register, the packed integers are located in the low quadword of the register.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[31:0]);
DEST[127:64] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[63:32]);

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTDQ2PD	__m128d _mm_cvtepi32_pd(__m128i a)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- **#SS(0)** For an illegal address in the SS segment.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.

#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CVTDQ2PS—Convert Packed Dword Integers to Packed Single-Precision FP Values

Description
Converts four packed signed doubleword integers in the source operand (second operand) to four packed single-precision floating-point values in the destination operand (first operand).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. When a conversion is inexact, rounding is performed according to the rounding control bits in the MXCSR register.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[31:0]);
DEST[63:32] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[63:32]);
DEST[95:64] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[95:64]);
DEST[127:96] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[127:96]);

Intel C/C++ Compiler Intrinsic Equivalent
CVTDQ2PS __m128 _mm_cvtepi32_ps(__m128i a)

SIMD Floating-Point Exceptions
Precision.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For a illegal address in the SS segment.
#PF(fault-code) For a page fault.
INSTRUCTION SET REFERENCE, A-M

#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
 If CR0.EM[bit 2] = 1.
 If CR4.OSFXSR[bit 9] = 0.
 If CPUID.01H:EDX.SSE2[bit 26] = 0.
 If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
 If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
 If CR0.EM[bit 2] = 1.
 If CR4.OSFXSR[bit 9] = 0.
 If CPUID.01H:EDX.SSE2[bit 26] = 0.
 If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
 If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.
CVTPD2DQ—Convert Packed Double-Precision FP Values to Packed Dword Integers

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 OF E6</td>
<td>CVTPD2DQ xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert two packed double-precision floating-point values from xmm2/m128 to two packed signed doubleword integers in xmm1.</td>
</tr>
</tbody>
</table>

Description

Converts two packed double-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The result is stored in the low quadword of the destination operand and the high quadword is cleared to all 0s.

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer(SRC[63:0]);
DEST[63:32] ← Convert_Double_Precision_Floating_Point_To_Integer(SRC[127:64]);
DEST[127:64] ← 0000000000000000H;

Intel C/C++ Compiler Intrinsic Equivalent

CVTPD2DQ _m128i _mm_cvtpd_epi32(_m128d a)

SIMD Floating-Point Exceptions

Invalid, Precision.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
INSTRUCTION SET REFERENCE, A-M

CVTPD2DQ—Convert Packed Double-Precision FP Values to Packed Dword Integers

If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
   If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.
CVTPD2PI—Convert Packed Double-Precision FP Values to Packed Dword Integers

**Opcode**
66 0F 2D /r

**Instruction**
CVTPD2PI mm, xmm/m128

**64-Bit Mode**
Valid

**Compat/Leg Mode**
Valid

**Description**
Converts two packed double-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an MMX technology register.

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTPD2PI instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**
DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer32(SRC[63:0]);
DEST[63:32] ← Convert_Double_Precision_Floating_Point_To_Integer32(SRC[127:64]);

**Intel C/C++ Compiler Intrinsic Equivalent**
CVTPD1PI ___m64 __mm_cvtpd_pi32(___m128d a)

**SIMD Floating-Point Exceptions**
Invalid, Precision.
Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
   If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#MF If there is a pending x87 FPU exception.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
   If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

- **#SS(0)** If a memory address referencing the SS segment is in a non-canonical form.
- **#GP(0)** If the memory address is in a non-canonical form.
  If memory operand is not aligned on a 16-byte boundary, regardless of segment.
- **#PF(fault-code)** For a page fault.
- **#MF** If there is a pending x87 FPU exception.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.
CVTPD2PS—Convert Packed Double-Precision FP Values to Packed Single-Precision FP Values

**Description**

Converts two packed double-precision floating-point values in the source operand (second operand) to two packed single-precision floating-point values in the destination operand (first operand).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The result is stored in the low quadword of the destination operand, and the high quadword is cleared to all 0s. When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{Convert\_Double\_Precision\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[63:0]); \\
\text{DEST}[63:32] & \leftarrow \text{Convert\_Double\_Precision\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[127:64]); \\
\text{DEST}[127:64] & \leftarrow 0000000000000000H;
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTPD2PS 

`__m128 _mm_cvtpd_ps(__m128d a)`

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
CVTPD2PS—Convert Packed Double-Precision FP Values to Packed Single-Precision FP Values

INSTRUCTION SET REFERENCE, A-M

#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-M

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.

#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
CVTPI2PD—Convert Packed Dword Integers to Packed Double-Precision FP Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 2A /r</td>
<td>CVTPI2PD</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert two packed signed doubleword integers from mm/mem64 to two packed double-precision floating-point values in xmm.</td>
</tr>
</tbody>
</table>

**NOTES:**
* Operation is different for different operand sets; see the Description section.

**Description**
Converts two packed signed doubleword integers in the source operand (second operand) to two packed double-precision floating-point values in the destination operand (first operand).

The source operand can be an MMX technology register or a 64-bit memory location. The destination operand is an XMM register. In addition, depending on the operand configuration:

- **For operands xmm, mm:** the instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTPI2PD instruction is executed.

- **For operands xmm, m64:** the instruction does not cause a transition to MMX technology and does not take x87 FPU exceptions.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Intel C/C++ Compiler Intrinsic Equivalent**
CVTPI2PD __m128d _mm_cvtpi32_pd(__m64 a)

**SIMD Floating-Point Exceptions**
None.
Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#UD If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE2[bit 26] = 0.

If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#UD If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE2[bit 26] = 0.

If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.
CVTPI2PD—Convert Packed Dword Integers to Packed Double-Precision FP Values

INSTRUCTION SET REFERENCE, A-M

#MF If there is a pending x87 FPU exception.

#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CVTPI2PS—Convert Packed Dword Integers to Packed Single-Precision FP Values

Description

Converts two packed signed doubleword integers in the source operand (second operand) to two packed single-precision floating-point values in the destination operand (first operand).

The source operand can be an MMX technology register or a 64-bit memory location. The destination operand is an XMM register. The results are stored in the low quadword of the destination operand, and the high quadword remains unchanged. When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTPI2PS instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

\[
\text{DEST}[31:0] \leftarrow \text{Convert \_Integer\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[31:0]); \\
\text{DEST}[63:32] \leftarrow \text{Convert \_Integer\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[63:32]); \\
\text{(* High quadword of destination unchanged *)}
\]

Intel C/C++ Compiler Intrinsic Equivalent

CVTPI2PS

__m128_mm_cvtpi32_ps(__m128 a, __m64 b)

SIMD Floating-Point Exceptions

Precision.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

#SS(0) For an illegal address in the SS segment.
#PF(fault-code)   For a page fault.
#NM               If CR0.TS[bit 3] = 1.
#MF               If there is a pending x87 FPU exception.
#XM               If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD               If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
               If CR0.EM[bit 2] = 1.
               If CR4.OSFXSR[bit 9] = 0.
               If CPUID.01H:EDX.SSE[bit 25] = 0.
               If the LOCK prefix is used.
#AC(0)            If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP  If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM  If CR0.TS[bit 3] = 1.
#MF  If there is a pending x87 FPU exception.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
               If CR0.EM[bit 2] = 1.
               If CR4.OSFXSR[bit 9] = 0.
               If CPUID.01H:EDX.SSE[bit 25] = 0.
               If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code)   For a page fault.
#AC(0)            If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.

#MF  If there is a pending x87 FPU exception.

#XM  If an unmasked SIMD floating-point exception and CR4.OSXMMX[bit 10] = 1.

#UD  If an unmasked SIMD floating-point exception and CR4.OSXMMX[bit 10] = 0.

If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE[bit 25] = 0.

If the LOCK prefix is used.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
**CVTPS2DQ—Convert Packed Single-Precision FP Values to Packed Dword Integers**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 5B /r</td>
<td>CVTPS2DQ xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert four packed single-precision floating-point values from xmm2/m128 to four packed signed doubleword integers in xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Converts four packed single-precision floating-point values in the source operand (second operand) to four packed signed doubleword integers in the destination operand (first operand).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[31:0]);
DEST[63:32] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[63:32]);
DEST[95:64] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[95:64]);
DEST[127:96] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[127:96]);

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTPS2DQ _m128i _mm_cvtps_epi32(__m128 a)

**SIMD Floating-Point Exceptions**

Invalid, Precision.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
### INSTRUCTION SET REFERENCE, A-M

- **#SS(0)** For an illegal address in the SS segment.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
  - If the LOCK prefix is used.

#### Real-Address Mode Exceptions
- **#GP** If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
  - If any part of the operand lies outside the effective address space from 0 to FFFFH.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
  - If the LOCK prefix is used.

#### Virtual-8086 Mode Exceptions
- Same exceptions as in real address mode.
- **#PF(fault-code)** For a page fault.

#### Compatibility Mode Exceptions
- Same exceptions as in protected mode.

#### 64-Bit Mode Exceptions
- **#SS(0)** If a memory address referencing the SS segment is in a non-canonical form.
- **#GP(0)** If the memory address is in a non-canonical form.
CVTPS2DQ—Convert Packed Single-Precision FP Values to Packed Dword Integers

If memory operand is not aligned on a 16-byte boundary, regardless of segment.

- **#PF(fault-code)**: For a page fault.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR4.OFSXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
  - If the LOCK prefix is used.
CVTPS2PD—Convert Packed Single-Precision FP Values to Packed Double-Precision FP Values

Description
Converts two packed single-precision floating-point values in the source operand (second operand) to two packed double-precision floating-point values in the destination operand (first operand).

The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. When the source operand is an XMM register, the packed single-precision floating-point values are contained in the low quadword of the register.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST[63:0] ← Convert_Single_Precision_To_Double_Precision_Floating_Point(SRC[31:0]);
DEST[127:64] ← Convert_Single_Precision_To_Double_Precision_Floating_Point(SRC[63:32]);

Intel C/C++ Compiler Intrinsic Equivalent
CVTPS2PD __m128d _mm_cvtps_pd(__m128 a)

SIMD Floating-Point Exceptions
Invalid, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
CVTPS2PD—Convert Packed Single-Precision FP Values to Packed Double-Precision FP Values

INSTRUCTION SET REFERENCE, A-M

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CVTPS2PI—Convert Packed Single-Precision FP Values to Packed Dword Integers

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 2D</td>
<td>CVTPS2PI mm, xmm/m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert two packed single-precision floating-point values from <code>xmm/m64</code> to two packed signed doubleword integers in <code>mm</code>.</td>
</tr>
</tbody>
</table>

Description

Converts two packed single-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an MMX technology register. When the source operand is an XMM register, the two single-precision floating-point values are contained in the low quadword of the register. When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

CVTPS2PI causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTPS2PI instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[31:0]);
DEST[63:32] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[63:32]);

Intel C/C++ Compiler Intrinsic Equivalent

CVTPS2PI __m64 _mm_cvtps_pi32(__m128 a)

SIMD Floating-Point Exceptions

Invalid, Precision.
Protected Mode Exceptions

[#GP(0)] For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

[#SS(0)] For an illegal address in the SS segment.

[#PF(fault-code)] For a page fault.

[#MF] If there is a pending x87 FPU exception.

[#NM] If CR0.TS[bit 3] = 1.


[#UD] If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.

If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE[bit 25] = 0.

If the LOCK prefix is used.

[#AC(0)] If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.

[#NM] If CR0.TS[bit 3] = 1.

[#MF] If there is a pending x87 FPU exception.


[#UD] If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.

If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE[bit 25] = 0.

If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

[#PF(fault-code)] For a page fault.

[#AC(0)] If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CVTSD2SI—Convert Scalar Double-Precision FP Value to Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compartment/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 OF 2D /r</td>
<td>CVTSD2SI r32,</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert one double-precision floating-point value from xmm/m64 to one signed doubleword integer r32.</td>
</tr>
<tr>
<td></td>
<td>xmm/m64</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F2 REX.W OF 2D /r</td>
<td>CVTSD2SI r64,</td>
<td>Valid</td>
<td>N.E.</td>
<td>Convert one double-precision floating-point value from xmm/m64 to one signed quadword integer sign-extended into r64.</td>
</tr>
<tr>
<td></td>
<td>xmm/m64</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Description**

Converts a double-precision floating-point value in the source operand (second operand) to a signed doubleword integer in the destination operand (first operand). The source operand can be an XMM register or a 64-bit memory location. The destination operand is a general-purpose register. When the source operand is an XMM register, the double-precision floating-point value is contained in the low quadword of the register.

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the instruction to 64-bit operation. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF 64-Bit Mode and OperandSize = 64
THEN
   DEST[63:0] ← Convert_Double_Precision_Floating_Point_To_Integer64(SRC[63:0]);
ELSE
   DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer32(SRC[63:0]);
FI;

**Intel C/C++ Compiler Intrinsic Equivalent**

int _mm_cvtsd_si32(__m128d a)
SIMD Floating-Point Exceptions
Invalid, Precision.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCP[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMEXCP[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
**CVTSD2SS—Convert Scalar Double-Precision FP Value to Scalar Single-Precision FP Value**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 5A /r</td>
<td>CVTSD2SS xmm1, xmm2/m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert one double-precision floating-point value in xmm2/m64 to one single-precision floating-point value in xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Converts a double-precision floating-point value in the source operand (second operand) to a single-precision floating-point value in the destination operand (first operand).

The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. When the source operand is an XMM register, the double-precision floating-point value is contained in the low quadword of the register. The result is stored in the low doubleword of the destination operand, and the upper 3 doublewords are left unchanged. When the conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[31:0] ← Convert_Double_Precision_To_Single_Precision_Floating_Point(SRC[63:0]); (* DEST[127:32] unchanged *)

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTSD2SS _mm128 _mm_cvtss(_m128 a, _m128d b)

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions**

- #GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- #SS(0) For an illegal address in the SS segment.
- #PF(fault-code) For a page fault.
- #NM If CR0.TS[bit 3] = 1.
INSTRUCTION SET REFERENCE, A-M

#XM  If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP  If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM  If CR0.TS[bit 3] = 1.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code)  For a page fault.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  For a page fault.
#NM  If CR0.TS[bit 3] = 1.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
INSTRUCTION SET REFERENCE, A-M

CVTSI2SD—Convert Dword Integer to Scalar Double-Precision FP Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 2A /r</td>
<td>CVTSI2SD xmm, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert one signed doubleword integer from r/m32 to one double-precision floating-point value in xmm.</td>
</tr>
<tr>
<td>F2 REX.W 0F 2A /r</td>
<td>CVTSI2SD xmm, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Convert one signed quadword integer from r/m64 to one double-precision floating-point value in xmm.</td>
</tr>
</tbody>
</table>

Description

Converts a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the source operand (second operand) to a double-precision floating-point value in the destination operand (first operand). The source operand can be a general-purpose register or a memory location. The destination operand is an XMM register. The result is stored in the low quadword of the destination operand, and the high quadword left unchanged.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the instruction to 64-bit operands. See the summary chart at the beginning of this section for encoding data and limits.

Operation

IF 64-Bit Mode And OperandSize = 64
THEN
DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[63:0]);
(* DEST[127:64] unchanged *)
ELSE
DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[31:0]);
(* DEST[127:64] unchanged *)
FI;

Intel C/C++ Compiler Intrinsic Equivalent
CVTSI2SD __m128d _mm_cvtsi32_sd(__m128d a, int b)

SIMD Floating-Point Exceptions
None.
Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
**CVTSI2SS—Convert Dword Integer to Scalar Single-Precision FP Value**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 2A /r</td>
<td>CVTSI2SS xmm, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert one signed doubleword integer from r/m32 to one single-precision floating-point value in xmm.</td>
</tr>
<tr>
<td>F3 REX.W 0F 2A /r</td>
<td>CVTSI2SS xmm, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Convert one signed quadword integer from r/m64 to one single-precision floating-point value in xmm.</td>
</tr>
</tbody>
</table>

**Description**

Converts a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the source operand (second operand) to a single-precision floating-point value in the destination operand (first operand). The source operand can be a general-purpose register or a memory location. The destination operand is an XMM register. The result is stored in the low doubleword of the destination operand, and the upper three doublewords are left unchanged. When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the instruction to 64-bit operands. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF 64-Bit Mode And OperandSize = 64
    THEN
        DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[63:0]);
        (* DEST[127:32] unchanged *)
    ELSE
        DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[31:0]);
        (* DEST[127:32] unchanged *)
    FI;

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTSI2SS __m128 _mm_cvtsi32_ss(__m128 a, int b)
SIMD Floating-Point Exceptions

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP  If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CVTSS2SD—Convert Scalar Single-Precision FP Value to Scalar Double-Precision FP Value

**Description**

Converts a single-precision floating-point value in the source operand (second operand) to a double-precision floating-point value in the destination operand (first operand). The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. When the source operand is an XMM register, the single-precision floating-point value is contained in the low doubleword of the register. The result is stored in the low quadword of the destination operand, and the high quadword is left unchanged.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\text{DEST}[63:0] \leftarrow \text{Convert Single Precision To Double Precision Floating Point(SRC[31:0])}; \\
(* \text{DEST}[127:64] unchanged *)
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

```
CVTSS2SD__mm128d__mm_cvtsd(__m128d a, __m128 b)
```

**SIMD Floating-Point Exceptions**

Invalid, Denormal.

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- **#SS(0)** For an illegal address in the SS segment.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

**Virtual-8086 Mode Exceptions**

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

CVTSS2SD—Convert Scalar Single-Precision FP Value to Scalar Double-Precision FP Value
### CVTSS2SD—Convert Scalar Single-Precision FP Value to Scalar Double-Precision FP Value

#### #UD

- If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0 exception and CR4.OSXMMEXCPT[bit 10] = 0.
- If CR0.EM[bit 2] = 1.
- If CR4.OSFXSR[bit 9] = 0.
- If CPUID.01H:EDX.SSE2[bit 26] = 0.
- If the LOCK prefix is used.

#### #AC(0)

- If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CVTSS2SI—Convert Scalar Single-Precision FP Value to Dword Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 2D /r</td>
<td>CVTSS2SI r32, xmm/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert one single-precision floating-point value from xmm/m32 to one signed doubleword integer in r32.</td>
</tr>
<tr>
<td>F3 REX.W 0F 2D /r</td>
<td>CVTSS2SI r64, xmm/m32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Convert one single-precision floating-point value from xmm/m32 to one signed quadword integer in r64.</td>
</tr>
</tbody>
</table>

**Description**

Converts a single-precision floating-point value in the source operand (second operand) to a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the destination operand (first operand). The source operand can be an XMM register or a memory location. The destination operand is a general-purpose register. When the source operand is an XMM register, the single-precision floating-point value is contained in the low doubleword of the register.

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the instruction to 64-bit operands. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF 64-bit Mode and OperandSize = 64 THEN

   DEST[64:0] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[31:0]);

ELSE

   DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[31:0]);

FI;

**Intel C/C++ Compiler Intrinsic Equivalent**

int _mm_cvtss_si32(__m128d a)
SIMD Floating-Point Exceptions
Invalid, Precision.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CVTTPD2DQ—Convert with Truncation Packed Double-Precision FP Values to Packed Dword Integers

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F E6</td>
<td>CVTTPD2DQ xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert two packed double-precision floating-point values from xmm2/m128 to two packed signed doubleword integers in xmm1 using truncation.</td>
</tr>
</tbody>
</table>

**Description**

Converts two packed double-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand). The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The result is stored in the low quadword of the destination operand and the high quadword is cleared to all 0s.

When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[63:0]);
DEST[63:32] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[127-64]);
DEST[127:64] ← 0000000000000000H;

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTTPD2DQ __m128i _mm_cvtpd_epi32(__m128d a)

**SIMD Floating-Point Exceptions**

Invalid, Precision.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM- MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM- MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM- MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM- MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non- canonical form.
INSTRUCTION SET REFERENCE, A-M

#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
**CVTTPD2PI—Convert with Truncation Packed Double-Precision FP Values to Packed Dword Integers**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 2C /r</td>
<td>CVTTPD2PI mm, xmm/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert two packed double-precision floating-point values from xmm/m128 to two packed signed doubleword integers in mm using truncation.</td>
</tr>
</tbody>
</table>

**Description**

Converts two packed double-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand). The source operand can be an XMM register or a 128-bit memory location. The destination operand is an MMX technology register.

When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTTPD2PI instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{Convert
double-precision floating-point to integer32,}\text{Truncate}(\text{SRC}[63:0]); \\
\text{DEST}[63:32] & \leftarrow \text{Convert
double-precision floating-point to integer32,}\text{Truncate}(\text{SRC}[127:64]);
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTT0P1PI_m64 __mm_cvttpd_pi32(__m128d a)

**SIMD Floating-Point Exceptions**

Invalid, Precision.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#MF If there is a pending x87 FPU exception.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
   If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.

#XM  If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.

#UD  If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
CVTTPS2DQ—Convert with Truncation Packed Single-Precision FP Values to Packed Dword Integers

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 5B /r</td>
<td>CVTTPS2DQ xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert four single-precision floating-point values from xmm2/m128 to four signed doubleword integers in xmm1 using truncation.</td>
</tr>
</tbody>
</table>

**Description**
Converts four packed single-precision floating-point values in the source operand (second operand) to four packed signed doubleword integers in the destination operand (first operand). The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer_Truncate(SRC[31:0]);
DEST[63:32] ← Convert_Single_Precision_Floating_Point_To_Integer_Truncate(SRC[63:32]);
DEST[95:64] ← Convert_Single_Precision_Floating_Point_To_Integer_Truncate(SRC[95:64]);
DEST[127:96] ← Convert_Single_Precision_Floating_Point_To_Integer_Truncate(SRC[127:96]);

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTTPS2DQ _m128i _mm_cvttps_epi32(_m128 a)

**SIMD Floating-Point Exceptions**
Invalid, Precision.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
  If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
  If memory operand is not aligned on a 16-byte boundary, regardless of segment.
INSTRUCTION SET REFERENCE, A-M

#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
CVTTPS2PI—Convert with Truncation Packed Single-Precision FP Values to Packed Dword Integers

Description

Converts two packed single-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand). The source operand can be an XMM register or a 64-bit memory location. The destination operand is an MMX technology register. When the source operand is an XMM register, the two single-precision floating-point values are contained in the low quadword of the register.

When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTTPS2PI instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{Convert Single-Precision Floating-Point To Integer_Truncate}(\text{SRC}[31:0]); \\
\text{DEST}[63:32] & \leftarrow \text{Convert Single-Precision Floating-Point To Integer_Truncate}(\text{SRC}[63:32]);
\end{align*}
\]

Intel C/C++ Compiler Intrinsic Equivalent

`CVTTPS2PI _m64 _mm_cvttps_pi32(__m128 a)`

SIMD Floating-Point Exceptions

Invalid, Precision.
Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#MF If there is a pending x87 FPU exception.

#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.

If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE[bit 25] = 0.

If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.

If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE[bit 25] = 0.

If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CVTTSD2SI—Convert with Truncation Scalar Double-Precision FP Value to Signed Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 2C /r</td>
<td>CVTTSD2SI r32, xmm/m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert one double-precision floating-point value from xmm/m64 to one signed doubleword integer in r32 using truncation.</td>
</tr>
<tr>
<td>F2 REX.W 0F 2C /r</td>
<td>CVTTSD2SI r64, xmm/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Convert one double precision floating-point value from xmm/m64 to one signed quadword integer in r64 using truncation.</td>
</tr>
</tbody>
</table>

**Description**

Converts a double-precision floating-point value in the source operand (second operand) to a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the destination operand (first operand). The source operand can be an XMM register or a 64-bit memory location. The destination operand is a general-purpose register. When the source operand is an XMM register, the double-precision floating-point value is contained in the low quadword of the register.

When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised. If this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the instruction to 64-bit operation. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF 64-Bit Mode and OperandSize = 64  
THEN  
    DEST[63:0] ← Convert_Double_Precision_Floating_Point_To_Integer64_Truncate(SRC[63:0]);  
ELSE  
    DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer32_Truncate(SRC[63:0]);  
FI;
Intel C/C++ Compiler Intrinsic Equivalent

\[
\text{int } _mm\_cvttssd\_si32(__m128d a)
\]

**SIMD Floating-Point Exceptions**

Invalid, Precision.

**Protected Mode Exceptions**

- **#GP(0)**: For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- **#SS(0)**: For an illegal address in the SS segment.
- **#PF(fault-code)**: For a page fault.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- **GP**: If any part of the operand lies outside the effective address space from 0 to FFFFH.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Virtual-8086 Mode Exceptions**

Same exceptions as in real address mode.

- **#PF(fault-code)**: For a page fault.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  For a page fault.
#NM  If CR0.TS[bit 3] = 1.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CVTTSS2SI—Convert with Truncation Scalar Single-Precision FP Value to Dword Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 2C /r</td>
<td>CVTTSS2SI r32, xmm/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert one single-precision floating-point value from xmm/m32 to one signed doubleword integer in r32 using truncation.</td>
</tr>
<tr>
<td>F3 REX.W 0F 2C /r</td>
<td>CVTTSS2SI r64, xmm/m32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Convert one single-precision floating-point value from xmm/m32 to one signed quadword integer in r64 using truncation.</td>
</tr>
</tbody>
</table>

**Description**

Converts a single-precision floating-point value in the source operand (second operand) to a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the destination operand (first operand). The source operand can be an XMM register or a 32-bit memory location. The destination operand is a general-purpose register. When the source operand is an XMM register, the single-precision floating-point value is contained in the low doubleword of the register.

When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised. If this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the instruction to 64-bit operation. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF 64-Bit Mode and OperandSize = 64
THEN
  DEST[63:0] ← Convert_Single_Precision_Floating_Point_To_Integer_Truncate(SRC[31:0]);
ELSE
  DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer_Truncate(SRC[31:0]);
FI;
INSTRUCTION SET REFERENCE, A-M

Intel C/C++ Compiler Intrinsic Equivalent
int _mm_cvttss_si32(__m128d a)

SIMD Floating-Point Exceptions
Invalid, Precision.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.

#UD If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.

If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE[bit 25] = 0.

If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CWD/CDQ/CQO—Convert Word to Doubleword/Convert Doubleword to Quadword

Description
Doubles the size of the operand in register AX, EAX, or RAX (depending on the operand size) by means of sign extension and stores the result in registers DX:AX, EDX:EAX, or RDX:RAX, respectively. The CWD instruction copies the sign (bit 15) of the value in the AX register into every bit position in the DX register. The CDQ instruction copies the sign (bit 31) of the value in the EAX register into every bit position in the EDX register. The CQO instruction (available in 64-bit mode only) copies the sign (bit 63) of the value in the RAX register into every bit position in the RDX register.

The CWD instruction can be used to produce a doubleword dividend from a word before word division. The CDQ instruction can be used to produce a quadword dividend from a doubleword before doubleword division. The CQO instruction can be used to produce a double quadword dividend from a quadword before a quadword division.

The CWD and CDQ mnemonics reference the same opcode. The CWD instruction is intended for use when the operand-size attribute is 16 and the CDQ instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when CWD is used and to 32 when CDQ is used. Others may treat these mnemonics as synonyms (CWD/CDQ) and use the current setting of the operand-size attribute to determine the size of values to be converted, regardless of the mnemonic used.

In 64-bit mode, use of the REX.W prefix promotes operation to 64 bits. The CQO mnemonics reference the same opcode as CWD/CDQ. See the summary chart at the beginning of this section for encoding data and limits.

Operation
IF OperandSize = 16 (* CWD instruction *)
THEN
  DX ← SignExtend(AX);
ELSE IF OperandSize = 32 (* CDQ instruction *)
  EDX ← SignExtend(EAX);
ELSE IF 64-Bit Mode and OperandSize = 64 (* CQO instruction*)

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>99</td>
<td>CWD</td>
<td>Valid</td>
<td>Valid</td>
<td>DX:AX ← sign-extend of AX.</td>
</tr>
<tr>
<td>99</td>
<td>CDQ</td>
<td>Valid</td>
<td>Valid</td>
<td>EDX:EAX ← sign-extend of EAX.</td>
</tr>
<tr>
<td>REX.W + 99</td>
<td>CQO</td>
<td>Valid</td>
<td>N.E.</td>
<td>RDX:RAX← sign-extend of RAX.</td>
</tr>
</tbody>
</table>
RDX ← SignExtend(RAX); Fl;
Fl;

Flags Affected
None.

Exceptions (All Operating Modes)
#UD If the LOCK prefix is used.
DAA—Decimal Adjust AL after Addition

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>27</td>
<td>DAA</td>
<td>Invalid</td>
<td>Valid</td>
<td>Decimal adjust AL after addition.</td>
</tr>
</tbody>
</table>

Description

Adjusts the sum of two packed BCD values to create a packed BCD result. The AL register is the implied source and destination operand. The DAA instruction is only useful when it follows an ADD instruction that adds (binary addition) two 2-digit, packed BCD values and stores a byte result in the AL register. The DAA instruction then adjusts the contents of the AL register to contain the correct 2-digit, packed BCD result. If a decimal carry is detected, the CF and AF flags are set accordingly.

This instruction executes as described above in compatibility mode and legacy mode. It is not valid in 64-bit mode.

Operation

IF 64-Bit Mode
THEN
   #UD;
ELSE
   old_AL ← AL;
   old_CF ← CF;
   CF ← 0;
   IF (((AL AND 0FH) > 9) or AF = 1)
   THEN
      AL ← AL + 6;
      CF ← old_CF or (Carry from AL ← AL + 6);
      AF ← 1;
   ELSE
      AF ← 0;
   FI;
   IF ((old_AL > 99H) or (old_CF = 1))
   THEN
      AL ← AL + 60H;
      CF ← 1;
   ELSE
      CF ← 0;
   FI;
FI;
DAA—Decimal Adjust AL after Addition

**Example**

ADD AL, BL  
Before: AL=79H  BL=35H  EFLAGS(OSZAPC)=XXXXXX  
After: AL=AEH  BL=35H  EFLAGS(OSZAPC)=110000

DAA  
Before: AL=AEH  BL=35H  EFLAGS(OSZAPC)=110000  
After: AL=14H  BL=35H  EFLAGS(OSZAPC)=X00111

DAA  
Before: AL=2EH  BL=35H  EFLAGS(OSZAPC)=110000  
After: AL=34H  BL=35H  EFLAGS(OSZAPC)=X00101

**Flags Affected**

The CF and AF flags are set if the adjustment of the value results in a decimal carry in either digit of the result (see the "Operation" section above). The SF, ZF, and PF flags are set according to the result. The OF flag is undefined.

**Protected Mode Exceptions**

#UD  
If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#UD  
If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#UD  
If the LOCK prefix is used.

**Compatibility Mode Exceptions**

#UD  
If the LOCK prefix is used.

**64-Bit Mode Exceptions**

#UD  
If in 64-bit mode.
### DAS—Decimal Adjust AL after Subtraction

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compag/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2F</td>
<td>DAS</td>
<td>Invalid</td>
<td>Valid</td>
<td>Decimal adjust AL after subtraction.</td>
</tr>
</tbody>
</table>

#### Description

Adjusts the result of the subtraction of two packed BCD values to create a packed BCD result. The AL register is the implied source and destination operand. The DAS instruction is only useful when it follows a SUB instruction that subtracts (binary subtraction) one 2-digit, packed BCD value from another and stores a byte result in the AL register. The DAS instruction then adjusts the contents of the AL register to contain the correct 2-digit, packed BCD result. If a decimal borrow is detected, the CF and AF flags are set accordingly.

This instruction executes as described above in compatibility mode and legacy mode. It is not valid in 64-bit mode.

#### Operation

IF 64-Bit Mode

THEN

#UD;

ELSE

old_AL ← AL;
old_CF ← CF;
CF ← 0;
IF (((AL AND 0FH) > 9) or AF = 1)
THEN

AL ← AL - 6;
CF ← old_CF or (Borrow from AL ← AL - 6);
AF ← 1;
ELSE

AF ← 0;
FI;

IF ((old_AL > 99H) or (old_CF = 1))
THEN

AL ← AL - 60H;
CF ← 1;
FI;

FI;
### Example

**DAS—Decimal Adjust AL after Subtraction**

#### SUB AL, BL

**Before:** AL = 35H, BL = 47H, EFLAGS(OSZAPC) = XXXXXX

**After:** AL = EEH, BL = 47H, EFLAGS(OSZAPC) = 010111

#### DAA

**Before:** AL = EEH, BL = 47H, EFLAGS(OSZAPC) = 010111

**After:** AL = 88H, BL = 47H, EFLAGS(OSZAPC) = X10111

### Flags Affected

The CF and AF flags are set if the adjustment of the value results in a decimal borrow in either digit of the result (see the “Operation” section above). The SF, ZF, and PF flags are set according to the result. The OF flag is undefined.

### Protected Mode Exceptions

#UD If the LOCK prefix is used.

### Real-Address Mode Exceptions

#UD If the LOCK prefix is used.

### Virtual-8086 Mode Exceptions

#UD If the LOCK prefix is used.

### Compatibility Mode Exceptions

#UD If the LOCK prefix is used.

### 64-Bit Mode Exceptions

#UD If in 64-bit mode.
INSTRUCTION SET REFERENCE, A-M

DEC—Decrement by 1

**Description**

Subtracts 1 from the destination operand, while preserving the state of the CF flag. The destination operand can be a register or a memory location. This instruction allows a loop counter to be updated without disturbing the CF flag. (To perform a decrement operation that updates the CF flag, use a SUB instruction with an immediate operand of 1.)

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, DEC r16 and DEC r32 are not encodable (because opcodes 48H through 4FH are REX prefixes). Otherwise, the instruction’s 64-bit mode default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits.

See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

DEST ← DEST - 1;

**Flags Affected**

The CF flag is not affected. The OF, SF, ZF, AF, and PF flags are set according to the result.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE /1</td>
<td>DEC r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement r/m8 by 1.</td>
</tr>
<tr>
<td>REX + FE /1</td>
<td>DEC r/m8'</td>
<td>Valid</td>
<td>N.E.</td>
<td>Decrement r/m8 by 1.</td>
</tr>
<tr>
<td>FF /1</td>
<td>DEC r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement r/m16 by 1.</td>
</tr>
<tr>
<td>FF /1</td>
<td>DEC r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement r/m32 by 1.</td>
</tr>
<tr>
<td>REX.W + FF /1</td>
<td>DEC r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Decrement r/m64 by 1.</td>
</tr>
<tr>
<td>48+rw</td>
<td>DEC r16</td>
<td>N.E.</td>
<td>Valid</td>
<td>Decrement r16 by 1.</td>
</tr>
<tr>
<td>48+rd</td>
<td>DEC r32</td>
<td>N.E.</td>
<td>Valid</td>
<td>Decrement r32 by 1.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
Protected Mode Exceptions

#GP(0)  If the destination operand is located in a non-writable segment.
         If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
         If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#UD  If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

#UD  If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.

#PF(fault-code)  If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
## DIV—Unsigned Divide

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /6</td>
<td>DIV r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned divide AX by r/m8, with result stored in AL ← Quotient, AH ← Remainder.</td>
</tr>
<tr>
<td>REX + F6 /6</td>
<td>DIV r/m8*</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide AX by r/m8, with result stored in AL ← Quotient, AH ← Remainder.</td>
</tr>
<tr>
<td>F7 /6</td>
<td>DIV r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned divide DX:AX by r/m16, with result stored in AX ← Quotient, DX ← Remainder.</td>
</tr>
<tr>
<td>F7 /6</td>
<td>DIV r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned divide EDX:EAX by r/m32, with result stored in EAX ← Quotient, EDX ← Remainder.</td>
</tr>
<tr>
<td>REX.W + F7 /6</td>
<td>DIV r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide RDX:RAX by r/m64, with result stored in RAX ← Quotient, RDX ← Remainder.</td>
</tr>
</tbody>
</table>

### Notes:
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

### Description
Divides unsigned the value in the AX, DX:AX, EDX:EAX, or RDX:RAX registers (dividend) by the source operand (divisor) and stores the result in the AX (AH:AL), DX:AX, EDX:EAX, or RDX:RAX registers. The source operand can be a general-purpose register or a memory location. The action of this instruction depends on the operand size (dividend/divisor). Division using 64-bit operand is available only in 64-bit mode.

Non-integral results are truncated (chopped) towards 0. The remainder is always less than the divisor in magnitude. Overflow is indicated with the #DE (divide error) exception rather than with the CF flag.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. In 64-bit mode when REX.W is applied, the instruction divides the unsigned value in RDX:RAX by the source operand and stores the quotient in RAX, the remainder in RDX.

See the summary chart at the beginning of this section for encoding data and limits. See Table 3-28.
DIV—Unsigned Divide

Table 3-28. DIV Action

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Dividend</th>
<th>Divisor</th>
<th>Quotient</th>
<th>Remainder</th>
<th>Maximum Quotient</th>
</tr>
</thead>
<tbody>
<tr>
<td>Word/byte</td>
<td>AX</td>
<td>r/m8</td>
<td>AL</td>
<td>AH</td>
<td>255</td>
</tr>
<tr>
<td>Doubleword/word</td>
<td>DX:AX</td>
<td>r/m16</td>
<td>AX</td>
<td>DX</td>
<td>65,535</td>
</tr>
<tr>
<td>Quadword/doubleword</td>
<td>EDX:EAX</td>
<td>r/m32</td>
<td>EAX</td>
<td>EDX</td>
<td>$2^{32} - 1$</td>
</tr>
<tr>
<td>Doublequadword/quadword</td>
<td>RDX:RAX</td>
<td>r/m64</td>
<td>RAX</td>
<td>RDX</td>
<td>$2^{64} - 1$</td>
</tr>
</tbody>
</table>

Operation

IF SRC = 0
THEN #DE; Fl; (* Divide Error *)
IF OperandSize = 8 (* Word/Byte Operation *)
THEN
  temp ← AX / SRC;
  IF temp > FFH
    THEN #DE; (* Divide error *)
    ELSE
      AL ← temp;
      AH ← AX MOD SRC;
    FI;
ELSE IF OperandSize = 16 (* Doubleword/word operation *)
THEN
  temp ← DX:AX / SRC;
  IF temp > FFFFH
    THEN #DE; (* Divide error *)
    ELSE
      AX ← temp;
      DX ← DX:AX MOD SRC;
    FI;
ELSE IF OperandSize = 32 (* Quadword/doubleword operation *)
THEN
  temp ← EDX:EAX / SRC;
  IF temp > FFFFFFFFH
    THEN #DE; (* Divide error *)
    ELSE
      EAX ← temp;
      EDX ← EDX:EAX MOD SRC;
    FI;
FI;

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ELSE IF 64-Bit Mode and Operandsize = 64 (* Doublequadword/quadword operation *)
   THEN
     temp ← RDX:RAX / SRC;
     IF temp > FFFFFFFF00000000H
       THEN #DE; (* Divide error *)
     ELSE
       RAX ← temp;
       RDX ← RDX:RAX MOD SRC;
     FI;
   FI;
FI;

Flags Affected
The CF, OF, SF, ZF, AF, and PF flags are undefined.

Protected Mode Exceptions
#DE  If the source operand (divisor) is 0
     If the quotient is too large for the designated register.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
     If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions
#DE  If the source operand (divisor) is 0.
     If the quotient is too large for the designated register.
#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
     If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD  If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#DE If the source operand (divisor) is 0.
If the quotient is too large for the designated register.

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#DE If the source operand (divisor) is 0
If the quotient is too large for the designated register.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
DIVPD—Divide Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 5E /r</td>
<td>DIVPD xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide packed double-precision floating-point values in xmm1 by packed double-precision floating-point values xmm2/m128.</td>
</tr>
</tbody>
</table>

Description
Performs a SIMD divide of the two packed double-precision floating-point values in the destination operand (first operand) by the two packed double-precision floating-point values in the source operand (second operand), and stores the packed double-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Chapter 11 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an overview of a SIMD double-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST[63:0] ← DEST[63:0] / SRC[63:0];
DEST[127:64] ← DEST[127:64] / SRC[127:64];

Intel C/C++ Compiler Intrinsic Equivalent
DIVPD __m128d _mm_div_pd(__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Divide-by-Zero, Precision, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
    If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
INSTRUCTION SET REFERENCE, A-M

#XM     If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD     If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
         If CR0.EM[bit 2] = 1.
         If CR4.OSFXSR[bit 9] = 0.
         If CPUID.01H:EDX.SSE2[bit 26] = 0.
         If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP  If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
         If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM  If CR0.TS[bit 3] = 1.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
         If CR0.EM[bit 2] = 1.
         If CR4.OSFXSR[bit 9] = 0.
         If CPUID.01H:EDX.SSE2[bit 26] = 0.
         If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)   If the memory address is in a non-canonical form.
         If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM     If CR0.TS[bit 3] = 1.
DIVPD—Divide Packed Double-Precision Floating-Point Values

INSTRUCTION SET REFERENCE, A-M

#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
DIVPS—Divide Packed Single-Precision Floating-Point Values

Description
Performs a SIMD divide of the four packed single-precision floating-point values in the destination operand (first operand) by the four packed single-precision floating-point values in the source operand (second operand), and stores the packed single-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an overview of a SIMD single-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST[31:0] ← DEST[31:0] / SRC[31:0];
DEST[95:64] ← DEST[95:64] / SRC[95:64];

Intel C/C++ Compiler Intrinsic Equivalent
DIVPS __m128 _mm_div_ps(__m128 a, __m128 b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Divide-by-Zero, Precision, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
INSTRUCTION SET REFERENCE, A-M

DIVPS—Divide Packed Single-Precision Floating-Point Values

#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE[bit 25] = 0.
    If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
    If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE[bit 25] = 0.
    If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
    If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
DIVSD—Divide Scalar Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 5E /r</td>
<td>DIVSD xmm1, xmm2/m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide low double-precision floating-point value in xmm1 by low double-precision floating-point value in xmm2/mem64.</td>
</tr>
</tbody>
</table>

**Description**
Divides the low double-precision floating-point value in the destination operand (first operand) by the low double-precision floating-point value in the source operand (second operand), and stores the double-precision floating-point result in the destination operand. The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. The high quadword of the destination operand remains unchanged. See Chapter 11 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an overview of a scalar double-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**
DEST[63:0] ← DEST[63:0] / SRC[63:0];
(* DEST[127:64] unchanged *)

**Intel C/C++ Compiler Intrinsic Equivalent**
DIVSD __m128d _mm_div_sd (m128d a, m128d b)

**SIMD Floating-Point Exceptions**
Overflow, Underflow, Invalid, Divide-by-Zero, Precision, Denormal.

**Protected Mode Exceptions**
- #GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- #SS(0) For an illegal address in the SS segment.
- #PF(fault-code) For a page fault.
- #NM If CR0.TS[bit 3] = 1.
- #UD If an unmasked SIMD floating-point exception and CR4.OSXMEXCEPT[bit 10] = 0.
INSTRUCTION SET REFERENCE, A-M

If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
DIVSD—Divide Scalar Double-Precision Floating-Point Values

INSTRUCTION SET REFERENCE, A-M

If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
DIVSS—Divide Scalar Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 5E /r</td>
<td>DIVSS xmm1, xmm2/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide low single-precision floating-point value in xmm1 by low single-precision floating-point value in xmm2/m32.</td>
</tr>
</tbody>
</table>

**Description**

Divides the low single-precision floating-point value in the destination operand (first operand) by the low single-precision floating-point value in the source operand (second operand), and stores the single-precision floating-point result in the destination operand. The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. The three high-order doublewords of the destination operand remain unchanged. See Chapter 10 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an overview of a scalar single-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[ \text{DEST}[31:0] \leftarrow \text{DEST}[31:0] / \text{SRC}[31:0]; \]

(* DEST[127:32] unchanged *)

**Intel C/C++ Compiler Intrinsic Equivalent**

```
DIVSS __m128 _mm_div_ss(__m128 a, __m128 b)
```

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Divide-by-Zero, Precision, Denormal.

**Protected Mode Exceptions**

- #GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- #SS(0) For an illegal address in the SS segment.
- #PF(fault-code) For a page fault.
- #NM If CR0.TS[bit 3] = 1.
- #UD If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
DIVSS—Divide Scalar Single-Precision Floating-Point Values

If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
INSTRUCTION SET REFERENCE, A-M

If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
DPPD — Dot Product of Packed Double Precision Floating-Point Values

**Opcode** | **Instruction** | **64-bit Mode** | **Compat/Leg Mode** | **Description**
---|---|---|---|---
66 0F 3A 41 /r ib | DPPD xmm1, xmm2/m128, imm8 | Valid | Valid | Selectively multiply packed DP floating-point values from xmm1 with packed DP floating-point values from xmm2, add and selectively store the packed DP floating-point values to xmm1.

**Description**

Conditionally multiplies the packed double-precision floating-point values in the destination operand (first operand) with the packed double-precision floating-point values in the source (second operand) depending on a mask extracted from bits [5:4] of the immediate operand (third operand). If a condition mask bit is zero, the corresponding multiplication is replaced by a value of 0.0.

The two resulting double-precision values are summed into an intermediate result. The intermediate result is conditionally broadcasted to the destination using a broadcast mask specified by bits [1:0] of the immediate byte.

If a broadcast mask bit is "1", the intermediate result is copied to the corresponding qword element in the destination operand. If a broadcast mask bit is zero, the corresponding element in the destination is set to zero.

DPPS follows the NaN forwarding rules stated in the Software Developer’s Manual, vol. 1, table 4.7. These rules do not cover horizontal prioritization of NaNs. Horizontal propagation of NaNs to the destination and the positioning of those NaNs in the destination is implementation dependent. NaNs on the input sources or computationally generated NaNs will have at least one NaN propagated to the destination.

**Operation**

\[
\begin{align*}
\text{IF} (\text{imm8}[4] = 1) & \quad \text{THEN} \ \text{Temp1}[63:0] \leftarrow \text{DEST}[63:0] \times \text{SRC}[63:0]; \\
\text{ELSE} \ \text{Temp1}[63:0] & \leftarrow +0.0; \ Ft; \\
\text{IF} (\text{imm8}[5] = 1) & \quad \text{THEN} \ \text{Temp1}[127:64] \leftarrow \text{DEST}[127:64] \times \text{SRC}[127:64]; \\
\text{ELSE} \ \text{Temp1}[127:64] & \leftarrow +0.0; \ Ft; \\
\text{Temp2}[63:0] & \leftarrow \text{Temp1}[63:0] + \text{Temp1}[127:64]; \\
\text{IF} (\text{imm8}[0] = 1) & \quad \text{THEN} \ \text{DEST}[63:0] \leftarrow \text{Temp2}[63:0];
\end{align*}
\]
ELSE DEST[63:0] ← +0.0; Fl;
IF (imm8[1] = 1)
    THEN DEST[127:64] ← Temp2[63:0];
ELSE DEST[127:64] ← +0.0; Fl;

Flags Affected
None

Intel C/C++ Compiler Intrinsic Equivalent
DPPD __m128d _mm_dp_pd (__m128d a, __m128d b, const int mask);

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal
Exceptions are determined separately for each add and multiply operation.
Unmasked exceptions will leave the destination untouched.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
    If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If an unmasked SIMD floating-point exception and OSXM-MEXCPT in CR4 is 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
    If LOCK prefix is used.
    Either the prefix REP (F3h) or REPN (F2H) is used.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

Real Mode Exceptions
#GP(0) if any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
    If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#NM  If CR0.TS[bit 3] = 1.
#UD  If an unmasked SIMD floating-point exception and OSXM-MEXCPT in CR4 is 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
   If LOCK prefix is used.
   Either the prefix REP (F3h) or REPN (F2H) is used.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

Virtual 8086 Mode Exceptions
Same exceptions as in Real Address Mode.
#PF(fault-code)  For a page fault.

Compatibility Mode Exceptions
Same exceptions as in Protected Mode.

64-Bit Mode Exceptions
#GP(0)  If the memory address is in a non-canonical form.
   If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#PF(fault-code)  For a page fault.
#NM  If TS in CR0 is set.
#UD  If an unmasked SIMD floating-point exception and OSXM-MEXCPT in CR4 is 0.
   If EM in CR0 is set.
   If OSFXSR in CR4 is 0.
   If CPUID feature flag ECX.SSE4_1 is 0.
   If LOCK prefix is used.
   Either the prefix REP (F3h) or REPN (F2H) is used.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
DPPS — Dot Product of Packed Single Precision Floating-Point Values

**Description**

Conditionally multiplies the packed single precision floating-point values in the destination operand (first operand) with the packed single-precision floats in the source (second operand) depending on a mask extracted from the high 4 bits of the immediate byte (third operand). If a condition mask bit in Imm8[7:4] is zero, the corresponding multiplication is replaced by a value of 0.0.

The four resulting single-precision values are summed into an intermediate result. The intermediate result is conditionally broadcasted to the destination using a broadcast mask specified by bits [3:0] of the immediate byte.

If a broadcast mask bit is "1", the intermediate result is copied to the corresponding dword element in the destination operand. If a broadcast mask bit is zero, the corresponding element in the destination is set to zero.

DPPS follows the NaN forwarding rules stated in the Software Developer’s Manual, vol. 1, table 4.7. These rules do not cover horizontal prioritization of NaNs. Horizontal propagation of NaNs to the destination and the positioning of those NaNs in the destination is implementation dependent. NaNs on the input sources or computationally generated NaNs will have at least one NaN propagated to the destination.

**Operation**

\[
\begin{align*}
&\text{IF (imm8}[4] == 1) \\
&\quad \text{THEN Temp1}[31:0] \leftarrow \text{DEST}[31:0] \times \text{SRC}[31:0]; \\
&\quad \text{ELSE Temp1}[31:0] \leftarrow +0.0; \text{Fl;} \\
&\text{IF (imm8}[5] == 1) \\
&\quad \text{THEN Temp1}[63:32] \leftarrow \text{DEST}[63:32] \times \text{SRC}[63:32]; \\
&\quad \text{ELSE Temp1}[63:32] \leftarrow +0.0; \text{Fl;} \\
&\text{IF (imm8}[6] == 1) \\
&\quad \text{THEN Temp1}[95:64] \leftarrow \text{DEST}[95:64] \times \text{SRC}[95:64]; \\
&\quad \text{ELSE Temp1}[95:64] \leftarrow +0.0; \text{Fl;} \\
&\text{IF (imm8}[7] == 1) \\
&\quad \text{THEN Temp1}[127:96] \leftarrow \text{DEST}[127:96] \times \text{SRC}[127:96];
\end{align*}
\]

**Opcode Instruction 64-bit**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66H OF 3A 40H</td>
<td>DPPS xmm1, xmm2/m128, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Selectively multiply packed SP floating-point values from xmm1 with packed SP floating-point values from xmm2, add and selectively store the packed SP floating-point values or zero values to xmm1.</td>
</tr>
</tbody>
</table>
ELSE Temp1[127:96] ← +0.0; Fl;
Temp2[31:0] ← Temp1[31:0] + Temp1[63:32];
Temp3[31:0] ← Temp1[95:64] + Temp1[127:96];
Temp4[31:0] ← Temp2[31:0] + Temp3[31:0];

IF (imm8[0] == 1)
    THEN DEST[31:0] ← Temp4[31:0];
    ELSE DEST[31:0] ← +0.0; Fl;
IF (imm8[1] == 1)
    THEN DEST[63:32] ← Temp4[31:0];
    ELSE DEST[63:32] ← +0.0; Fl;
IF (imm8[2] == 1)
    THEN DEST[95:64] ← Temp4[31:0];
    ELSE DEST[95:64] ← +0.0; Fl;
IF (imm8[3] == 1)
    THEN DEST[127:96] ← Temp4[31:0];
    ELSE DEST[127:96] ← +0.0; Fl;

Intel C/C++ Compiler Intrinsic Equivalent
DPPS __m128 _mm_dp_ps (__m128 a, __m128 b, const int mask);

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal
Exceptions are determined separately for each add and multiply operation, in the
order of their execution. Unmasked exceptions will leave the destination operands
unchanged.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS,
ES, FS, or GS segments.
    If a memory operand is not aligned on a 16-byte boundary,
    regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If an unmasked SIMD floating-point exception and OSXM-
    MEXCPT in CR4 is 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

Real Mode Exceptions

#GP(0) if any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM If CR0.TS[bit 3] = 1.

#UD If an unmasked SIMD floating-point exception and OSXM-MEXCPT in CR4 is 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

Virtual 8086 Mode Exceptions

Same exceptions as in Real Address Mode.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in Protected Mode.

64-Bit Mode Exceptions

#GP(0) If the memory address is in a non-canonical form.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#PF(fault-code) For a page fault.

#NM If TS in CR0 is set.

#UD If an unmasked SIMD floating-point exception and OSXM-MEXCPT in CR4 is 0.
If EM in CR0 is set.
If OSFXSR in CR4 is 0.
If CPUID feature flag ECX.SSE4_1 is 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

#XM
**EMMS—Empty MMX Technology State**

**Description**

Sets the values of all the tags in the x87 FPU tag word to empty (all 1s). This operation marks the x87 FPU data registers (which are aliased to the MMX technology registers) as available for use by x87 FPU floating-point instructions. (See Figure 8-7 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for the format of the x87 FPU tag word.) All other MMX instructions (other than the EMMS instruction) set all the tags in x87 FPU tag word to valid (all 0s).

The EMMS instruction must be used to clear the MMX technology state at the end of all MMX technology procedures or subroutines and before calling other procedures or subroutines that may execute x87 floating-point instructions. If a floating-point instruction loads one of the registers in the x87 FPU data register stack before the x87 FPU tag word has been reset by the EMMS instruction, an x87 floating-point register stack overflow can occur that will result in an x87 floating-point exception or incorrect result.

EMMS operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[ \text{x87FPUTagWord} \leftarrow \text{FFFFH}; \]

**Intel C/C++ Compiler Intrinsic Equivalent**

`void _mm_empty()`

**Flags Affected**

None.

**Protected Mode Exceptions**

- #UD If CR0.EM[bit 2] = 1.
- #NM If CR0.TS[bit 3] = 1.
- #MF If there is a pending FPU exception.
- #UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.
Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
ENTER—Make Stack Frame for Procedure Parameters

Description

Creates a stack frame for a procedure. The first operand (size operand) specifies the size of the stack frame (that is, the number of bytes of dynamic storage allocated on the stack for the procedure). The second operand (nesting level operand) gives the lexical nesting level (0 to 31) of the procedure. The nesting level determines the number of stack frame pointers that are copied into the “display area” of the new stack frame from the preceding frame. Both of these operands are immediate values.

The stack-size attribute determines whether the BP (16 bits), EBP (32 bits), or RBP (64 bits) register specifies the current frame pointer and whether SP (16 bits), ESP (32 bits), or RSP (64 bits) specifies the stack pointer. In 64-bit mode, stack-size attribute is always 64-bits.

The ENTER and companion LEAVE instructions are provided to support block structured languages. The ENTER instruction (when used) is typically the first instruction in a procedure and is used to set up a new stack frame for a procedure. The LEAVE instruction is then used at the end of the procedure (just before the RET instruction) to release the stack frame.

If the nesting level is 0, the processor pushes the frame pointer from the BP/EBP/RBP register onto the stack, copies the current stack pointer from the SP/ESP/RSP register into the BP/EBP/RBP register, and loads the SP/ESP/RSP register with the current stack-pointer value minus the value in the size operand. For nesting levels of 1 or greater, the processor pushes additional frame pointers on the stack before adjusting the stack pointer. These additional frame pointers provide the called procedure with access points to other nested frames on the stack. See “Procedure Calls for Block-Structured Languages” in Chapter 6 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information about the actions of the ENTER instruction.

The ENTER instruction causes a page fault whenever a write using the final value of the stack pointer (within the current stack segment) would do so.

In 64-bit mode, default operation size is 64 bits; 32-bit operation size cannot be encoded.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C8 iw 00</td>
<td>ENTER imm16, 0</td>
<td>Valid</td>
<td>Valid</td>
<td>Create a stack frame for a procedure.</td>
</tr>
<tr>
<td>C8 iw 01</td>
<td>ENTER imm16,1</td>
<td>Valid</td>
<td>Valid</td>
<td>Create a nested stack frame for a procedure.</td>
</tr>
<tr>
<td>C8 iw lb</td>
<td>ENTER imm16, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Create a nested stack frame for a procedure.</td>
</tr>
</tbody>
</table>
Operation

NestingLevel ← NestingLevel MOD 32
IF 64-Bit Mode (StackSize = 64)
THEN
  Push(RBP);
  FrameTemp ← RSP;
ELSE IF StackSize = 32
THEN
  Push(EBP);
  FrameTemp ← ESP; Fl;
ELSE (* StackSize = 16 *)
  Push(BP);
  FrameTemp ← SP;
FI;
IF NestingLevel = 0
THEN GOTO CONTINUE;
FI;
IF (NestingLevel > 1)
THEN FOR i ← 1 to (NestingLevel - 1)
  DO
    IF 64-Bit Mode (StackSize = 64)
    THEN
      RBP ← RBP - 8;
      Push([RBP]); (* Quadword push *)
    ELSE IF OperandSize = 32
    THEN
      IF StackSize = 32
      THEN
        EBP ← EBP - 4;
        Push([EBP]); (* Doubleword push *)
      ELSE (* StackSize = 16 *)
      THEN
        BP ← BP - 4;
        Push([BP]); (* Doubleword push *)
      FI;
    ELSE (* OperandSize = 16 *)
    ELSE (* OperandSize = 16 *)
    IF StackSize = 32
    THEN
      EBP ← EBP - 2;
      Push([EBP]); (* Word push *)
    ELSE (* StackSize = 16 *)
    THEN
      BP ← BP - 2;
      Push([BP]); (* Word push *)
    FI;
  FI;
CONTINUE;

ENTER—Make Stack Frame for Procedure Parameters
**ENTER—Make Stack Frame for Procedure Parameters**

```
FI;
FI;
OD;
FI;

IF 64-Bit Mode (StackSize = 64)
  THEN
    Push(FrameTemp); (* Quadword push *)
  ELSE IF OperandSize = 32
    THEN
      Push(FrameTemp); FI; (* Doubleword push *)
  ELSE (* OperandSize = 16 *)
    Push(FrameTemp); (* Word push *)
FI;

CONTINUE:
IF 64-Bit Mode (StackSize = 64)
  THEN
    RBP ← FrameTemp;
    RSP ← RSP − Size;
  ELSE IF StackSize = 32
    THEN
      EBP ← FrameTemp;
      ESP ← ESP − Size; FI;
  ELSE (* StackSize = 16 *)
    BP ← FrameTemp;
    SP ← SP − Size;
FI;
END;

**Flags Affected**
None.

**Protected Mode Exceptions**

- #SS(0) If the new value of the SP or ESP register is outside the stack segment limit.
- #PF(fault-code) If a page fault occurs or if a write using the final value of the stack pointer (within the current stack segment) would cause a page fault.
- #UD If the LOCK prefix is used.

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ENTER—Make Stack Frame for Procedure Parameters

**Real-Address Mode Exceptions**

- **#SS** If the new value of the SP or ESP register is outside the stack segment limit.
- **#UD** If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

- **#SS(0)** If the new value of the SP or ESP register is outside the stack segment limit.
- **#PF(fault-code)** If a page fault occurs or if a write using the final value of the stack pointer (within the current stack segment) would cause a page fault.
- **#UD** If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

- **#SS(0)** If the stack address is in a non-canonical form.
- **#PF(fault-code)** If a page fault occurs or if a write using the final value of the stack pointer (within the current stack segment) would cause a page fault.
- **#UD** If the LOCK prefix is used.
EXTRACTPS — Extract Packed Single Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 OF 3A 17</td>
<td>EXTRACTPS reg/m32, xmm2, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Extract a single-precision floating-point value from xmm2 at the source offset specified by imm8 and store the result to reg or m32. The upper 32 bits of r64 is zeroed if reg is r64.</td>
</tr>
</tbody>
</table>

Description

Extract a single-precision floating-point value from the source xmm register (second argument) at an offset determined by imm8[1-0]*32. The extracted single precision floating-point value is stored into the low 32-bits of the destination register or to the 32-bit memory location.

When in 64-bit mode and the destination operand is a general purpose register (GPR), the default operand size is 64 bits. The upper 32 bits of the 64-bit register is filled with zero.

Operation

IF (64-Bit Mode and the destination is a GPR )
THEN
    DEST[31:0] ← (SRC >> (32 * imm8[1:0])) AND 0FFFFFFFh;
    DEST[63:32] ← ZERO_FILL;
ELSE
    DEST[31:0] ← (SRC >> (32 * imm8[1:0])) AND 0FFFFFFFh;
FI;

Intel C/C++ Compiler Intrinsic Equivalent

EXTRACTPS int _mm_extract_ps(__m128 src, const intndx);

SIMD Floating-Point Exceptions

None

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code)  For a page fault.
#NM                If CR0.TS[bit 3] = 1.
#UD                If CR0.EM[bit 2] = 1.
                 If CR4.OSFXSR[bit 9] = 0.
                 If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
                 If LOCK prefix is used.
                 Either the prefix REP (F3h) or REPN (F2H) is used.
#AC(0)            If alignment checking is enabled and an unaligned memory
                 reference is made while the current privilege level is 3.

Real Mode Exceptions
#GP                if any part of the operand lies outside of the effective address
                 space from 0 to 0FFFFH.
#NM                If CR0.TS[bit 3] = 1.
#UD                If CR0.EM[bit 2] = 1.
                 If CR4.OSFXSR[bit 9] = 0.
                 If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
                 If LOCK prefix is used.
                 Either the prefix REP (F3h) or REPN (F2H) is used.

Virtual 8086 Mode Exceptions
Same exceptions as in Real Address Mode.
#PF(fault-code)   For a page fault.

Compatibility Mode Exceptions
Same exceptions as in Protected Mode.

64-Bit Mode Exceptions
#GP(0)            If the memory address is in a non-canonical form.
#SS(0)            If a memory address referencing the SS segment is in a non-
                 canonical form.
#PF(fault-code)   For a page fault.
#NM                If TS in CR0 is set.
#UD                If EM in CR0 is set.
                 If OSFXSR in CR4 is 0.
                 If CPUID feature flag ECX.SSE4_1 is 0.
                 If LOCK prefix is used.
                 Either the prefix REP (F3h) or REPN (F2H) is used.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
F2XM1—Compute $2^{x-1}$

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F0</td>
<td>F2XM1</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(0) with $(2^{ST(0)} - 1)$.</td>
</tr>
</tbody>
</table>

Description

Computes the exponential value of 2 to the power of the source operand minus 1. The source operand is located in register ST(0) and the result is also stored in ST(0). The value of the source operand must lie in the range –1.0 to +1.0. If the source value is outside this range, the result is undefined.

The following table shows the results obtained when computing the exponential value of various classes of numbers, assuming that neither overflow nor underflow occurs.

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>– 1.0 to –0</td>
<td>– 0.5 to –0</td>
</tr>
<tr>
<td>– 0</td>
<td>– 0</td>
</tr>
<tr>
<td>+ 0</td>
<td>+ 0</td>
</tr>
<tr>
<td>+ 0 to +1.0</td>
<td>+ 0 to 1.0</td>
</tr>
</tbody>
</table>

Values other than 2 can be exponentiated using the following formula:

$$x^y \leftarrow 2^{(y \cdot \log_2 x)}$$

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

$$ST(0) \leftarrow (2^{ST(0)} - 1);$$

FPU Flags Affected

- **C1**
  - Set to 0 if stack underflow occurred.
  - Set if result was rounded up; cleared otherwise.
- **C0, C2, C3**
  - Undefined.

Floating-Point Exceptions

- **#IS**
  - Stack underflow occurred.
- **#IA**
  - Source operand is an SNaN value or unsupported format.
- **#D**
  - Source is a denormal value.
INSTRUCTION SET REFERENCE, A-M

#U Result is too small for destination format.

#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FABS—Absolute Value

Description
Clears the sign bit of ST(0) to create the absolute value of the operand. The following table shows the results obtained when creating the absolute value of various classes of numbers.

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>- *</td>
<td>+ *</td>
</tr>
<tr>
<td>- F</td>
<td>+ F</td>
</tr>
<tr>
<td>- 0</td>
<td>+ 0</td>
</tr>
<tr>
<td>+ 0</td>
<td>+ 0</td>
</tr>
<tr>
<td>+ F</td>
<td>+ F</td>
</tr>
<tr>
<td>+ *</td>
<td>+ *</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
ST(0) ← |ST(0)|;

FPU Flags Affected
C1 Set to 0 if stack underflow occurred; otherwise, set to 0.
C0, C2, C3 Undefined.

Floating-Point Exceptions
#IS Stack underflow occurred.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.
Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FADD/FADDP/FIADD—Add

**Description**

Adds the destination and source operands and stores the sum in the destination location. The destination operand is always an FPU register; the source operand can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format or in word or doubleword integer format.

The no-operand version of the instruction adds the contents of the ST(0) register to the ST(1) register. The one-operand version adds the contents of a memory location (either a floating-point or an integer value) to the contents of the ST(0) register. The two-operand version, adds the contents of the ST(0) register to the ST(i) register or vice versa. The value in ST(0) can be doubled by coding:

```
FADD ST(0), ST(0);
```

The FADDP instructions perform the additional operation of popping the FPU register stack after storing the result. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. (The no-operand version of the floating-point add instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FADD rather than FADDP.)

The FIADD instructions convert an integer source operand to double extended-precision floating-point format before performing the addition.

---

**Opcode Instruction**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /0</td>
<td>FADD m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Add m32fp to ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC /0</td>
<td>FADD m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Add m64fp to ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>D8 C0+i</td>
<td>FADD ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Add ST(0) to ST(i) and store result in ST(0).</td>
</tr>
<tr>
<td>DC C0+i</td>
<td>FADD ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Add ST(i) to ST(0) and store result in ST(i).</td>
</tr>
<tr>
<td>DE C0+i</td>
<td>FADDP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Add ST(0) to ST(i), store result in ST(i), and pop the register stack.</td>
</tr>
<tr>
<td>DE C1</td>
<td>FADDP</td>
<td>Valid</td>
<td>Valid</td>
<td>Add ST(0) to ST(1), store result in ST(1), and pop the register stack.</td>
</tr>
<tr>
<td>DA /0</td>
<td>FIADD m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Add m32int to ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DE /0</td>
<td>FIADD m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Add m16int to ST(0) and store result in ST(0).</td>
</tr>
</tbody>
</table>
The table on the following page shows the results obtained when adding various classes of numbers, assuming that neither overflow nor underflow occurs.

When the sum of two operands with opposite signs is 0, the result is \(+0\), except for the round toward \(-\infty\) mode, in which case the result is \(-0\). When the source operand is an integer 0, it is treated as a \(+0\).

When both operand are infinities of the same sign, the result is \(\infty\) of the expected sign. If both operands are infinities of opposite signs, an invalid-operation exception is generated. See Table 3-31.

### Table 3-31. FADD/FADDP/FIADD Results

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
<th>-(\infty)</th>
<th>-F</th>
<th>-0</th>
<th>+0</th>
<th>+F</th>
<th>+(\infty)</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-(\infty)</td>
<td>-(\infty)</td>
<td>-(\infty)</td>
<td>-(\infty)</td>
<td>-(\infty)</td>
<td>*</td>
<td>NaN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-F or -I</td>
<td>-(\infty)</td>
<td>-F</td>
<td>SRC</td>
<td>SRC</td>
<td>(\pm F or \pm 0)</td>
<td>+(\infty)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>-0</td>
<td>-(\infty)</td>
<td>DEST</td>
<td>-0</td>
<td>(\pm 0)</td>
<td>DEST</td>
<td>+(\infty)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+0</td>
<td>-(\infty)</td>
<td>DEST</td>
<td>(\pm 0)</td>
<td>+0</td>
<td>DEST</td>
<td>+(\infty)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+F or +I</td>
<td>-(\infty)</td>
<td>(\pm F or \pm 0)</td>
<td>SRC</td>
<td>SRC</td>
<td>+F</td>
<td>+(\infty)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+(\infty)</td>
<td>*</td>
<td>+(\infty)</td>
<td>+(\infty)</td>
<td>+(\infty)</td>
<td>+(\infty)</td>
<td>NaN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.

I Means integer.

* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

### Operation

IF Instruction = FIADD

THEN

\[
\text{DEST} \leftarrow \text{DEST} + \text{ConvertToDoubleExtendedPrecisionFP}(\text{SRC});
\]

ELSE (* Source operand is floating-point value *)

\[
\text{DEST} \leftarrow \text{DEST} + \text{SRC};
\]

FI;

IF Instruction = FADDP

THEN

PopRegisterStack;

FI;
FPU Flags Affected

C1      Set to 0 if stack underflow occurred.
       Set if result was rounded up; cleared otherwise.
C0, C2, C3      Undefined.

Floating-Point Exceptions

#IS      Stack underflow occurred.
#IA      Operand is an SNaN value or unsupported format.
       Operands are infinities of unlike sign.
#D       Source operand is a denormal value.
#U       Result is too small for destination format.
#O       Result is too large for destination format.
#P       Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#GP(0)   If a memory operand effective address is outside the CS, DS,
       ES, FS, or GS segment limit.
       If the DS, ES, FS, or GS register contains a NULL segment
       selector.
#SS(0)   If a memory operand effective address is outside the SS
       segment limit.
#NM      CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code)   If a page fault occurs.
#AC(0)   If alignment checking is enabled and an unaligned memory
       reference is made while the current privilege level is 3.
#UD      If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP      If a memory operand effective address is outside the CS, DS,
       ES, FS, or GS segment limit.
#SS      If a memory operand effective address is outside the SS
       segment limit.
#NM      CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD      If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0)   If a memory operand effective address is outside the CS, DS,
       ES, FS, or GS segment limit.
#SS(0)   If a memory operand effective address is outside the SS
       segment limit.
INSTRUCTION SET REFERENCE, A-M

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FBLD—Load Binary Coded Decimal

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /4</td>
<td>FBLD m80 dec</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert BCD value to floating-point and push onto the FPU stack.</td>
</tr>
</tbody>
</table>

**Description**

Converts the BCD source operand into double extended-precision floating-point format and pushes the value onto the FPU stack. The source operand is loaded without rounding errors. The sign of the source operand is preserved, including that of −0.

The packed BCD digits are assumed to be in the range 0 through 9; the instruction does not check for invalid digits (AH through FH). Attempting to load an invalid encoding produces an undefined result.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

TOP ← TOP − 1;
ST(0) ← ConvertToDoubleExtendedPrecisionFP(SRC);

**FPU Flags Affected**

C1 Set to 1 if stack overflow occurred; otherwise, set to 0.
C0, C2, C3 Undefined.

**Floating-Point Exceptions**

#IS Stack overflow occurred.

**Protected Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
FBSTP—Store BCD Integer and Pop

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /6</td>
<td>FBSTP m80bcd</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m80bcd and pop ST(0).</td>
</tr>
</tbody>
</table>

Description

Converts the value in the ST(0) register to an 18-digit packed BCD integer, stores the result in the destination operand, and pops the register stack. If the source value is a non-integral value, it is rounded to an integer value, according to rounding mode specified by the RC field of the FPU control word. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

The destination operand specifies the address where the first byte destination value is to be stored. The BCD value (including its sign bit) requires 10 bytes of space in memory.

The following table shows the results obtained when storing various classes of numbers in packed BCD format.

Table 3-32. FBSTP Results

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>-∞ or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
<tr>
<td>$F \leq -1$</td>
<td>$-D$</td>
</tr>
<tr>
<td>$-1 &lt; F &lt; -0$</td>
<td>**</td>
</tr>
<tr>
<td>$-0$</td>
<td>$-0$</td>
</tr>
<tr>
<td>$+0$</td>
<td>$+0$</td>
</tr>
<tr>
<td>$+0 &lt; F &lt; +1$</td>
<td>**</td>
</tr>
<tr>
<td>$F \geq +1$</td>
<td>$+D$</td>
</tr>
<tr>
<td>+∞ or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>*</td>
</tr>
</tbody>
</table>

NOTES:

F Means finite floating-point value.
D Means packed-BCD number.
* Indicates floating-point invalid-operation (#IA) exception.
** ±0 or ±1, depending on the rounding mode.

If the converted value is too large for the destination format, or if the source operand is an $\infty$, SNaN, QNaN, or is in an unsupported format, an invalid-arithmetic-operand condition is signaled. If the invalid-operation exception is not masked, an invalid-arithmetic-operand exception (#IA) is generated and no value is stored in the desti-
nation operand. If the invalid-operation exception is masked, the packed BCD indefinite value is stored in memory.
This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

`DEST ← BCD(ST(0));`
`PopRegisterStack;`

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred.
- Set if result was rounded up; cleared otherwise.
- **C0, C2, C3** Undefined.

**Floating-Point Exceptions**

- **#IS** Stack underflow occurred.
- **#IA** Converted value that exceeds 18 BCD digits in length.
  Source operand is an SNaN, QNaN, ±∞, or in an unsupported format.
- **#P** Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- **#GP(0)** If a segment register is being loaded with a segment selector that points to a non-writable segment.
  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS** If a memory operand effective address is outside the SS segment limit.
FBSTP—Store BCD Integer and Pop

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
**FCHS—Change Sign**

**Description**
Complements the sign bit of ST(0). This operation changes a positive value into a negative value of equal magnitude or vice versa. The following table shows the results obtained when changing the sign of various classes of numbers.

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>- •</td>
<td>+ •</td>
</tr>
<tr>
<td>- F</td>
<td>+ F</td>
</tr>
<tr>
<td>- 0</td>
<td>+ 0</td>
</tr>
<tr>
<td>+ 0</td>
<td>- 0</td>
</tr>
<tr>
<td>+ F</td>
<td>- F</td>
</tr>
<tr>
<td>+ •</td>
<td>- •</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**
* F means finite floating-point value.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**
\[
\text{SignBit(ST(0))} \leftarrow \text{NOT (SignBit(ST(0)))};
\]

**FPU FlagsAffected**
- **C1**: Set to 0 if stack underflow occurred; otherwise, set to 0.
- **C0, C2, C3**: Undefined.

**Floating-Point Exceptions**
- **#IS**: Stack underflow occurred.

**Protected Mode Exceptions**
- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#UD**: If the LOCK prefix is used.
Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FCLEX/FNCLEX—Clear Exceptions

Description
Clears the floating-point exception flags (PE, UE, OE, ZE, DE, and IE), the exception summary status flag (ES), the stack fault flag (SF), and the busy flag (B) in the FPU status word. The FCLEX instruction checks for and handles any pending unmasked floating-point exceptions before clearing the exception flags; the FNCLEX instruction does not.

The assembler issues two instructions for the FCLEX instruction (an FWAIT instruction followed by an FNCLEX instruction), and the processor executes each of these instructions separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

IA-32 Architecture Compatibility
When operating a Pentium or Intel486 processor in MS-DOS* compatibility mode, it is possible (under unusual circumstances) for an FNCLEX instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled “No-Wait FPU Instructions Can Get FPU Interrupt in Window” in Appendix D of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a description of these circumstances. An FNCLEX instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

This instruction affects only the x87 FPU floating-point exception flags. It does not affect the SIMD floating-point exception flags in the MXCRS register.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
FPUStatusWord[0:7] ← 0;
FPUStatusWord[15] ← 0;

NOTES:
* See IA-32 Architecture Compatibility section below.
FPU Flags Affected
The PE, UE, OE, ZE, DE, IE, ES, SF, and B flags in the FPU status word are cleared. The C0, C1, C2, and C3 flags are undefined.

Floating-Point Exceptions
None.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FCMOVcc—Floating-Point Conditional Move

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode*</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DA C0+i</td>
<td>FCMOVB ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below (CF=1).</td>
</tr>
<tr>
<td>DA C8+i</td>
<td>FCMOVE ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if equal (ZF=1).</td>
</tr>
<tr>
<td>DA D0+i</td>
<td>FCMOVBE ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>DA DB+i</td>
<td>FCMOVU ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if unordered (PF=1).</td>
</tr>
<tr>
<td>DB C0+i</td>
<td>FCMOVNB ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not below (CF=0).</td>
</tr>
<tr>
<td>DB C8+i</td>
<td>FCMOVNE ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not equal (ZF=0).</td>
</tr>
<tr>
<td>DB D0+i</td>
<td>FCMOVNBE ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not below or equal (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>DB DB+i</td>
<td>FCMOVNU ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not unordered (PF=0).</td>
</tr>
</tbody>
</table>

**NOTES:**
* See IA-32 Architecture Compatibility section below.

**Description**

Tests the status flags in the EFLAGS register and moves the source operand (second operand) to the destination operand (first operand) if the given test condition is true. The condition for each mnemonic os given in the Description column above and in Chapter 8 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*. The source operand is always in the ST(i) register and the destination operand is always ST(0).

The FCMOVcc instructions are useful for optimizing small IF constructions. They also help eliminate branching overhead for IF operations and the possibility of branch mispredictions by the processor.

A processor may not support the FCMOVcc instructions. Software can check if the FCMOVcc instructions are supported by checking the processor’s feature information with the CPUID instruction (see “COMISS—Compare Scalar Ordered Single-Precision Floating-Point Values and Set EFLAGS” in this chapter). If both the CMOV and FPU feature bits are set, the FCMOVcc instructions are supported.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

The FCMOVcc instructions were introduced to the IA-32 Architecture in the P6 family processors and are not available in earlier IA-32 processors.
FCMOVcc—Floating-Point Conditional Move

**Operation**

IF condition TRUE
    THEN ST(0) ← ST(i);
FI;

**FPU Flags Affected**

C1 Set to 0 if stack underflow occurred.
C0, C2, C3 Undefined.

**Floating-Point Exceptions**

#IS Stack underflow occurred.

**Integer Flags Affected**

None.

**Protected Mode Exceptions**

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
FCOM/FCOMP/FCOMPP—Compare Floating Point Values

Description

Compares the contents of register ST(0) and source value and sets condition code flags C0, C2, and C3 in the FPU status word according to the results (see the table below). The source operand can be a data register or a memory location. If no source operand is given, the value in ST(0) is compared with the value in ST(1). The sign of zero is ignored, so that –0.0 is equal to +0.0.

This instruction checks the class of the numbers being compared (see "FXAM—Examine ModR/M" in this chapter). If either operand is a NaN or is in an unsupported format, an invalid-arithmetic-operand exception (#IA) is raised and, if the exception is masked, the condition flags are set to “unordered.” If the invalid-arithmetic-operand exception is unmasked, the condition code flags are not set.

Table 3-34. FCOM/FCOMP/FCOMPP Results

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; SRC</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; SRC</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = SRC</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered*</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTES:

* Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.
The FCOMP instruction pops the register stack following the comparison operation and the FCOMPP instruction pops the register stack twice following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

The FCOM instructions perform the same operation as the FUCOM instructions. The only difference is how they handle QNaN operands. The FCOM instructions raise an invalid-arithmetic-operand exception (#IA) when either or both of the operands is a NaN value or is in an unsupported format. The FUCOM instructions perform the same operation as the FCOM instructions, except that they do not generate an invalid-arithmetic-operand exception for QNaNs.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

CASE (relation of operands) OF

- **ST > SRC**: C3, C2, C0 ← 000;
- **ST < SRC**: C3, C2, C0 ← 001;
- **ST = SRC**: C3, C2, C0 ← 100;

ESAC;

IF ST(0) or SRC = NaN or unsupported format

THEN

#IA

IF FPUCControlWord.IM = 1

THEN

C3, C2, C0 ← 111;

FI;

FI;

IF Instruction = FCOMP

THEN

PopRegisterStack;

FI;

IF Instruction = FCOMPP

THEN

PopRegisterStack;

PopRegisterStack;

FI;

**FPU Flags Affected**

- **C1**: Set to 0 if stack underflow occurred; otherwise, set to 0.
- **C0, C2, C3**: See table on previous page.
Floating-Point Exceptions

#IS Stack underflow occurred.
#IA One or both operands are NaN values or have unsupported formats.
Register is marked empty.
#D One or both operands are denormal values.

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FCOMI/FCOMIP/FUCOMI/FUCOMIP—Compare Floating Point Values and Set EFLAGS

**Description**

Performs an unordered comparison of the contents of registers ST(0) and ST(i) and sets the status flags ZF, PF, and CF in the EFLAGS register according to the results (see the table below). The sign of zero is ignored for comparisons, so that –0.0 is equal to +0.0.

**Table 3-35. FCOMI/FCOMIP/ FUCOMI/FUCOMIP Results**

<table>
<thead>
<tr>
<th>Comparison Results*</th>
<th>ZF</th>
<th>PF</th>
<th>CF</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST0 &gt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST0 &lt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST0 = ST(i)</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered**</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**NOTES:**

* See the IA-32 Architecture Compatibility section below.

**Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.

An unordered comparison checks the class of the numbers being compared (see “FXAM—Examine ModR/M” in this chapter). The FUCOMI/FUCOMIP instructions perform the same operations as the FCOMI/FCOMIP instructions. The only difference is that the FUCOMI/FUCOMIP instructions raise the invalid-arithmetic-operand exception (#IA) only when either or both operands are an SNaN or are in an unsupported format; QNaNs cause the condition code flags to be set to unordered, but do not cause an exception to be generated. The FCOMI/FCOMIP instructions raise an invalid-operation exception when either or both of the operands are a NaN value of any kind or are in an unsupported format.
If the operation results in an invalid-arithmetic-operand exception being raised, the status flags in the EFLAGS register are set only if the exception is masked.

The FCOMI/FCOMIP and FUCOMI/FUCOMIP instructions clear the OF flag in the EFLAGS register (regardless of whether an invalid-operation exception is detected).

The FCOMIP and FUCOMIP instructions also pop the register stack following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

The FCOMI/FCOMIP/FUCOMI/FUCOMIP instructions were introduced to the IA-32 Architecture in the P6 family processors and are not available in earlier IA-32 processors.

**Operation**

CASE (relation of operands) OF

\[\text{ST}(0) > \text{ST}(i): \quad ZF, PF, CF \leftarrow 000;\]
\[\text{ST}(0) < \text{ST}(i): \quad ZF, PF, CF \leftarrow 001;\]
\[\text{ST}(0) = \text{ST}(i): \quad ZF, PF, CF \leftarrow 100;\]

ESAC;

IF Instruction is FCOMI or FCOMIP
THEN
  IF ST(0) or ST(i) = NaN or unsupported format
  THEN
    #IA
    IF FPUControlWord.IM = 1
    THEN
      ZF, PF, CF ← 111;
    FI;
  FI;

IF Instruction is FUCOMI or FUCOMIP
THEN
  IF ST(0) or ST(i) = QNaN, but not SNaN or unsupported format
  THEN
    ZF, PF, CF ← 111;
  ELSE (* ST(0) or ST(i) is SNaN or unsupported format *)
    #IA;
    IF FPUControlWord.IM = 1
    THEN
ZF, PF, CF ← 111;
FT;
FI;
FI;
IF Instruction is FCOMIP or FUCOMIP
    THEN
        PopRegisterStack;
FI;

FPU Flags Affected
C1 Set to 0 if stack underflow occurred; otherwise, set to 0.
C0, C2, C3 Not affected.

Floating-Point Exceptions
#IS Stack underflow occurred.
#IA (FCOMI or FCOMIP instruction) One or both operands are NaN values or have unsupported formats.
(FUCOMI or FUCOMIP instruction) One or both operands are SNaN values (but not QNaNs) or have undefined formats.
Detection of a QNaN value does not raise an invalid-operand exception.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FCOS—Cosine

Description

Computes the cosine of the source operand in register ST(0) and stores the result in ST(0). The source operand must be given in radians and must be within the range $-2^{63}$ to $+2^{63}$. The following table shows the results obtained when taking the cosine of various classes of numbers.

Table 3-36. FCOS Results

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>- F</td>
<td>-1 to +1</td>
</tr>
<tr>
<td>- 0</td>
<td>+1</td>
</tr>
<tr>
<td>+ 0</td>
<td>+1</td>
</tr>
<tr>
<td>+ F</td>
<td>-1 to +1</td>
</tr>
<tr>
<td>+ •</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range $-2^{63}$ to $+2^{63}$ can be reduced to the range of the instruction by subtracting an appropriate integer multiple of $2\pi$ or by using the FPREM instruction with a divisor of $2\pi$. See the section titled “Pi” in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a discussion of the proper value to use for $\pi$ in performing such reductions.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

IF $|ST(0)| < 2^{63}$
THEN
   C2 ← 0;
INSTRUCTION SET REFERENCE, A-M

ST(0) ← \text{cosine}(ST(0));
ELSE (* Source operand is out-of-range *)
    C2 ← 1;
FI;

**FPU Flags Affected**

C1  Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.
    Undefined if C2 is 1.

C2  Set to 1 if outside range \((-2^{63} < \text{source operand} < 2^{63})\); otherwise, set to 0.

C0, C3  Undefined.

**Floating-Point Exceptions**

#IS  Stack underflow occurred.

#IA  Source operand is an SNaN value, \(\infty\), or unsupported format.

#D  Source is a denormal value.

#P  Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF  If there is a pending x87 FPU exception.

#UD  If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
FDECSTP—Decrement Stack-Top Pointer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F6</td>
<td>FDECSTP</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement TOP field in FPU status word.</td>
</tr>
</tbody>
</table>

**Description**

Subtracts one from the TOP field of the FPU status word (decrements the top-of-stack pointer). If the TOP field contains a 0, it is set to 7. The effect of this instruction is to rotate the stack by one position. The contents of the FPU data registers and tag register are not affected.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

```plaintext
IF TOP = 0  
  THEN TOP ← 7;  
  ELSE TOP ← TOP - 1;
FI;
```

**FPU Flags Affected**

The C1 flag is set to 0. The C0, C2, and C3 flags are undefined.

**Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #MF If there is a pending x87 FPU exception.
- #UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FDIV/FDIVP/FIDIV—Divide

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /6</td>
<td>FDIV m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by m32fp and store result in ST(0).</td>
</tr>
<tr>
<td>DC /6</td>
<td>FDIV m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by m64fp and store result in ST(0).</td>
</tr>
<tr>
<td>D8 F0+i</td>
<td>FDIV ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by ST(i) and store result in ST(0).</td>
</tr>
<tr>
<td>DC F8+i</td>
<td>FDIV ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(i) by ST(0) and store result in ST(i).</td>
</tr>
<tr>
<td>DE F8+i</td>
<td>FDIVP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(i) by ST(0), store result in ST(0), and pop the register stack.</td>
</tr>
<tr>
<td>DE F9</td>
<td>FDIVP</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(1) by ST(0), store result in ST(1), and pop the register stack.</td>
</tr>
<tr>
<td>DA /6</td>
<td>FIDIV m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by m32int and store result in ST(0).</td>
</tr>
<tr>
<td>DE /6</td>
<td>FIDIV m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by m64int and store result in ST(0).</td>
</tr>
</tbody>
</table>

Description

Divides the destination operand by the source operand and stores the result in the destination location. The destination operand (dividend) is always in an FPU register; the source operand (divisor) can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format, word or doubleword integer format.

The no-operand version of the instruction divides the contents of the ST(1) register by the contents of the ST(0) register. The one-operand version divides the contents of the ST(0) register by the contents of a memory location (either a floating-point or an integer value). The two-operand version, divides the contents of the ST(0) register by the contents of the ST(i) register or vice versa.

The FDIVP instructions perform the additional operation of popping the FPU register stack after storing the result. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point divide instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FDIV rather than FDIVP.

The FIDIV instructions convert an integer source operand to double extended-precision floating-point format before performing the division. When the source operand is an integer 0, it is treated as a +0.
If an unmasked divide-by-zero exception (#Z) is generated, no result is stored; if the exception is masked, an $\infty$ of the appropriate sign is stored in the destination operand.

The following table shows the results obtained when dividing various classes of numbers, assuming that neither overflow nor underflow occurs.

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
<th>-•</th>
<th>-F</th>
<th>0</th>
<th>+0</th>
<th>+F</th>
<th>++</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-•</td>
<td>$-\infty$</td>
<td>+0</td>
<td>+0</td>
<td>-0</td>
<td>-0</td>
<td>-0</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>-F</td>
<td>$+\infty$</td>
<td>+F</td>
<td>+0</td>
<td>-0</td>
<td>-0</td>
<td>-F</td>
<td>-•</td>
<td>NaN</td>
</tr>
<tr>
<td>-I</td>
<td>$+\infty$</td>
<td>+F</td>
<td>+0</td>
<td>-0</td>
<td>-F</td>
<td>-•</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>-0</td>
<td>**</td>
<td>**</td>
<td>*</td>
<td>*</td>
<td>**</td>
<td>*</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+0</td>
<td>-•</td>
<td>**</td>
<td>*</td>
<td>*</td>
<td>++</td>
<td>*</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+I</td>
<td>-•</td>
<td>-F</td>
<td>-0</td>
<td>+0</td>
<td>+F</td>
<td>++</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+F</td>
<td>-•</td>
<td>-F</td>
<td>-0</td>
<td>+0</td>
<td>+F</td>
<td>++</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>++</td>
<td>*</td>
<td>-0</td>
<td>-0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
- F Means finite floating-point value.
- I Means integer.
- * Indicates floating-point invalid-arithmetic-operand (#IA) exception.
- ** Indicates floating-point zero-divide (#Z) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

IF SRC = 0
THEN
  #Z;
ELSE
  IF Instruction is FIDIV
  THEN
    DEST ← DEST / ConvertToDoubleExtendedPrecisionFP(SRC);
  ELSE (* Source operand is floating-point value *)
    DEST ← DEST / SRC;
  FI;
FI;

Table 3-37. FDIV/FDIVP/FIDIV Results
FDIV/FDIVP/FIDIV—Divide

IF Instruction = FDIVP
  THEN
    PopRegisterStack;
FI;

**FPU Flags Affected**

C1  Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.

C0, C2, C3  Undefined.

**Floating-Point Exceptions**

#IS  Stack underflow occurred.
#IA   Operand is an SNaN value or unsupported format.
      \( \pm\infty / \pm\infty; \pm0 / \pm0 \)
#D    Source is a denormal value.
#Z    DEST / \pm0, where DEST is not equal to \pm0.
#U    Result is too small for destination format.
#O    Result is too large for destination format.
#P    Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM   CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD   If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP   If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS   If a memory operand effective address is outside the SS segment limit.
#NM   CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD   If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
#UD    If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#NM    CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF    If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD    If the LOCK prefix is used.
FDIVR/FDIVRP/FIDIVR—Reverse Divide

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 7</td>
<td>FDIVR m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide m32fp by ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC 7</td>
<td>FDIVR m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide m64fp by ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>D8 F8+i</td>
<td>FDIVR ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(i) by ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC F0+i</td>
<td>FDIVR ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by ST(i) and store result in ST(i).</td>
</tr>
<tr>
<td>DE F0+i</td>
<td>FDIVRP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by ST(i), store result in ST(i), and pop the register stack.</td>
</tr>
<tr>
<td>DE F1</td>
<td>FDIVRP</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by ST(1), store result in ST(1), and pop the register stack.</td>
</tr>
<tr>
<td>DA 7</td>
<td>FIDIVR m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide m32int by ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DE 7</td>
<td>FIDIVR m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide m16int by ST(0) and store result in ST(0).</td>
</tr>
</tbody>
</table>

Description

Divides the source operand by the destination operand and stores the result in the destination location. The destination operand (divisor) is always in an FPU register; the source operand (dividend) can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format, word or doubleword integer format.

These instructions perform the reverse operations of the FDIV, FDIVP, and FIDIV instructions. They are provided to support more efficient coding.

The no-operand version of the instruction divides the contents of the ST(0) register by the contents of the ST(1) register. The one-operand version divides the contents of a memory location (either a floating-point or an integer value) by the contents of the ST(0) register. The two-operand version, divides the contents of the ST(i) register by the contents of the ST(0) register or vice versa.

The FDIVRP instructions perform the additional operation of popping the FPU register stack after storing the result. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point divide instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FDIVR rather than FDIVRP.
The FIDIVR instructions convert an integer source operand to double extended-precision floating-point format before performing the division.

If an unmasked divide-by-zero exception (#Z) is generated, no result is stored; if the exception is masked, an ∞ of the appropriate sign is stored in the destination operand.

The following table shows the results obtained when dividing various classes of numbers, assuming that neither overflow nor underflow occurs.

**Table 3-38. FDIVR/FDIVRP/FIDIVR Results**

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
<th>*</th>
<th>–F</th>
<th>–0</th>
<th>+0</th>
<th>+F</th>
<th>++</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>–*</td>
<td>*</td>
<td>++</td>
<td>**</td>
<td>**</td>
<td>–F</td>
<td>–0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>–F</td>
<td>+0</td>
<td>+F</td>
<td>**</td>
<td>**</td>
<td>–F</td>
<td>–0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>–I</td>
<td>+0</td>
<td>+F</td>
<td>**</td>
<td>**</td>
<td>–F</td>
<td>–0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>–0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>*</td>
<td>–0</td>
<td>–0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+0</td>
<td>–0</td>
<td>–0</td>
<td>*</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+I</td>
<td>–0</td>
<td>–F</td>
<td>**</td>
<td>**</td>
<td>+F</td>
<td>+0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+F</td>
<td>–0</td>
<td>–F</td>
<td>**</td>
<td>**</td>
<td>+F</td>
<td>+0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>++</td>
<td>*</td>
<td>–*</td>
<td>–*</td>
<td>**</td>
<td>++</td>
<td>++</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**
- F Means finite floating-point value.
- I Means integer.
- * Indicates floating-point invalid-arithmetic-operand (#IA) exception.
- ** Indicates floating-point zero-divide (#Z) exception.

When the source operand is an integer 0, it is treated as a +0. This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

IF DEST = 0
THEN
    #Z;
ELSE
    IF Instruction = FIDIVR
    THEN
        DEST ← ConvertToDoubleExtendedPrecisionFP(SRC) / DEST;
    ELSE (* Source operand is floating-point value *)

3-360  Vol. 2A  FDIVR/FDIVRP/FIDIVR—Reverse Divide
DEST ← SRC / DEST;
F0;
F0;

IF Instruction = FDIVRP
THEN
  PopRegisterStack;
F0;

FPU Flags Affected
C1    Set to 0 if stack underflow occurred.
     Set if result was rounded up; cleared otherwise.
C0, C2, C3 Undefi ned.

Floating-Point Exceptions
#IS Stack underflow occurred.
#IA Operand is an SNaN value or unsupported format.
      ±∞ / ±∞; ±0 / ±0
#D Source is a denormal value.
#Z SRC / ±0, where SRC is not equal to ±0.
#U Result is too small for destination format.
#O Result is too large for destination format.
#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS,
      ES, FS, or GS segment limit.
     If the DS, ES, FS, or GS register contains a NULL segment
     selector.
#SS(0) If a memory operand effective address is outside the SS
      segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory
      reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS,
      ES, FS, or GS segment limit.
INSTRUCTION SET REFERENCE, A-M

#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
**FFREE—Free Floating-Point Register**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DD C0+i</td>
<td>FFREE ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Sets tag for ST(i) to empty.</td>
</tr>
</tbody>
</table>

**Description**

Sets the tag in the FPU tag register associated with register ST(i) to empty (11B). The contents of ST(i) and the FPU stack-top pointer (TOP) are not affected. This instruction's operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

TAG(i) ← 11B;

**FPU Flags Affected**

C0, C1, C2, C3 undefined.

**Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- #NM if CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #MF if there is a pending x87 FPU exception.
- #UD if the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
**FICOM/FICOMP—Compare Integer**

**Description**

Compares the value in ST(0) with an integer source operand and sets the condition code flags C0, C2, and C3 in the FPU status word according to the results (see table below). The integer value is converted to double extended-precision floating-point format before the comparison is made.

**Table 3-39. FICOM/FICOMP Results**

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; SRC</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; SRC</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = SRC</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

These instructions perform an “unordered comparison.” An unordered comparison also checks the class of the numbers being compared (see “FXAM—Examine ModR/M” in this chapter). If either operand is a NaN or is in an undefined format, the condition flags are set to “unordered.”

The sign of zero is ignored, so that –0.0 ← +0.0.

The FICOMP instructions pop the register stack following the comparison. To pop the register stack, the processor marks the ST(0) register empty and increments the stack pointer (TOP) by 1.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

CASE (relation of operands) OF

- ST(0) > SRC: C3, C2, C0 ← 000;
- ST(0) = SRC: C3, C2, C0 ← 001;
- ST(0) = SRC: C3, C2, C0 ← 100;
- Unordered: C3, C2, C0 ← 111;
ESAC;
IF Instruction = FICOMP
    THEN
        PopRegisterStack;
FI;

FPU Flags Affected
C1    Set to 0 if stack underflow occurred; otherwise, set to 0.
C0, C2, C3 See table on previous page.

Floating-Point Exceptions
#IS    Stack underflow occurred.
#IA    One or both operands are NaN values or have unsupported formats.
#D     One or both operands are denormal values.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM    CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD    If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS    If a memory operand effective address is outside the SS segment limit.
#NM    CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD    If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
INSTRUCTION SET REFERENCE, A-M

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
FILD—Load Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /0</td>
<td>FILD m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Push m16int onto the FPU register stack.</td>
</tr>
<tr>
<td>DB /0</td>
<td>FILD m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Push m32int onto the FPU register stack.</td>
</tr>
<tr>
<td>DF /5</td>
<td>FILD m64int</td>
<td>Valid</td>
<td>Valid</td>
<td>Push m64int onto the FPU register stack.</td>
</tr>
</tbody>
</table>

Description

Converts the signed-integer source operand into double extended-precision floating-point format and pushes the value onto the FPU register stack. The source operand can be a word, doubleword, or quadword integer. It is loaded without rounding errors. The sign of the source operand is preserved.

This instruction's operation is the same in non-64-bit modes and 64-bit mode.

Operation

TOP ← TOP – 1;
ST(0) ← ConvertToDoubleExtendedPrecisionFP(SRC);

FPU Flags Affected

C1 Set to 1 if stack overflow occurred; set to 0 otherwise.
C0, C2, C3 Undefined.

Floating-Point Exceptions

#IS Stack overflow occurred.

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
INSTRUCTION SET REFERENCE, A-M

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FINCSTP—Increment Stack-Top Pointer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F7</td>
<td>FINCSTP</td>
<td>Valid</td>
<td>Valid</td>
<td>Increment the TOP field in the FPU status register.</td>
</tr>
</tbody>
</table>

Description

Adds one to the TOP field of the FPU status word (increments the top-of-stack pointer). If the TOP field contains a 7, it is set to 0. The effect of this instruction is to rotate the stack by one position. The contents of the FPU data registers and tag register are not affected. This operation is not equivalent to popping the stack, because the tag for the previous top-of-stack register is not marked empty.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

IF TOP = 7
    THEN TOP ← 0;
    ELSE TOP ← TOP + 1;
Fi;

FPU Flags Affected

The C1 flag is set to 0. The C0, C2, and C3 flags are undefined.

Floating-Point Exceptions

None.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-M

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**FINIT/FNINIT—Initialize Floating-Point Unit**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DB E3</td>
<td>FINIT</td>
<td>Valid</td>
<td>Valid</td>
<td>Initialize FPU after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>DB E3</td>
<td>FNINIT*</td>
<td>Valid</td>
<td>Valid</td>
<td>Initialize FPU without checking for pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

**NOTES:**
* See IA-32 Architecture Compatibility section below.

**Description**
Sets the FPU control, status, tag, instruction pointer, and data pointer registers to their default states. The FPU control word is set to 037FH (round to nearest, all exceptions masked, 64-bit precision). The status word is cleared (no exception flags set, TOP is set to 0). The data registers in the register stack are left unchanged, but they are all tagged as empty (11B). Both the instruction and data pointers are cleared.

The FINIT instruction checks for and handles any pending unmasked floating-point exceptions before performing the initialization; the FNINIT instruction does not.

The assembler issues two instructions for the FINIT instruction (an FWAIT instruction followed by an FNINIT instruction), and the processor executes each of these instructions in separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**
When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNINIT instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled “No-Wait FPU Instructions Can Get FPU Interrupt in Window” in Appendix D of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a description of these circumstances. An FNINIT instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

In the Intel387 math coprocessor, the FINIT/FNINIT instruction does not clear the instruction and data pointers.

This instruction affects only the x87 FPU. It does not affect the XMM and MXCSR registers.
INSTRUCTION SET REFERENCE, A-M

Operation
FPUCtrlWord ← 037FH;
FPUStratusWord ← 0;
FPUTagWord ← FFFFH;
FPUDataPointer ← 0;
FPUInstructionPointer ← 0;
FPULastInstructionOpcode ← 0;

FPU Flags Affected
C0, C1, C2, C3 set to 0.

Floating-Point Exceptions
None.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**FIST/FISTP—Store Integer**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /2</td>
<td>FIST m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m16int.</td>
</tr>
<tr>
<td>DB /2</td>
<td>FIST m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m32int.</td>
</tr>
<tr>
<td>DF /3</td>
<td>FISTP m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m16int and pop register stack.</td>
</tr>
<tr>
<td>DB /3</td>
<td>FISTP m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m32int and pop register stack.</td>
</tr>
<tr>
<td>DF /7</td>
<td>FISTP m64int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m64int and pop register stack.</td>
</tr>
</tbody>
</table>

**Description**

The FIST instruction converts the value in the ST(0) register to a signed integer and stores the result in the destination operand. Values can be stored in word or double-word integer format. The destination operand specifies the address where the first byte of the destination value is to be stored.

The FISTP instruction performs the same operation as the FIST instruction and then pops the register stack. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The FISTP instruction also stores values in quadword integer format.

The following table shows the results obtained when storing various classes of numbers in integer format.

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>• or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
<tr>
<td>( F \leq -1 )</td>
<td>-1</td>
</tr>
<tr>
<td>(-1 &lt; F &lt; 0 )</td>
<td>**</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>+0</td>
<td>0</td>
</tr>
<tr>
<td>(+0 &lt; F &lt; +1 )</td>
<td>**</td>
</tr>
<tr>
<td>( F \geq +1 )</td>
<td>+1</td>
</tr>
<tr>
<td>• or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
</tbody>
</table>

**Table 3-40. FIST/FISTP Results**
If the source value is a non-integral value, it is rounded to an integer value, according to the rounding mode specified by the RC field of the FPU control word.

If the converted value is too large for the destination format, or if the source operand is an $\infty$, SNaN, QNAN, or is in an unsupported format, an invalid-arithmetic-operand condition is signaled. If the invalid-operation exception is not masked, an invalid-arithmetic-operand exception (#IA) is generated and no value is stored in the destination operand. If the invalid-operation exception is masked, the integer indefinite value is stored in memory.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

DEST $\leftarrow$ Integer(ST(0));

IF Instruction = FISTP
   THEN
       PopRegisterStack;
   FI;

**FPU Flags Affected**

C1 Set to 0 if stack underflow occurred.
Indicates rounding direction of if the inexact exception (#P) is generated: 0 $\leftarrow$ not roundup; 1 $\leftarrow$ roundup.
Set to 0 otherwise.
C0, C2, C3 Undefined.

**Floating-Point Exceptions**

#IS Stack underflow occurred.
#IA Converted value is too large for the destination format.
Source operand is an SNaN, QNaN, $\pm\infty$, or unsupported format.
#P Value cannot be represented exactly in destination format.
Protected Mode Exceptions

#GP(0)  If the destination is located in a non-writable segment.
        If a memory operand effective address is outside the CS, DS,
        ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register is used to access memory and it
        contains a NULL segment selector.
#SS(0)  If a memory operand effective address is outside the SS
        segment limit.
#NM     CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made while the current privilege level is 3.
#UD     If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS,
     ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS
     segment limit.
#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS,
        ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS
        segment limit.
#NM     CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made.
#UD     If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-
        canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#NM        CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF        If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0)     If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD        If the LOCK prefix is used.
FISTTP—Store Integer with Truncation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /1</td>
<td>FISTTP m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m16int with truncation.</td>
</tr>
<tr>
<td>DB /1</td>
<td>FISTTP m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m32int with truncation.</td>
</tr>
<tr>
<td>DD /1</td>
<td>FISTTP m64int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m64int with truncation.</td>
</tr>
</tbody>
</table>

Description

FISTTP converts the value in ST into a signed integer using truncation (chop) as rounding mode, transfers the result to the destination, and pop ST. FISTTP accepts word, short integer, and long integer destinations.

The following table shows the results obtained when storing various classes of numbers in integer format.

Table 3-41. FISTTP Results

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>-• or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
<tr>
<td>F ≤ -1</td>
<td>0</td>
</tr>
<tr>
<td>-1 &lt; F &lt; +1</td>
<td>0</td>
</tr>
<tr>
<td>F ≥ +1</td>
<td>+1</td>
</tr>
<tr>
<td>+• or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>*</td>
</tr>
</tbody>
</table>

NOTES:

F Means finite floating-point value.
I Means integer.
* Indicates floating-point invalid-operation (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

DEST ← ST;
pop ST;

Flags Affected

C1 is cleared; C0, C2, C3 undefined.
Numeric Exceptions
Invalid, Stack Invalid (stack underflow), Precision.

Protected Mode Exceptions
#GP(0) If the destination is in a nonwritable segment.
For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#NM If CR0.EM[bit 2] = 1.
If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.

Real Address Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
#NM If CR0.EM[bit 2] = 1.
If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.

Virtual 8086 Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
#NM If CR0.EM[bit 2] = 1.
If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
#PF(fault-code) For a page fault.
#AC(0) For unaligned memory reference if the current privilege is 3.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

If the LOCK prefix is used.
FLD—Load Floating Point Value

**Description**

Pushes the source operand onto the FPU register stack. The source operand can be in single-precision, double-precision, or double extended-precision floating-point format. If the source operand is in single-precision or double-precision floating-point format, it is automatically converted to the double extended-precision floating-point format before being pushed on the stack.

The FLD instruction can also push the value in a selected FPU register [ST(i)] onto the stack. Here, pushing register ST(0) duplicates the stack top.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

IF SRC is ST(i)
   THEN
      temp ← ST(i);
   FI;

TOP ← TOP − 1;

IF SRC is memory-operand
   THEN
      ST(0) ← ConvertToDoubleExtendedPrecisionFP(SRC);
   ELSE (* SRC is ST(i) *)
      ST(0) ← temp;
   FI;

**FPU Flags Affected**

C1 Set to 1 if stack overflow occurred; otherwise, set to 0.
C0, C2, C3 Undefined.

**Floating-Point Exceptions**

#IS Stack underflow or overflow occurred.
#IA  Source operand is an SNaN. Does not occur if the source operand is in double extended-precision floating-point format (FLD m80fp or FLD ST(i)).

#D  Source operand is a denormal value. Does not occur if the source operand is in double extended-precision floating-point format.

**Protected Mode Exceptions**

#GP(0)  If destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD  If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

#UD  If the LOCK prefix is used.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonicial form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FLD1/FLDL2T/FLDL2E/FLDPI/FLDLG2/FLDLN2/FLDZ—Load Constant

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 EB</td>
<td>FLD1</td>
<td>Valid</td>
<td>Valid</td>
<td>Push +1.0 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 E9</td>
<td>FLDL2T</td>
<td>Valid</td>
<td>Valid</td>
<td>Push log₂10 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EA</td>
<td>FLDL2E</td>
<td>Valid</td>
<td>Valid</td>
<td>Push log₂e onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EB</td>
<td>FLDPI</td>
<td>Valid</td>
<td>Valid</td>
<td>Push π onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EC</td>
<td>FLDLG2</td>
<td>Valid</td>
<td>Valid</td>
<td>Push log₁₀2 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 ED</td>
<td>FLDLN2</td>
<td>Valid</td>
<td>Valid</td>
<td>Push logₑ2 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EE</td>
<td>FLNZ</td>
<td>Valid</td>
<td>Valid</td>
<td>Push +0.0 onto the FPU register stack.</td>
</tr>
</tbody>
</table>

NOTES:
* See IA-32 Architecture Compatibility section below.

Description
Push one of seven commonly used constants (in double extended-precision floating-point format) onto the FPU register stack. The constants that can be loaded with these instructions include +1.0, +0.0, log₂10, log₂e, π, log₁₀2, and logₑ2. For each constant, an internal 66-bit constant is rounded (as specified by the RC field in the FPU control word) to double extended-precision floating-point format. The inexact-result exception (#P) is not generated as a result of the rounding, nor is the C1 flag set in the x87 FPU status word if the value is rounded up.

See the section titled "Pi" in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a description of the π constant.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

IA-32 Architecture Compatibility
When the RC field is set to round-to-nearest, the FPU produces the same constants that is produced by the Intel 8087 and Intel 287 math coprocessors.

Operation
TOP ← TOP − 1;
ST(0) ← CONSTANT;

FPU Flags Affected
C1 Set to 1 if stack overflow occurred; otherwise, set to 0.
C0, C2, C3 Undefined.
Floating-Point Exceptions
#IS Stack overflow occurred.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FLDCW—Load x87 FPU Control Word

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 /5</td>
<td>FLDCW m2byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FPU control word from m2byte.</td>
</tr>
</tbody>
</table>

Description
Loads the 16-bit source operand into the FPU control word. The source operand is a memory location. This instruction is typically used to establish or change the FPU’s mode of operation.

If one or more exception flags are set in the FPU status word prior to loading a new FPU control word and the new control word unmasks one or more of those exceptions, a floating-point exception will be generated upon execution of the next floating-point instruction (except for the no-wait floating-point instructions, see the section titled “Software Exception Handling” in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). To avoid raising exceptions when changing FPU operating modes, clear any pending exceptions (using the FCLEX or FNCLEX instruction) before loading the new control word.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
FPUCtrlWord ← SRC;

FPU Flags Affected
C0, C1, C2, C3 undefined.

Floating-Point Exceptions
None; however, this operation might unmask a pending exception in the FPU status word. That exception is then generated upon execution of the next “waiting” floating-point instruction.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
FLDENV—Load x87 FPU Environment

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compatibility Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 /4</td>
<td>FLDENV m14/28byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FPU environment from m14byte or m28byte.</td>
</tr>
</tbody>
</table>

**Description**

Loads the complete x87 FPU operating environment from memory into the FPU registers. The source operand specifies the first byte of the operating-environment data in memory. This data is typically written to the specified memory location by a FSTENV or FNSTENV instruction.

The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. Figures 8-9 through 8-12 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, show the layout in memory of the loaded environment, depending on the operating mode of the processor (protected or real) and the current operand-size attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used.

The FLDENV instruction should be executed in the same operating mode as the corresponding FSTENV/FNSTENV instruction.

If one or more unmasked exception flags are set in the new FPU status word, a floating-point exception will be generated upon execution of the next floating-point instruction (except for the no-wait floating-point instructions, see the section titled "Software Exception Handling" in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). To avoid generating exceptions when loading a new environment, clear all the exception flags in the FPU status word that is being loaded.

If a page or limit fault occurs during the execution of this instruction, the state of the x87 FPU registers as seen by the fault handler may be different than the state being loaded from memory. In such situations, the fault handler should ignore the status of the x87 FPU registers, handle the fault, and return. The FLDENV instruction will then complete the loading of the x87 FPU registers with no resulting context inconsistency.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\begin{align*}
\text{FPUCoeffWord} & \leftarrow \text{SRC}[\text{FPUCoeffWord}]; \\
\text{FPUStrucWord} & \leftarrow \text{SRC}[\text{FPUStrucWord}]; \\
\text{FPUCoeffWord} & \leftarrow \text{SRC}[\text{FPUCoeffWord}]; \\
\text{FPUDataPointer} & \leftarrow \text{SRC}[\text{FPUDataPointer}]; \\
\text{FPULastInstructionOpcode} & \leftarrow \text{SRC}[\text{FPULastInstructionOpcode}]; \\
\text{FPULastInstructionOpcode} & \leftarrow \text{SRC}[\text{FPULastInstructionOpcode}];
\end{align*}
\]
**FPU Flags Affected**
The C0, C1, C2, C3 flags are loaded.

**Floating-Point Exceptions**
None; however, if an unmasked exception is loaded in the status word, it is generated upon execution of the next “waiting” floating-point instruction.

**Protected Mode Exceptions**
- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**
- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS** If a memory operand effective address is outside the SS segment limit.
- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#UD** If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**
- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made.
- **#UD** If the LOCK prefix is used.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FMUL/FMULP/FIMUL—Multiply

Description
Multiplies the destination and source operands and stores the product in the destination location. The destination operand is always an FPU data register; the source operand can be an FPU data register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format or in word or doubleword integer format.

The no-operand version of the instruction multiplies the contents of the ST(1) register by the contents of the ST(0) register and stores the product in the ST(1) register. The one-operand version multiplies the contents of the ST(0) register by the contents of a memory location (either a floating point or an integer value) and stores the product in the ST(0) register. The two-operand version, multiplies the contents of the ST(0) register by the contents of the ST(i) register, or vice versa, with the result being stored in the register specified with the first operand (the destination operand).

The FMULP instructions perform the additional operation of popping the FPU register stack after storing the product. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point multiply instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FMUL rather than FMULP.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /1</td>
<td>FMUL m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by m32fp and store result in ST(0).</td>
</tr>
<tr>
<td>DC /1</td>
<td>FMUL m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by m64fp and store result in ST(0).</td>
</tr>
<tr>
<td>D8 C8+i</td>
<td>FMUL ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by ST(i) and store result in ST(0).</td>
</tr>
<tr>
<td>DC C8+i</td>
<td>FMUL ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(i) by ST(0) and store result in ST(i).</td>
</tr>
<tr>
<td>DE C8+i</td>
<td>FMULP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(i) by ST(0), store result in ST(i), and pop the register stack.</td>
</tr>
<tr>
<td>DE C9</td>
<td>FMULP</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(1) by ST(0), store result in ST(1), and pop the register stack.</td>
</tr>
<tr>
<td>DA /1</td>
<td>FIMUL m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by m32int and store result in ST(0).</td>
</tr>
<tr>
<td>DE /1</td>
<td>FIMUL m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by m16int and store result in ST(0).</td>
</tr>
</tbody>
</table>
The FIMUL instructions convert an integer source operand to double extended-precision floating-point format before performing the multiplication.

The sign of the result is always the exclusive-OR of the source signs, even if one or more of the values being multiplied is 0 or \( \infty \). When the source operand is an integer 0, it is treated as a +0.

The following table shows the results obtained when multiplying various classes of numbers, assuming that neither overflow nor underflow occurs.

**Table 3-42. FMUL/FMULP/FIMUL Results**

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
<th>.-</th>
<th>-F</th>
<th>-0</th>
<th>+0</th>
<th>+F</th>
<th>+•</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>.-</td>
<td>+-</td>
<td>.-</td>
<td>.-</td>
<td>-0</td>
<td>+0</td>
<td>-F</td>
<td>-•</td>
<td>NaN</td>
</tr>
<tr>
<td>-F</td>
<td>+-</td>
<td>+F</td>
<td>+0</td>
<td>-0</td>
<td>-F</td>
<td>-•</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>-0</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>-0</td>
<td>-0</td>
<td>-0</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>*</td>
<td>-0</td>
<td>-0</td>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>+I</td>
<td>.-</td>
<td>-F</td>
<td>-0</td>
<td>+0</td>
<td>+F</td>
<td>+•</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+F</td>
<td>.-</td>
<td>.-</td>
<td>.-</td>
<td>+0</td>
<td>+F</td>
<td>+•</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+•</td>
<td>.-</td>
<td>.-</td>
<td>.-</td>
<td>.-</td>
<td>.-</td>
<td>.-</td>
<td>.-</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

F  Means finite floating-point value.
I  Means Integer.
* Indicates invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

IF Instruction = FIMUL
THEN
   DEST ← DEST * ConvertToDoubleExtendedPrecisionFP(SRC);
ELSE (* Source operand is floating-point value *)
   DEST ← DEST * SRC;
FI;

IF Instruction = FMULP
THEN
   PopRegisterStack;
FI;

FMUL/FMULP/FIMUL—Multiply
FPU Flags Affected

C1  Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.
C0, C2, C3  Undefined.

Floating-Point Exceptions

#IS  Stack underflow occurred.
#IA  Operand is an SNaN value or unsupported format.
     One operand is ±0 and the other is ±\infty.
#D  Source operand is a denormal value.
#U  Result is too small for destination format.
#O  Result is too large for destination format.
#P  Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
     If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
**FNOP—No Operation**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 D0</td>
<td>FNOP</td>
<td>Valid</td>
<td>Valid</td>
<td>No operation is performed.</td>
</tr>
</tbody>
</table>

**Description**
Performs no FPU operation. This instruction takes up space in the instruction stream but does not affect the FPU or machine context, except the EIP register.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**FPU Flags Affected**
C0, C1, C2, C3 undefined.

**Floating-Point Exceptions**
None.

**Protected Mode Exceptions**

- [#MF] If there is a pending x87 FPU exception.
- [#UD] If the LOCK prefix is used.

**Real-Address Mode Exceptions**
Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**
Same exceptions as in protected mode.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
Same exceptions as in protected mode.
FPATAN—Partial Arctangent

Computes the arctangent of the source operand in register ST(1) divided by the source operand in register ST(0), stores the result in ST(1), and pops the FPU register stack. The result in register ST(0) has the same sign as the source operand ST(1) and a magnitude less than $+\pi$.

The FPATAN instruction returns the angle between the X axis and the line from the origin to the point (X,Y), where Y (the ordinate) is ST(1) and X (the abscissa) is ST(0). The angle depends on the sign of X and Y independently, not just on the sign of the ratio Y/X. This is because a point (X,Y) is in the second quadrant, resulting in an angle between $\pi/2$ and $\pi$, while a point (X,−Y) is in the fourth quadrant, resulting in an angle between 0 and $−\pi/2$. A point (−X,Y) is in the third quadrant, giving an angle between $−\pi/2$ and $−\pi$.

The following table shows the results obtained when computing the arctangent of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F3</td>
<td>FPATAN</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(1) with arctan(ST(1)/ST(0)) and pop the register stack.</td>
</tr>
</tbody>
</table>

NOTES:
* See IA-32 Architecture Compatibility section below.
There is no restriction on the range of source operands that FPATAN can accept. This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

The source operands for this instruction are restricted for the 80287 math coprocessor to the following range:

\[ 0 \leq |ST(1)| < |ST(0)| < +\infty \]

**Operation**

\[ ST(1) \leftarrow \arctan(ST(1) / ST(0)); \]
\[ \text{PopRegisterStack}; \]

### Table 3-43. FPATAN Results

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>-F</th>
<th>-0</th>
<th>+0</th>
<th>+F</th>
<th>+N</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-F</td>
<td>-π/2</td>
<td>-π/2</td>
<td>-π/2</td>
<td>-π/2</td>
<td>-π/2</td>
<td>NaN</td>
</tr>
<tr>
<td>-0</td>
<td>-p</td>
<td>-p</td>
<td>-p</td>
<td>-0</td>
<td>-0</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>+p</td>
<td>+p</td>
<td>+0</td>
<td>+π</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+N</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.

* Table B-10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, specifies that the ratios 0/0 and +/- generate the floating-point invalid arithmetic-operation exception and, if this exception is masked, the floating-point QNaN indefinite value is returned. With the FPATAN instruction, the 0/0 or +/- value is actually not calculated using division. Instead, the arctangent of the two variables is derived from a standard mathematical formulation that is generalized to allow complex numbers as arguments. In this complex variable formulation, \( \arctan(0,0) \) etc. has well defined values. These values are needed to develop a library to compute transcendental functions with complex arguments, based on the FPU functions that only allow floating-point values as arguments.

There is no restriction on the range of source operands that FPATAN can accept.
FPATAN—Partial Arctangent

**FPU Flags Affected**

C1  Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.
C0, C2, C3  Undefined.

**Floating-Point Exceptions**

#IS  Stack underflow occurred.
#IA  Source operand is an SNaN value or unsupported format.
#D  Source operand is a denormal value.
#U  Result is too small for destination format.
#P  Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF  If there is a pending x87 FPU exception.
#UD  If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
**FPREM—Partial Remainder**

**Description**

Computes the remainder obtained from dividing the value in the ST(0) register (the dividend) by the value in the ST(1) register (the divisor or **modulus**), and stores the result in ST(0). The remainder represents the following value:

\[
\text{Remainder} \leftarrow \text{ST}(0) - (Q \times \text{ST}(1))
\]

Here, \( Q \) is an integer value that is obtained by truncating the floating-point number quotient of \( \text{ST}(0) / \text{ST}(1) \) toward zero. The sign of the remainder is the same as the sign of the dividend. The magnitude of the remainder is less than that of the modulus, unless a partial remainder was computed (as described below).

This instruction produces an exact result; the inexact-result exception does not occur and the rounding control has no effect. The following table shows the results obtained when computing the remainder of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>- •</th>
<th>-F</th>
<th>-0</th>
<th>+0</th>
<th>+F</th>
<th>++</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-F</td>
<td>ST(0)</td>
<td>-F or -0</td>
<td>**</td>
<td>**</td>
<td>-F or -0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>-0</td>
<td>-0</td>
<td>-0</td>
<td>*</td>
<td>*</td>
<td>-0</td>
<td>-0</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>ST(0)</td>
<td>+F or +0</td>
<td>**</td>
<td>**</td>
<td>+F or +0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>++</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.

* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

** Indicates floating-point zero-divide (#Z) exception.

When the result is 0, its sign is the same as that of the dividend. When the modulus is \( \infty \), the result is equal to the value in ST(0).
The FPREM instruction does not compute the remainder specified in IEEE Std 754. The IEEE specified remainder can be computed with the FPREM1 instruction. The FPREM instruction is provided for compatibility with the Intel 8087 and Intel287 math coprocessors.

The FPREM instruction gets its name "partial remainder" because of the way it computes the remainder. This instruction arrives at a remainder through iterative subtraction. It can, however, reduce the exponent of ST(0) by no more than 63 in one execution of the instruction. If the instruction succeeds in producing a remainder that is less than the modulus, the operation is complete and the C2 flag in the FPU status word is cleared. Otherwise, C2 is set, and the result in ST(0) is called the **partial remainder**. The exponent of the partial remainder will be less than the exponent of the original dividend by at least 32. Software can re-execute the instruction (using the partial remainder in ST(0) as the dividend) until C2 is cleared. (Note that while executing such a remainder-computation loop, a higher-priority interrupting routine that needs the FPU can force a context switch in-between the instructions in the loop.)

An important use of the FPREM instruction is to reduce the arguments of periodic functions. When reduction is complete, the instruction stores the three least-significant bits of the quotient in the C3, C1, and C0 flags of the FPU status word. This information is important in argument reduction for the tangent function (using a modulus of \(\pi/4\)), because it locates the original angle in the correct one of eight sectors of the unit circle.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
D \leftarrow \text{exponent}(\text{ST}(0)) - \text{exponent}(\text{ST}(1));
\]

IF \(D < 64\)

THEN

\[
Q \leftarrow \text{Integer}(\text{TruncateTowardZero}(\text{ST}(0) / \text{ST}(1))); \\
\text{ST}(0) \leftarrow \text{ST}(0) - (\text{ST}(1) \ast Q); \\
C2 \leftarrow 0; \\
C0, C3, C1 \leftarrow \text{LeastSignificantBits}(Q); (* Q2, Q1, Q0 *)
\]

ELSE

\[
C2 \leftarrow 1; \\
N \leftarrow \text{An implementation-dependent number between 32 and 63}; \\
QQ \leftarrow \text{Integer}(\text{TruncateTowardZero}((\text{ST}(0) / \text{ST}(1)) / 2^{D-N})); \\
\text{ST}(0) \leftarrow \text{ST}(0) - (\text{ST}(1) \ast QQ \ast 2^{D-N});
\]

FI;
FPU Flags Affected
C0    Set to bit 2 (Q2) of the quotient.
C1    Set to 0 if stack underflow occurred; otherwise, set to least
     significant bit of quotient (Q0).
C2    Set to 0 if reduction complete; set to 1 if incomplete.
C3    Set to bit 1 (Q1) of the quotient.

Floating-Point Exceptions
#IS   Stack underflow occurred.
#IA   Source operand is an SNaN value, modulus is 0, dividend is \( \infty \),
     or unsupported format.
#D    Source operand is a denormal value.
#U    Result is too small for destination format.

Protected Mode Exceptions
#NM   CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF   If there is a pending x87 FPU exception.
#UD   If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FPREM1—Partial Remainder

**Description**

Computes the IEEE remainder obtained from dividing the value in the ST(0) register (the dividend) by the value in the ST(1) register (the divisor or **modulus**), and stores the result in ST(0). The remainder represents the following value:

\[
\text{Remainder} \leftarrow ST(0) - (Q \times ST(1))
\]

Here, \( Q \) is an integer value that is obtained by rounding the floating-point number quotient of \([ST(0) / ST(1)]\) toward the nearest integer value. The magnitude of the remainder is less than or equal to half the magnitude of the modulus, unless a partial remainder was computed (as described below).

This instruction produces an exact result; the precision (inexact) exception does not occur and the rounding control has no effect. The following table shows the results obtained when computing the remainder of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>- •</th>
<th>-F</th>
<th>-0</th>
<th>+0</th>
<th>+F</th>
<th>+*</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-F</td>
<td>ST(0)</td>
<td>±F or -0</td>
<td>**</td>
<td>**</td>
<td>±F or -0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>-0</td>
<td>-0</td>
<td>-0</td>
<td>*</td>
<td>*</td>
<td>-0</td>
<td>-0</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>ST(0)</td>
<td>±F or +0</td>
<td>**</td>
<td>**</td>
<td>±F or +0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>+*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:

- F Means finite floating-point value.
- * Indicates floating-point invalid-arithmetic-operand (#IA) exception.
- ** Indicates floating-point zero-divide (#Z) exception.

When the result is 0, its sign is the same as that of the dividend. When the modulus is \( \infty \), the result is equal to the value in ST(0).
The FPREM1 instruction computes the remainder specified in IEEE Standard 754. This instruction operates differently from the FPREM instruction in the way that it rounds the quotient of ST(0) divided by ST(1) to an integer (see the “Operation” section below).

Like the FPREM instruction, FPREM1 computes the remainder through iterative subtraction, but can reduce the exponent of ST(0) by no more than 63 in one execution of the instruction. If the instruction succeeds in producing a remainder that is less than one half the modulus, the operation is complete and the C2 flag in the FPU status word is cleared. Otherwise, C2 is set, and the result in ST(0) is called the partial remainder. The exponent of the partial remainder will be less than the exponent of the original dividend by at least 32. Software can re-execute the instruction (using the partial remainder in ST(0) as the dividend) until C2 is cleared. (Note that while executing such a remainder-computation loop, a higher-priority interrupting routine that needs the FPU can force a context switch in-between the instructions in the loop.)

An important use of the FPREM1 instruction is to reduce the arguments of periodic functions. When reduction is complete, the instruction stores the three least-significant bits of the quotient in the C3, C1, and C0 flags of the FPU status word. This information is important in argument reduction for the tangent function (using a modulus of π/4), because it locates the original angle in the correct one of eight sectors of the unit circle.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
D \leftarrow \text{exponent}(\text{ST}(0)) - \text{exponent}(\text{ST}(1));
\]

**IF** \(D < 64\) **THEN**

\[
\begin{align*}
Q & \leftarrow \text{Integer}((\text{RoundTowardNearestInteger}(\text{ST}(0) / \text{ST}(1)))); \\
\text{ST}(0) & \leftarrow \text{ST}(0) - (\text{ST}(1) \times Q); \\
C2 & \leftarrow 0; \\
C0, C3, C1 & \leftarrow \text{LeastSignificantBits}(Q); (* Q2, Q1, Q0 *)
\end{align*}
\]

**ELSE**

\[
\begin{align*}
C2 & \leftarrow 1; \\
N & \leftarrow \text{An implementation-dependent number between 32 and 63}; \\
QQ & \leftarrow \text{Integer}((\text{TruncateTowardZero}(\text{ST}(0) / \text{ST}(1)) / 2^{(0 - N)})); \\
\text{ST}(0) & \leftarrow \text{ST}(0) - (\text{ST}(1) \times QQ \times 2^{(0 - N)});
\end{align*}
\]

**FI;**

**FPU Flags Affected**

- **C0** set to bit 2 (Q2) of the quotient.
- **C1** set to 0 if stack underflow occurred; otherwise, set to least significant bit of quotient (Q0).
FPREM1—Partial Remainder

C2 Set to 0 if reduction complete; set to 1 if incomplete.
C3 Set to bit 1 (Q1) of the quotient.

Floating-Point Exceptions

#IS Stack underflow occurred.
#IA Source operand is an SNaN value, modulus (divisor) is 0, dividend is ∞, or unsupported format.
#D Source operand is a denormal value.
#U Result is too small for destination format.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

Same exceptions as in protected mode.
FPTAN—Partial Tangent

Computes the tangent of the source operand in register ST(0), stores the result in ST(0), and pushes a 1.0 onto the FPU register stack. The source operand must be given in radians and must be less than ±2^{63}. The following table shows the unmasked results obtained when computing the partial tangent of various classes of numbers, assuming that underflow does not occur.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range −2^{63} to +2^{63} can be reduced to the range of the instruction by subtracting an appropriate integer multiple of 2\pi or by using the FPREM instruction with a divisor of 2\pi. See the section titled “Pi” in Chapter 8 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a discussion of the proper value to use for \pi in performing such reductions.

The value 1.0 is pushed onto the register stack after the tangent has been computed to maintain compatibility with the Intel 8087 and Intel287 math coprocessors. This operation also simplifies the calculation of other trigonometric functions. For instance, the cotangent (which is the reciprocal of the tangent) can be computed by executing a FDIVR instruction after the FPTAN instruction.

### Table 3-46. FPTAN Results

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>.</td>
<td>*</td>
</tr>
<tr>
<td>- F</td>
<td>− F to + F</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>+ 0</td>
<td>+ 0</td>
</tr>
<tr>
<td>+ F</td>
<td>− F to + F</td>
</tr>
<tr>
<td>±</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**
- F Means finite floating-point value.
- * Indicates floating-point invalid-arithmetic-operand (#IA) exception.
This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\text{IF } ST(0) < 2^{63} \\
\text{THEN} \\
\hspace{5mm} C2 \leftarrow 0; \\
\hspace{5mm} ST(0) \leftarrow \tan(ST(0)); \\
\hspace{5mm} TOP \leftarrow TOP - 1; \\
\hspace{5mm} ST(0) \leftarrow 1.0; \\
\hspace{5mm} \text{ELSE (* Source operand is out-of-range *)} \\
\hspace{10mm} C2 \leftarrow 1; \\
\text{FI;}
\]

**FPU Flags Affected**

- **C1**: Set to 0 if stack underflow occurred; set to 1 if stack overflow occurred.
  - Set if result was rounded up; cleared otherwise.
- **C2**: Set to 1 if outside range \((-2^{63} < \text{source operand} < +2^{63})\); otherwise, set to 0.
- **C0, C3**: Undefined.

**Floating-Point Exceptions**

- **#IS**: Stack underflow or overflow occurred.
- **#IA**: Source operand is an SNaN value, \(\infty\), or unsupported format.
- **#D**: Source operand is a denormal value.
- **#U**: Result is too small for destination format.
- **#P**: Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#MF**: If there is a pending x87 FPU exception.
- **#UD**: If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FRNDINT—Round to Integer

**Description**

Rounds the source value in the ST(0) register to the nearest integral value, depending on the current rounding mode (setting of the RC field of the FPU control word), and stores the result in ST(0).

If the source value is \( \infty \), the value is not changed. If the source value is not an integral value, the floating-point inexact-result exception (#P) is generated.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[ \text{ST}(0) \leftarrow \text{RoundToIntegralValue}(\text{ST}(0)) \]

**FPU Flags Affected**

- **C1**: Set to 0 if stack underflow occurred. Set if result was rounded up; cleared otherwise.
- **C0, C2, C3**: Undefined.

**Floating-Point Exceptions**

- **#IS**: Stack underflow occurred.
- **#IA**: Source operand is an SNaN value or unsupported format.
- **#D**: Source operand is a denormal value.
- **#P**: Source operand is not an integral value.

**Protected Mode Exceptions**

- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#MF**: If there is a pending x87 FPU exception.
- **#UD**: If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-M

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FRSTOR—Restore x87 FPU State

### Description

Loads the FPU state (operating environment and register stack) from the memory area specified with the source operand. This state data is typically written to the specified memory location by a previous FSAVE/FNSAVE instruction.

The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. Figures 8-9 through 8-12 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, show the layout in memory of the stored environment, depending on the operating mode of the processor (protected or real) and the current operand-size attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used. The contents of the FPU register stack are stored in the 80 bytes immediately following the operating environment image.

The FRSTOR instruction should be executed in the same operating mode as the corresponding FSAVE/FNSAVE instruction.

If one or more unmasked exception bits are set in the new FPU status word, a floating-point exception will be generated. To avoid raising exceptions when loading a new operating environment, clear all the exception flags in the FPU status word that is being loaded.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

### Operation

\[
\begin{align*}
\text{FPUControlWord} & \leftarrow \text{SRC}[\text{FPUControlWord}]; \\
\text{FPUSStatusWord} & \leftarrow \text{SRC}[\text{FPUSStatusWord}]; \\
\text{FPUTagWord} & \leftarrow \text{SRC}[\text{FPUTagWord}]; \\
\text{FPUDataPointer} & \leftarrow \text{SRC}[\text{FPUDataPointer}]; \\
\text{FPUIInstructionPointer} & \leftarrow \text{SRC}[\text{FPUIInstructionPointer}]; \\
\text{FPULastInstructionOpcode} & \leftarrow \text{SRC}[\text{FPULastInstructionOpcode}]; \\
\text{ST}(0) & \leftarrow \text{SRC}[\text{ST}(0)]; \\
\text{ST}(1) & \leftarrow \text{SRC}[\text{ST}(1)]; \\
\text{ST}(2) & \leftarrow \text{SRC}[\text{ST}(2)]; \\
\text{ST}(3) & \leftarrow \text{SRC}[\text{ST}(3)]; \\
\text{ST}(4) & \leftarrow \text{SRC}[\text{ST}(4)]; \\
\text{ST}(5) & \leftarrow \text{SRC}[\text{ST}(5)]; \\
\text{ST}(6) & \leftarrow \text{SRC}[\text{ST}(6)];
\end{align*}
\]

### Opcode Instruction

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DD /4</td>
<td>FRSTOR m94/108byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FPU state from m94byte or m108byte.</td>
</tr>
</tbody>
</table>
ST(7) ← SRC[ST(7)];

**FPU Flags Affected**
The C0, C1, C2, C3 flags are loaded.

**Floating-Point Exceptions**
None; however, this operation might unmask an existing exception that has been detected but not generated, because it was masked. Here, the exception is generated at the completion of the instruction.

**Protected Mode Exceptions**
- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #NM CR0.E[bit 2] or CR0.TS[bit 3] = 1.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- #UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**
- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.
- #NM CR0.E[bit 2] or CR0.TS[bit 3] = 1.
- #UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**
- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #NM CR0.E[bit 2] or CR0.TS[bit 3] = 1.
- #PF(fault-code) If a page fault occurs.
FRSTOR—Restore x87 FPU State

INSTRUCTION SET REFERENCE, A-M

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
FSAVE/FNSAVE—Store x87 FPU State

Description
Stores the current FPU state (operating environment and register stack) at the specified destination in memory, and then re-initializes the FPU. The FSAVE instruction checks for and handles pending unmasked floating-point exceptions before storing the FPU state; the FNSAVE instruction does not.

The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. Figures 8-9 through 8-12 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, show the layout in memory of the stored environment, depending on the operating mode of the processor (protected or real) and the current operand-size attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used. The contents of the FPU register stack are stored in the 80 bytes immediately follow the operating environment image.

The saved image reflects the state of the FPU after all floating-point instructions preceding the FSAVE/FNSAVE instruction in the instruction stream have been executed.

After the FPU state has been saved, the FPU is reset to the same default values it is set to with the FINIT/FNINIT instructions (see "FINIT/FNINIT—Initialize Floating-Point Unit" in this chapter).

The FSAVE/FNSAVE instructions are typically used when the operating system needs to perform a context switch, an exception handler needs to use the FPU, or an application program needs to pass a “clean” FPU to a procedure.

The assembler issues two instructions for the FSAVE instruction (an FWAIT instruction followed by an FNSAVE instruction), and the processor executes each of these

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DD /6</td>
<td>FSAVE m94/108byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU state to m94byte or m108byte after checking for pending unmasked floating-point exceptions. Then re-initialize the FPU.</td>
</tr>
<tr>
<td>DD /6</td>
<td>FNSAVE* m94/108byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU environment to m94byte or m108byte without checking for pending unmasked floating-point exceptions. Then re-initialize the FPU.</td>
</tr>
</tbody>
</table>

NOTES:
* See IA-32 Architecture Compatibility section below.
instructions separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

For Intel math coprocessors and FPUs prior to the Intel Pentium processor, an FWAIT instruction should be executed before attempting to read from the memory image stored with a prior FSAVE/FNSAVE instruction. This FWAIT instruction helps insure that the storage operation has been completed.

When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNSAVE instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled “No-Wait FPU Instructions Can Get FPU Interrupt in Window” in Appendix D of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a description of these circumstances. An FNSAVE instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

**Operation**

(* Save FPU State and Registers *)

DEST[FPUCtrlWord] ← FPUCtrlWord;
DEST[FPUStWord] ← FPUStWord;
DEST[FPUTagWord] ← FPUTagWord;
DEST[FPUDataPointer] ← FPUDataPointer;
DEST[FPUInstrPointer] ← FPUInstrPointer;

DEST[ST(0)] ← ST(0);
DEST[ST(1)] ← ST(1);
DEST[ST(2)] ← ST(2);
DEST[ST(3)] ← ST(3);
DEST[ST(4)] ← ST(4);
DEST[ST(5)] ← ST(5);
DEST[ST(6)] ← ST(6);
DEST[ST(7)] ← ST(7);

(* Initialize FPU *)

FPUCtrlWord ← 037FH;
FPUStWord ← 0;
FPUTagWord ← FFFFH;
FPUDataPointer ← 0;
FPUInstrPointer ← 0;
FPUInstOpCode ← 0;

FSAVE/FNSAVE—Store x87 FPU State
FPU Flags Affected
The C0, C1, C2, and C3 flags are saved and then cleared.

Floating-Point Exceptions
None.

Protected Mode Exceptions
- #GP(0) If destination is located in a non-writable segment.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- #UD If the LOCK prefix is used.

Real-Address Mode Exceptions
- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.
- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made.
- #UD If the LOCK prefix is used.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-
canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory
reference is made while the current privilege level is 3.
FScale—Scale

Description

Truncates the value in the source operand (toward 0) to an integral value and adds that value to the exponent of the destination operand. The destination and source operands are floating-point values located in registers ST(0) and ST(1), respectively. This instruction provides rapid multiplication or division by integral powers of 2. The following table shows the results obtained when scaling various classes of numbers, assuming that neither overflow nor underflow occurs.

Table 3-47. FSCALE Results

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>-•</th>
<th>F</th>
<th>0</th>
<th>+0</th>
<th>+F</th>
<th>+•</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-•</td>
<td>NaN</td>
<td>-•</td>
<td>-•</td>
<td>-•</td>
<td>-•</td>
<td>-•</td>
<td>NaN</td>
</tr>
<tr>
<td>-F</td>
<td>-0</td>
<td>-F</td>
<td>-F</td>
<td>-F</td>
<td>-F</td>
<td>-F</td>
<td>NaN</td>
</tr>
<tr>
<td>-0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:

F Means finite floating-point value.

In most cases, only the exponent is changed and the mantissa (significand) remains unchanged. However, when the value being scaled in ST(0) is a denormal value, the mantissa is also changed and the result may turn out to be a normalized number. Similarly, if overflow or underflow results from a scale operation, the resulting mantissa will differ from the source's mantissa.

The FSCALE instruction can also be used to reverse the action of the FXTRACT instruction, as shown in the following example:

FXTRACT;
FScale;
FSTP ST(1);

In this example, the FXTRACT instruction extracts the significand and exponent from the value in ST(0) and stores them in ST(0) and ST(1) respectively. The FSCALE then scales the significand in ST(0) by the exponent in ST(1), recreating the original value.
before the FXTRACT operation was performed. The FSTP ST(1) instruction overwrites the exponent (extracted by the FXTRACT instruction) with the recreated value, which returns the stack to its original state with only one register [ST(0)] occupied. This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[ ST(0) \leftarrow ST(0) \times 2^{\text{RoundTowardZero(ST(1))}}; \]

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred.
- Set if result was rounded up; cleared otherwise.
- C0, C2, C3 Undefined.

**Floating-Point Exceptions**

- **#IS** Stack underflow occurred.
- **#IA** Source operand is an SNaN value or unsupported format.
- **#D** Source operand is a denormal value.
- **#U** Result is too small for destination format.
- **#O** Result is too large for destination format.
- **#P** Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#MF** If there is a pending x87 FPU exception.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-M

FSIN—Sine

Description
Computes the sine of the source operand in register ST(0) and stores the result in ST(0). The source operand must be given in radians and must be within the range $-2^{63}$ to $+2^{63}$. The following table shows the results obtained when taking the sine of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>SRC (ST(0))</th>
<th>DEST (ST(0))</th>
</tr>
</thead>
<tbody>
<tr>
<td>- • *</td>
<td>*</td>
</tr>
<tr>
<td>- F</td>
<td>- 1 to + 1</td>
</tr>
<tr>
<td>- 0</td>
<td>0</td>
</tr>
<tr>
<td>+ 0</td>
<td>+ 0</td>
</tr>
<tr>
<td>+ F</td>
<td>- 1 to +1</td>
</tr>
<tr>
<td>+ • *</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range $-2^{63}$ to $+2^{63}$ can be reduced to the range of the instruction by subtracting an appropriate integer multiple of $2\pi$ or by using the FPREM instruction with a divisor of $2\pi$. See the section titled "Pi" in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a discussion of the proper value to use for $\pi$ in performing such reductions.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
IF ST(0) < $2^{63}$
    THEN
        C2 ← 0;

FSIN—Sine

ST(0) ← sin(ST(0));
ELSE (* Source operand out of range *)
    C2 ← 1;
FI;

FPU Flags Affected
C1 Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.
C2 Set to 1 if outside range (−2^{63} < source operand < +2^{63}); otherwise, set to 0.
C0, C3 Undefined.

Floating-Point Exceptions
#IS Stack underflow occurred.
#IA Source operand is an SNaN value, ∞, or unsupported format.
#D Source operand is a denormal value.
#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**FSINCOS—Sine and Cosine**

**Description**

 Computes both the sine and the cosine of the source operand in register ST(0), stores the sine in ST(0), and pushes the cosine onto the top of the FPU register stack.

This instruction is faster than executing the FSIN and FCOS instructions in succession.

The source operand must be given in radians and must be within the range $-2^{63}$ to $+2^{63}$. The following table shows the results obtained when taking the sine and cosine of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0)</td>
<td>ST(1) Cosine</td>
</tr>
<tr>
<td>-1 to +1</td>
<td>-1 to +1</td>
</tr>
<tr>
<td>+1</td>
<td>+1</td>
</tr>
<tr>
<td>+0</td>
<td>+1</td>
</tr>
<tr>
<td>+F</td>
<td>+1</td>
</tr>
<tr>
<td>+*</td>
<td>*</td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range $-2^{63}$ to $+2^{63}$ can be reduced to the range of the instruction by subtracting an appropriate integer multiple of $2\pi$ or by using the FPREM instruction with a divisor of $2\pi$. See the section titled "Pi" in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a discussion of the proper value to use for $\pi$ in performing such reductions.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.
Operation

IF ST(0) \( < 2^{63} \)
THEN
  \( C2 \leftarrow 0; \)
  \( \text{TEMP} \leftarrow \cos(\text{ST}(0)); \)
  \( \text{ST}(0) \leftarrow \sin(\text{ST}(0)); \)
  \( \text{TOP} \leftarrow \text{TOP} - 1; \)
  \( \text{ST}(0) \leftarrow \text{TEMP}; \)
ELSE (* Source operand out of range *)
  \( C2 \leftarrow 1; \)
FI;

FPU Flags Affected

\( C1 \) Set to 0 if stack underflow occurred; set to 1 of stack overflow occurs.
Set if result was rounded up; cleared otherwise.
\( C2 \) Set to 1 if outside range \( (-2^{63} < \text{source operand} < +2^{63}) \); otherwise, set to 0.
\( C0, C3 \) Undefined.

Floating-Point Exceptions

\#IS Stack underflow or overflow occurred.
\#IA Source operand is an SNaN value, \( \infty \), or unsupported format.
\#D Source operand is a denormal value.
\#U Result is too small for destination format.
\#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions

\#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
\#MF If there is a pending x87 FPU exception.
\#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FSQRT—Square Root

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 FA</td>
<td>FSQRT</td>
<td>Valid</td>
<td>Valid</td>
<td>Computes square root of ST(0) and stores the result in ST(0).</td>
</tr>
</tbody>
</table>

Description

Computes the square root of the source value in the ST(0) register and stores the result in ST(0).

The following table shows the results obtained when taking the square root of various classes of numbers, assuming that neither overflow nor underflow occurs.

**Table 3-50. FSQRT Results**

<table>
<thead>
<tr>
<th>SRC (ST(0))</th>
<th>DEST (ST(0))</th>
</tr>
</thead>
<tbody>
<tr>
<td>-•</td>
<td>*</td>
</tr>
<tr>
<td>− F</td>
<td>*</td>
</tr>
<tr>
<td>− 0</td>
<td>− 0</td>
</tr>
<tr>
<td>+ 0</td>
<td>+ 0</td>
</tr>
<tr>
<td>+ F</td>
<td>+ F</td>
</tr>
<tr>
<td>+•</td>
<td>+•</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

ST(0) ← SquareRoot(ST(0));

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred.
- Set if result was rounded up; cleared otherwise.
- **C0, C2, C3** Undefined.

**Floating-Point Exceptions**

- **#IS** Stack underflow occurred.
- **#IA** Source operand is an SNaN value or unsupported format.
INSTRUCTION SET REFERENCE, A-M

Source operand is a negative value (except for −0).

#D Source operand is a denormal value.

#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

Same exceptions as in protected mode.
FST/FSTP—Store Floating Point Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compag/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 /2</td>
<td>FST m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m32fp.</td>
</tr>
<tr>
<td>DD /2</td>
<td>FST m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m64fp.</td>
</tr>
<tr>
<td>DD D0+i</td>
<td>FST ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to ST(i).</td>
</tr>
<tr>
<td>D9 /3</td>
<td>FSTP m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m32fp and pop register stack.</td>
</tr>
<tr>
<td>DD /3</td>
<td>FSTP m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m64fp and pop register stack.</td>
</tr>
<tr>
<td>DB /7</td>
<td>FSTP m80fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m80fp and pop register stack.</td>
</tr>
<tr>
<td>DD D8+i</td>
<td>FSTP ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to ST(i) and pop register stack.</td>
</tr>
</tbody>
</table>

Description

The FST instruction copies the value in the ST(0) register to the destination operand, which can be a memory location or another register in the FPU register stack. When storing the value in memory, the value is converted to single-precision or double-precision floating-point format.

The FSTP instruction performs the same operation as the FST instruction and then pops the register stack. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The FSTP instruction can also store values in memory in double extended-precision floating-point format.

If the destination operand is a memory location, the operand specifies the address where the first byte of the destination value is to be stored. If the destination operand is a register, the operand specifies a register in the register stack relative to the top of the stack.

If the destination size is single-precision or double-precision, the significand of the value being stored is rounded to the width of the destination (according to the rounding mode specified by the RC field of the FPU control word), and the exponent is converted to the width and bias of the destination format. If the value being stored is too large for the destination format, a numeric overflow exception (#O) is generated and, if the exception is unmasked, no value is stored in the destination operand. If the value being stored is a denormal value, the denormal exception (#D) is not generated. This condition is simply signaled as a numeric underflow exception (#U) condition.

If the value being stored is ±0, ±∞, or a NaN, the least-significant bits of the significand and the exponent are truncated to fit the destination format. This operation preserves the value’s identity as a 0, ∞, or NaN.
If the destination operand is a non-empty register, the invalid-operation exception is not generated. This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

DEST ← ST(0);

IF Instruction = FSTP
   THEN
      PopRegisterStack;
   FI;

**FPU Flags Affected**

C1 Set to 0 if stack underflow occurred.
Indicates rounding direction of if the floating-point inexact exception (#P) is generated: 0 ← not roundup; 1 ← roundup.
C0, C2, C3 Undefined.

**Floating-Point Exceptions**

#IS Stack underflow occurred.
#IA Source operand is an SNaN value or unsupported format. Does not occur if the source operand is in double extended-precision floating-point format.
#U Result is too small for the destination format.
#O Result is too large for the destination format.
#P Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
**FSTCW/FNSTCW—Store x87 FPU Control Word**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B D9 /7</td>
<td>FSTCW m2byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU control word to m2byte after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>D9 /7</td>
<td>FNSTCW m2byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU control word to m2byte without checking for pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

**NOTES:**
* See IA-32 Architecture Compatibility section below.

**Description**
Stores the current value of the FPU control word at the specified destination in memory. The FSTCW instruction checks for and handles pending unmasked floating-point exceptions before storing the control word; the FNSTCW instruction does not.

The assembler issues two instructions for the FSTCW instruction (an FWAIT instruction followed by an FNSTCW instruction), and the processor executes each of these instructions in separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**
When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNSTCW instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled "No-Wait FPU Instructions Can Get FPU Interrupt in Window” in Appendix D of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a description of these circumstances. An FNSTCW instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

**Operation**

\[ \text{DEST} \leftarrow \text{FPUC}ontrol\text{Word}; \]

**FPU Flags Affected**
The C0, C1, C2, and C3 flags are undefined.

**Floating-Point Exceptions**
None.
Protected Mode Exceptions

#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.
INSTRUCTION SET REFERENCE, A-M

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FSTENV/FNSTENV—Store x87 FPU Environment

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B D9 /6</td>
<td>FSTENV m14/28byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU environment to m14byte or m28byte after checking for pending unmasked floating-point exceptions. Then mask all floating-point exceptions.</td>
</tr>
<tr>
<td>D9 /6</td>
<td>FNSTENV* m14/28byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU environment to m14byte or m28byte without checking for pending unmasked floating-point exceptions. Then mask all floating-point exceptions.</td>
</tr>
</tbody>
</table>

**NOTES:**
* See IA-32 Architecture Compatibility section below.

**Description**

Saves the current FPU operating environment at the memory location specified with the destination operand, and then masks all floating-point exceptions. The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. Figures 8-9 through 8-12 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, show the layout in memory of the stored environment, depending on the operating mode of the processor (protected or real) and the current operand-size attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used.

The FSTENV instruction checks for and handles any pending unmasked floating-point exceptions before storing the FPU environment; the FNSTENV instruction does not. The saved image reflects the state of the FPU after all floating-point instructions preceding the FSTENV/FNSTENV instruction in the instruction stream have been executed.

These instructions are often used by exception handlers because they provide access to the FPU instruction and data pointers. The environment is typically saved in the stack. Masking all exceptions after saving the environment prevents floating-point exceptions from interrupting the exception handler.

The assembler issues two instructions for the FSTENV instruction (an FWAIT instruction followed by an FNSTENV instruction), and the processor executes each of these instructions separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.
IA-32 Architecture Compatibility

When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNSTENV instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled "No-Wait FPU Instructions Can Get FPU Interrupt in Window" in Appendix D of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, for a description of these circumstances. An FNSTENV instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

Operation

\[
\begin{align*}
\text{DEST}[\text{FPUControlWord}] & \leftarrow \text{FPUControlWord}; \\
\text{DEST}[\text{FPUStatusWord}] & \leftarrow \text{FPUStatusWord}; \\
\text{DEST}[\text{FPUTagWord}] & \leftarrow \text{FPUTagWord}; \\
\text{DEST}[\text{FPUDataPointer}] & \leftarrow \text{FPUDataPointer}; \\
\text{DEST}[\text{FPUInstructionPointer}] & \leftarrow \text{FPUInstructionPointer}; \\
\text{DEST}[\text{FPULastInstructionOpcode}] & \leftarrow \text{FPULastInstructionOpcode};
\end{align*}
\]

FPU Flags Affected

The C0, C1, C2, and C3 are undefined.

Floating-Point Exceptions

None.

Protected Mode Exceptions

- **#GP(0)**
  - If the destination is located in a non-writable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.

- **#NM**
  - CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

- **#UD**
  - If the LOCK prefix is used.

Real-Address Mode Exceptions

- **#GP**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FSTSW/FNSTSW—Store x87 FPU Status Word

**Description**

Stores the current value of the x87 FPU status word in the destination location. The destination operand can be either a two-byte memory location or the AX register. The FSTSW instruction checks for and handles pending unmasked floating-point exceptions before storing the status word; the FNSTSW instruction does not.

The FNSTSW AX form of the instruction is used primarily in conditional branching (for instance, after an FPU comparison instruction or an FPREM, FPREM1, or FXAM instruction), where the direction of the branch depends on the state of the FPU condition code flags. (See the section titled "Branching and Conditional Moves on FPU Condition Codes" in Chapter 8 of the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1.*) This instruction can also be used to invoke exception handlers (by examining the exception flags) in environments that do not use interrupts. When the FNSTSW AX instruction is executed, the AX register is updated before the processor executes any further instructions. The status stored in the AX register is thus guaranteed to be from the completion of the prior FPU instruction.

The assembler issues two instructions for the FSTSW instruction (an FWAIT instruction followed by an FNSTSW instruction), and the processor executes each of these instructions separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

### Opcode Instruction 64-Bit Mode Compat/ Leg Mode Description

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DD /7</td>
<td>FSTSW m2byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU status word at m2byte after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>9B DF E0</td>
<td>FSTSW AX</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU status word in AX register after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>DD /7</td>
<td>FNSTSW m2byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU status word at m2byte without checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>DF E0</td>
<td>FNSTSW AX</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU status word in AX register without checking for pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

**NOTES:**

* See IA-32 Architecture Compatibility section below.
IA-32 Architecture Compatibility

When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNSTSW instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled "No-Wait FPU Instructions Can Get FPU Interrupt in Window" in Appendix D of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, for a description of these circumstances. An FNSTSW instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

Operation

DEST ← FPUSstatusWord;

FPU Flags Affected

The C0, C1, C2, and C3 are undefined.

Floating-Point Exceptions

None.

Protected Mode Exceptions

#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
FSUB/FSUBP/FISUB—Subtract

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /4</td>
<td>FSUB m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract m32fp from ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC /4</td>
<td>FSUB m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract m64fp from ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>D8 E0+i</td>
<td>FSUB ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(i) from ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC E8+i</td>
<td>FSUB ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from ST(i) and store result in ST(i).</td>
</tr>
<tr>
<td>DE E8+i</td>
<td>FSUBP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from ST(i), store result in ST(i), and pop register stack.</td>
</tr>
<tr>
<td>DE E9</td>
<td>FSUBP</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from ST(1), store result in ST(1), and pop register stack.</td>
</tr>
<tr>
<td>DA /4</td>
<td>FISUB m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract m32int from ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DE /4</td>
<td>FISUB m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract m16int from ST(0) and store result in ST(0).</td>
</tr>
</tbody>
</table>

Description

Subtracts the source operand from the destination operand and stores the difference in the destination location. The destination operand is always an FPU data register; the source operand can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format or in word or doubleword integer format.

The no-operand version of the instruction subtracts the contents of the ST(0) register from the ST(1) register and stores the result in ST(1). The one-operand version subtracts the contents of a memory location (either a floating-point or an integer value) from the contents of the ST(0) register and stores the result in ST(0). The two-operand version, subtracts the contents of the ST(0) register from the ST(i) register or vice versa.

The FSUBP instructions perform the additional operation of popping the FPU register stack following the subtraction. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point subtract instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FSUB rather than FSUBP.
INSTRUCTION SET REFERENCE, A-M

The FISUB instructions convert an integer source operand to double extended-precision floating-point format before performing the subtraction.

Table 3-51 shows the results obtained when subtracting various classes of numbers from one another, assuming that neither overflow nor underflow occurs. Here, the SRC value is subtracted from the DEST value (DEST − SRC = result).

When the difference between two operands of like sign is 0, the result is +0, except for the round toward −∞ mode, in which case the result is −0. This instruction also guarantees that +0 − (−0) = +0, and that −0 − (+0) = −0. When the source operand is an integer 0, it is treated as a +0.

When one operand is ∞, the result is ∞ of the expected sign. If both operands are ∞ of the same sign, an invalid-operation exception is generated.

<table>
<thead>
<tr>
<th>SRC</th>
<th>-F or -I</th>
<th>-0</th>
<th>+0</th>
<th>+F or +I</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-F</td>
<td>-F</td>
<td>±F or ±0</td>
<td>DEST</td>
<td>DEST</td>
<td>-F</td>
</tr>
<tr>
<td>-0</td>
<td>+F</td>
<td>-SRC</td>
<td>±0</td>
<td>-0</td>
<td>-SRC</td>
</tr>
<tr>
<td>+0</td>
<td>+F</td>
<td>−SRC</td>
<td>+0</td>
<td>±0</td>
<td>−SRC</td>
</tr>
<tr>
<td>+F</td>
<td>+F</td>
<td>DEST</td>
<td>DEST</td>
<td>±F or ±0</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.
I Means integer.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

IF Instruction = FISUB
THEN
    DEST ← DEST − ConvertToDoubleExtendedPrecisionFP(SRC);
ELSE ("Source operand is floating-point value")
    DEST ← DEST − SRC;
FI;
IF Instruction = FSUBP
    THEN
        PopRegisterStack;
FI;

**FPU Flags Affected**

C1  Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.

C0, C2, C3  Undefined.

**Floating-Point Exceptions**

#IS  Stack underflow occurred.

#IA  Operand is a SNaN value or unsupported format.

#D  Source operand is a denormal value.

#U  Result is too small for destination format.

#O  Result is too large for destination format.

#P  Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#GP(0)  If a memory operand effective address is outside the CS, DS,
        ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register is used to access memory and it
        contains a NULL segment selector.

#SS(0)  If a memory operand effective address is outside the SS
        segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP  If a memory operand effective address is outside the CS, DS,
     ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS
     segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD  If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
**Description**

Subtracts the destination operand from the source operand and stores the difference in the destination location. The destination operand is always an FPU register; the source operand can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format or in word or doubleword integer format.

These instructions perform the reverse operations of the FSUB, FSUBP, and FISUB instructions. They are provided to support more efficient coding.

The no-operand version of the instruction subtracts the contents of the ST(1) register from the ST(0) register and stores the result in ST(1). The one-operand version subtracts the contents of the ST(0) register from the contents of a memory location (either a floating-point or an integer value) and stores the result in ST(0). The two-operand version, subtracts the contents of the ST(i) register from the ST(0) register or vice versa.

The FSUBRP instructions perform the additional operation of popping the FPU register stack following the subtraction. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point reverse subtract instructions always results in...
the register stack being popped. In some assemblers, the mnemonic for this instruction is FSUBR rather than FSUBRP.

The FISUBR instructions convert an integer source operand to double extended-precision floating-point format before performing the subtraction.

The following table shows the results obtained when subtracting various classes of numbers from one another, assuming that neither overflow nor underflow occurs. Here, the DEST value is subtracted from the SRC value (SRC − DEST = result).

When the difference between two operands of like sign is 0, the result is +0, except for the round toward −∞ mode, in which case the result is −0. This instruction also guarantees that +0 − (−0) = +0, and that −0 − (+0) = −0. When the source operand is an integer 0, it is treated as a +0.

When one operand is ∞, the result is ∞ of the expected sign. If both operands are ∞ of the same sign, an invalid-operation exception is generated.

Table 3-52. FSUBR/FSUBRP/FISUBR Results

<table>
<thead>
<tr>
<th>DEST</th>
<th>·</th>
<th>−F or −I</th>
<th>−0</th>
<th>+0</th>
<th>+F or +I</th>
<th>·</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−F</td>
<td>·</td>
<td>±F or ±0</td>
<td>−DEST</td>
<td>−DEST</td>
<td>+ F</td>
<td>·</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>·</td>
<td>SRC</td>
<td>±0</td>
<td>+ 0</td>
<td>SRC</td>
<td>±</td>
<td>NaN</td>
</tr>
<tr>
<td>+ 0</td>
<td>·</td>
<td>SRC</td>
<td>−0</td>
<td>±0</td>
<td>SRC</td>
<td>±</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>·</td>
<td>−F</td>
<td>−DEST</td>
<td>−DEST</td>
<td>±F or ±0</td>
<td>·</td>
<td>NaN</td>
</tr>
<tr>
<td>·</td>
<td>·</td>
<td>·</td>
<td>·</td>
<td>·</td>
<td>·</td>
<td>·</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.
I Means integer.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

IF Instruction = FISUBR
    THEN
        DEST ← ConvertToDoubleExtendedPrecisionFP(SRC) − DEST;
    ELSE (* Source operand is floating-point value *)
        DEST ← SRC − DEST; FI;
IF Instruction = FSUBRP
    THEN
        PopRegisterStack; Fl;

**FPU Flags Affected**

C1  Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.

C0, C2, C3  Undefined.

**Floating-Point Exceptions**

#IS  Stack underflow occurred.

#IA  Operand is an SNaN value or unsupported format.
    Operands are infinities of like sign.

#D  Source operand is a denormal value.

#U  Result is too small for destination format.

#O  Result is too large for destination format.

#P  Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD  If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FTST—TEST

Description

Compares the value in the ST(0) register with 0.0 and sets the condition code flags C0, C2, and C3 in the FPU status word according to the results (see table below).

Table 3-53. FTST Results

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; 0.0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; 0.0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = 0.0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

This instruction performs an “unordered comparison.” An unordered comparison also checks the class of the numbers being compared (see “FXAM—Examine ModR/M” in this chapter). If the value in register ST(0) is a NaN or is in an undefined format, the condition flags are set to “unordered” and the invalid operation exception is generated.

The sign of zero is ignored, so that (– 0.0 ← +0.0).

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

CASE (relation of operands) OF
  Not comparable: C3, C2, C0 ← 111;
  ST(0) > 0.0: C3, C2, C0 ← 000;
  ST(0) < 0.0: C3, C2, C0 ← 001;
  ST(0) = 0.0: C3, C2, C0 ← 100;
ESAC;

FPU Flags Affected

C1 Set to 0 if stack underflow occurred; otherwise, set to 0.
C0, C2, C3 See Table 3-53.

Floating-Point Exceptions

#IS Stack underflow occurred.
#IA  The source operand is a NaN value or is in an unsupported format.

#D  The source operand is a denormal value.

Protected Mode Exceptions

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF  If there is a pending x87 FPU exception.

#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

Same exceptions as in protected mode.
**FUCOM/FUCOMP/FUCOMPP—Unordered Compare Floating Point Values**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DD E0+i</td>
<td>FUCOM ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(i).</td>
</tr>
<tr>
<td>DD E1</td>
<td>FUCOM</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(1).</td>
</tr>
<tr>
<td>DD E8+i</td>
<td>FUCOMP ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(i) and pop register stack.</td>
</tr>
<tr>
<td>DD E9</td>
<td>FUCOMP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(1) and pop register stack.</td>
</tr>
<tr>
<td>DA E9</td>
<td>FUCOMPP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(1) and pop register stack twice.</td>
</tr>
</tbody>
</table>

**Description**

Performs an unordered comparison of the contents of register ST(0) and ST(i) and sets condition code flags C0, C2, and C3 in the FPU status word according to the results (see the table below). If no operand is specified, the contents of registers ST(0) and ST(1) are compared. The sign of zero is ignored, so that –0.0 is equal to +0.0.

**Table 3-54. FUCOM/FUCOMP/FUCOMPP Results**

<table>
<thead>
<tr>
<th>Comparison Results*</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST0 &gt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST0 &lt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST0 = ST(i)</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**NOTES:**

* Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.

An unordered comparison checks the class of the numbers being compared (see “FXAM—Examine ModR/M” in this chapter). The FUCOM/FUCOMP/FUCOMPP instructions perform the same operations as the FCOM/FCOMP/FCOMPP instructions. The only difference is that the FUCOM/FUCOMP/FUCOMPP instructions raise the invalid-arithmetic-operand exception (#IA) only when either or both operands are an SNaN or are in an unsupported format; QNaNs cause the condition code flags to be set to unordered, but do not cause an exception to be generated. The FCOM/FCOMP/FCOMPP instructions raise an invalid-operation exception when either or both of the operands are a NaN value of any kind or are in an unsupported format. As with the FCOM/FCOMP/FCOMPP instructions, if the operation results in an invalid-arithmetic-operand exception being raised, the condition code flags are set only if the exception is masked.
The FUCOMP instruction pops the register stack following the comparison operation and the FUCOMPP instruction pops the register stack twice following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

CASE (relation of operands) OF
  - ST > SRC: C3, C2, C0 ← 000;
  - ST < SRC: C3, C2, C0 ← 001;
  - ST = SRC: C3, C2, C0 ← 100;
ESAC;

IF ST(0) or SRC = QNaN, but not SNaN or unsupported format
  THEN
    C3, C2, C0 ← 111;
ELSE (* ST(0) or SRC is SNaN or unsupported format *)
  #IA;
    IF FPUControlWord.IM = 1
       THEN
         C3, C2, C0 ← 111;
    FI;
FI;

IF Instruction = FUCOMP
  THEN
    PopRegisterStack;
FI;

IF Instruction = FUCOMPP
  THEN
    PopRegisterStack;
FI;

**FPU Flags Affected**

C1 Set to 0 if stack underflow occurred.
C0, C2, C3 See Table 3-54.

**Floating-Point Exceptions**

#IS Stack underflow occurred.
FUCOM/FUCOMP/FUCOMP—Unordered Compare Floating Point Values

INSTRUCTION SET REFERENCE, A-M

#IA One or both operands are SNaN values or have unsupported formats. Detection of a QNaN value in and of itself does not raise an invalid-operand exception.

#D One or both operands are denormal values.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FXAM—Examine ModR/M

Description
Examines the contents of the ST(0) register and sets the condition code flags C0, C2, and C3 in the FPU status word to indicate the class of value or number in the register (see the table below).

Table 3-55. FXAM Results

<table>
<thead>
<tr>
<th>Class</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unsupported</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>NaN</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Normal finite number</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Infinity</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Zero</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Empty</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Denormal number</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The C1 flag is set to the sign of the value in ST(0), regardless of whether the register is empty or full.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
C1 ← sign bit of ST; (* 0 for positive, 1 for negative *)

CASE (class of value or number in ST(0)) OF
 Unsupported: C3, C2, C0 ← 000;
 NaN: C3, C2, C0 ← 001;
 Normal: C3, C2, C0 ← 010;
 Infinity: C3, C2, C0 ← 011;
 Zero: C3, C2, C0 ← 100;
 Empty: C3, C2, C0 ← 101;
 Denormal: C3, C2, C0 ← 110;
ESAC;
**FPU Flags Affected**

C1  Sign of value in ST(0).
C0, C2, C3  See Table 3-55.

**Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF  If there is a pending x87 FPU exception.
#UD  If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
**FXCH—Exchange Register Contents**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 C8+i</td>
<td>FXCH ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange the contents of ST(0) and ST(i).</td>
</tr>
<tr>
<td>D9 C9</td>
<td>FXCH</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange the contents of ST(0) and ST(1).</td>
</tr>
</tbody>
</table>

**Description**

Exchanges the contents of registers ST(0) and ST(i). If no source operand is specified, the contents of ST(0) and ST(1) are exchanged.

This instruction provides a simple means of moving values in the FPU register stack to the top of the stack [ST(0)], so that they can be operated on by those floating-point instructions that can only operate on values in ST(0). For example, the following instruction sequence takes the square root of the third register from the top of the register stack:

```
FXCH ST(3);
FSQRT;
FXCH ST(3);
```

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

IF (Number-of-operands) is 1
THEN
  temp ← ST(0);
  ST(0) ← SRC;
  SRC ← temp;
ELSE
  temp ← ST(0);
  ST(0) ← ST(1);
  ST(1) ← temp;
FI;

**FPU Flags Affected**

- C1 Set to 0 if stack underflow occurred; otherwise, set to 1.
- C0, C2, C3 Undefined.

**Floating-Point Exceptions**

- #IS Stack underflow occurred.
Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FXRSTOR—Restore x87 FPU, MMX, XMM, and MXCSR State

**Description**

Reloads the x87 FPU, MMX technology, XMM, and MXCSR registers from the 512-byte memory image specified in the source operand. This data should have been written to memory previously using the FXSAVE instruction, and in the same format as required by the operating modes. The first byte of the data should be located on a 16-byte boundary. There are three distinct layout of the FXSAVE state map: one for legacy and compatibility mode, a second format for 64-bit mode with promoted operand size, and the third format is for 64-bit mode with default operand size. Table 3-56 shows the layout of the legacy/compatibility mode state information in memory and describes the fields in the memory image for the FXRSTOR and FXSAVE instructions. Table 3-59 shows the layout of the 64-bit mode stat information when REX.W is set. Table 3-60 shows the layout of the 64-bit mode stat information when REX.W is clear.

The state image referenced with an FXRSTOR instruction must have been saved using an FXSAVE instruction or be in the same format as required by Table 3-56, Table 3-59, or Table 3-60. Referencing a state image saved with an FSAVE, FNSAVE instruction or incompatible field layout will result in an incorrect state restoration.

The FXRSTOR instruction does not flush pending x87 FPU exceptions. To check and raise exceptions when loading x87 FPU state information with the FXRSTOR instruction, use an FWAIT instruction after the FXRSTOR instruction.

If the OSFXSR bit in control register CR4 is not set, the FXRSTOR instruction may not restore the states of the XMM and MXCSR registers. This behavior is implementation dependent.

If the MXCSR state contains an unmasked exception with a corresponding status flag also set, loading the register with the FXRSTOR instruction will not result in a SIMD floating-point error condition being generated. Only the next occurrence of this unmasked exception will result in the exception being generated.

Bits 16 through 32 of the MXCSR register are defined as reserved and should be set to 0. Attempting to write a 1 in any of these bits from the saved state image will result in a general protection exception (#GP) being generated.

Bytes 464:511 of an FXSAVE image are available for software use. FXRSTOR ignores the content of bytes 464:511 in an FXSAVE state image.
Operation

(x87 FPU, MMX, XMM7-XMM0, MXCSR) ← Load(SRC);

x87 FPU and SIMD Floating-Point Exceptions

None.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment. (See alignment check exception [#AC] below.)
For an attempt to set reserved bits in MXCSR.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
If CR0.EM[bit 2] = 1.
#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
If instruction is preceded by a LOCK prefix.
#AC If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
For an attempt to set reserved bits in MXCSR.
#NM If CR0.TS[bit 3] = 1.
If CR0.EM[bit 2] = 1.
INSTRUCTION SET REFERENCE, A-M

#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
    If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC For unaligned memory reference.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
    If memory operand is not aligned on a 16-byte boundary, regardless of segment.
    For an attempt to set reserved bits in MXCSR.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
    If CR0.EM[bit 2] = 1.
#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
    If instruction is preceded by a LOCK prefix.
#AC If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).
**FXSAVE—Save x87 FPU, MMX Technology, and SSE State**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AE /0</td>
<td>FXSAVE m512byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Save the x87 FPU, MMX, XMM, and MXCSR register state to m512byte.</td>
</tr>
</tbody>
</table>

**Description**

Saves the current state of the x87 FPU, MMX technology, XMM, and MXCSR registers to a 512-byte memory location specified in the destination operand. The content layout of the 512 byte region depends on whether the processor is operating in non-64-bit operating modes or 64-bit sub-mode of IA-32e mode.

Bytes 464:511 are available to software use. The processor does not write to bytes 464:511 of an FXSAVE area.

The operation of FXSAVE in non-64-bit modes is described first.

**Non-64-Bit Mode Operation**

Table 3-56 shows the layout of the state information in memory when the processor is operating in legacy modes.

**Table 3-56. Non-64-bit-Mode Layout of FXSAVE and FXRSTOR Memory Region**

<table>
<thead>
<tr>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 11</th>
<th>Bit 10</th>
<th>Bit 9</th>
<th>Bit 8</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rsvrd</td>
<td>CS</td>
<td>FPU IP</td>
<td>FOP</td>
<td>FTW</td>
<td>FSW</td>
<td>FCW</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MXCSR_Mask</td>
<td>MXCSR</td>
<td>Rsvrd</td>
<td>DS</td>
<td>FPU DP</td>
<td>16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST0/MM0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST1/MM1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST2/MM2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST3/MM3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST4/MM4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST5/MM5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST6/MM6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST7/MM7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| XMM0 | 160 |
| XMM1 | 176 |
| XMM2 | 192 |
The destination operand contains the first byte of the memory image, and it must be aligned on a 16-byte boundary. A misaligned destination operand will result in a general-protection (#GP) exception being generated (or in some cases, an alignment check exception [#AC]).

The FXSAVE instruction is used when an operating system needs to perform a context switch or when an exception handler needs to save and examine the current state of the x87 FPU, MMX technology, and/or XMM and MXCSR registers.

The fields in Table 3-56 are defined in Table 3-57.
Table 3-57. Field Definitions

<table>
<thead>
<tr>
<th>Field</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>FCW</td>
<td>x87 FPU Control Word (16 bits). See Figure 8-6 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for the layout of the x87 FPU control word.</td>
</tr>
<tr>
<td>FSW</td>
<td>x87 FPU Status Word (16 bits). See Figure 8-4 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for the layout of the x87 FPU status word.</td>
</tr>
<tr>
<td>FTW</td>
<td>x87 FPU Tag Word (8 bits). The tag information saved here is abridged, as described in the following paragraphs. See Figure 8-7 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for the layout of the x87 FPU tag word.</td>
</tr>
<tr>
<td>FOP</td>
<td>x87 FPU Opcode (16 bits). The lower 11 bits of this field contain the opcode, upper 5 bits are reserved. See Figure 8-8 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for the layout of the x87 FPU opcode field.</td>
</tr>
<tr>
<td>FPU IP</td>
<td>x87 FPU Instruction Pointer Offset (32 bits). The contents of this field differ depending on the current addressing mode (32-bit or 16-bit) of the processor when the FXSAVE instruction was executed: 32-bit mode — 32-bit IP offset. 16-bit mode — low 16 bits are IP offset; high 16 bits are reserved. See “x87 FPU Instruction and Operand (Data) Pointers” in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a description of the x87 FPU instruction pointer.</td>
</tr>
<tr>
<td>CS</td>
<td>x87 FPU Instruction Pointer Selector (16 bits).</td>
</tr>
<tr>
<td>FPU DP</td>
<td>x87 FPU Instruction Operand (Data) Pointer Offset (32 bits). The contents of this field differ depending on the current addressing mode (32-bit or 16-bit) of the processor when the FXSAVE instruction was executed: 32-bit mode — 32-bit IP offset. 16-bit mode — low 16 bits are IP offset; high 16 bits are reserved. See “x87 FPU Instruction and Operand (Data) Pointers” in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a description of the x87 FPU operand pointer.</td>
</tr>
<tr>
<td>DS</td>
<td>x87 FPU Instruction Operand (Data) Pointer Selector (16 bits).</td>
</tr>
</tbody>
</table>
The FXSAVE instruction saves an abridged version of the x87 FPU tag word in the FTW field (unlike the FSAVE instruction, which saves the complete tag word). The tag information is saved in physical register order (R0 through R7), rather than in top-of-stack (TOS) order. With the FXSAVE instruction, however, only a single bit (1 for valid or 0 for empty) is saved for each tag. For example, assume that the tag word is currently set as follows:

R7  R6  R5  R4  R3  R2  R1  R0
11  xx  xx  xx  11  11  11  11

Here, 11B indicates empty stack elements and “xx” indicates valid (00B), zero (01B), or special (10B).

For this example, the FXSAVE instruction saves only the following 8 bits of information:

R7  R6  R5  R4  R3  R2  R1  R0
0  1  1  1  0  0  0  0

<table>
<thead>
<tr>
<th>Field</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>MXCSR</td>
<td>MXCSR Register State (32 bits). See Figure 10-3 in the <em>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1</em>, for the layout of the MXCSR register. If the OSFXSR bit in control register CR4 is not set, the FXSAVE instruction may not save this register. This behavior is implementation dependent.</td>
</tr>
<tr>
<td>MXCSR_MASK</td>
<td>MXCSR_MASK (32 bits). This mask can be used to adjust values written to the MXCSR register, ensuring that reserved bits are set to 0. Set the mask bits and flags in MXCSR to the mode of operation desired for SSE and SSE2 SIMD floating-point instructions. See “Guidelines for Writing to the MXCSR Register” in Chapter 11 of the <em>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1</em>, for instructions for how to determine and use the MXCSR_MASK value.</td>
</tr>
<tr>
<td>ST0/MM0 through ST7/MM7</td>
<td>x87 FPU or MMX technology registers. These 80-bit fields contain the x87 FPU data registers or the MMX technology registers, depending on the state of the processor prior to the execution of the FXSAVE instruction. If the processor had been executing x87 FPU instruction prior to the FXSAVE instruction, the x87 FPU data registers are saved; if it had been executing MMX instructions (or SSE or SSE2 instructions that operated on the MMX technology registers), the MMX technology registers are saved. When the MMX technology registers are saved, the high 16 bits of the field are reserved.</td>
</tr>
<tr>
<td>XMM0 through XMM7</td>
<td>XMM registers (128 bits per field). If the OSFXSR bit in control register CR4 is not set, the FXSAVE instruction may not save these registers. This behavior is implementation dependent.</td>
</tr>
</tbody>
</table>
Here, a 1 is saved for any valid, zero, or special tag, and a 0 is saved for any empty tag.

The operation of the FXSAVE instruction differs from that of the FSAVE instruction, as follows:

- FXSAVE instruction does not check for pending unmasked floating-point exceptions. (The FXSAVE operation in this regard is similar to the operation of the FNSAVE instruction).
- After the FXSAVE instruction has saved the state of the x87 FPU, MMX technology, XMM, and MXCSR registers, the processor retains the contents of the registers. Because of this behavior, the FXSAVE instruction cannot be used by an application program to pass a "clean" x87 FPU state to a procedure, since it retains the current state. To clean the x87 FPU state, an application must explicitly execute an FINIT instruction after an FXSAVE instruction to reinitialize the x87 FPU state.
- The format of the memory image saved with the FXSAVE instruction is the same regardless of the current addressing mode (32-bit or 16-bit) and operating mode (protected, real address, or system management). This behavior differs from the FSAVE instructions, where the memory image format is different depending on the addressing mode and operating mode. Because of the different image formats, the memory image saved with the FXSAVE instruction cannot be restored correctly with the FRSTOR instruction, and likewise the state saved with the FSAVE instruction cannot be restored correctly with the FXRSTOR instruction.

The FSAVE format for FTW can be recreated from the FTW valid bits and the stored 80-bit FP data (assuming the stored data was not the contents of MMX technology registers) using Table 3-58.

### Table 3-58. Recreating FSAVE Format

<table>
<thead>
<tr>
<th>Exponent all 1’s</th>
<th>Exponent all 0’s</th>
<th>Fraction all 0’s</th>
<th>J and M bits</th>
<th>FTW valid bit</th>
<th>x87 FTW</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1x</td>
<td>1</td>
<td>Valid 00</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>00</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>10</td>
<td>1</td>
<td>Valid 00</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0x</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1x</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>00</td>
<td>1</td>
<td>Zero 01</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>10</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1x</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1x</td>
<td>1</td>
<td>Special 10</td>
</tr>
</tbody>
</table>
The J-bit is defined to be the 1-bit binary integer to the left of the decimal place in the significand. The M-bit is defined to be the most significant bit of the fractional portion of the significand (i.e., the bit immediately to the right of the decimal place).

When the M-bit is the most significant bit of the fractional portion of the significand, it must be 0 if the fraction is all 0's.

IA-32e Mode Operation

In compatibility sub-mode of IA-32e mode, legacy SSE registers, XMM0 through XMM7, are saved according to the legacy FXSAVE map. In 64-bit mode, all of the SSE registers, XMM0 through XMM15, are saved. But the layout of the 64-bit FXSAVE map has two flavors, depending on the value of the REX.W bit. The difference of these two flavors is in the FPU IP and FPU DP pointers. When REX.W = 0, the FPU IP is saved as CS with the 32 bit IP, and the FPU DP is saved as DS with the 32 bit DP. When REX.W = 1, the FPU IP and FPU DP are both 64 bit values without and segment selectors.

The IA-32e mode save formats are shown in Table 3-59 and Table 3-60 listed below.

Table 3-58. Recreating FSAVE Format (Contd.)

<table>
<thead>
<tr>
<th>Exponent all 1's</th>
<th>Exponent all 0's</th>
<th>Fraction all 0's</th>
<th>J and M bits</th>
<th>FTW valid bit</th>
<th>x87 FTW</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>00</td>
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For all legal combinations above.

Table 3-59. Layout of the 64-bit-mode FXSAVE Map with Promoted OperandSize

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### Table 3-60. Layout of the 64-bit-mode FXSAVE Map with Default OperandSize

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### Table 3-60. Layout of the 64-bit-mode FXSAVE Map with Default OperandSize (Contd.)

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**Operation**

IF 64-Bit Mode

THEN

IF REX.W = 1
THEN
   DEST ← Save64BitPromotedFxsave(x87 FPU, MMX, XMM7-XMM0, MXCSR);
ELSE
   DEST ← Save64BitDefaultFxsave(x87 FPU, MMX, XMM7-XMM0, MXCSR);
FI;
ELSE
   DEST ← SaveLegacyFxsave(x87 FPU, MMX, XMM7-XMM0, MXCSR);
FI;

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
   If a memory operand is not aligned on a 16-byte boundary, regardless of segment. (See the description of the alignment check exception [#AC] below.)
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
   If CR0.EM[bit 2] = 1.
#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
   If the LOCK prefix is used.
#AC If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
   If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
INSTRUCTION SET REFERENCE, A-M

If CR0.EM[bit 2] = 1.

#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC For unaligned memory reference.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
If CR0.EM[bit 2] = 1.
#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
If the LOCK prefix is used.

#AC If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).
Implementation Note

The order in which the processor signals general-protection (#GP) and page-fault (#PF) exceptions when they both occur on an instruction boundary is given in Table 5-2 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*. This order vary for FXSAVE for different processor implementations.
FXTRACT—Extract Exponent and Significand

### Description
Separates the source value in the ST(0) register into its exponent and significand, stores the exponent in ST(0), and pushes the significand onto the register stack. Following this operation, the new top-of-stack register ST(0) contains the value of the original significand expressed as a floating-point value. The sign and significand of this value are the same as those found in the source operand, and the exponent is 3FFFH (biased value for a true exponent of zero). The ST(1) register contains the value of the original operand's true (unbiased) exponent expressed as a floating-point value. (The operation performed by this instruction is a superset of the IEEE-recommended \( \log_b(x) \) function.)

This instruction and the F2XM1 instruction are useful for performing power and range scaling operations. The FXTRACT instruction is also useful for converting numbers in double extended-precision floating-point format to decimal representations (e.g., for printing or displaying).

If the floating-point zero-divide exception (#Z) is masked and the source operand is zero, an exponent value of \(-\infty\) is stored in register ST(1) and 0 with the sign of the source operand is stored in register ST(0).

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

### Operation
\[
\begin{align*}
\text{TEMP} & \leftarrow \text{Significand(ST(0))}; \\
\text{ST(0)} & \leftarrow \text{Exponent(ST(0))}; \\
\text{TOP} & \leftarrow \text{TOP} - 1; \\
\text{ST(0)} & \leftarrow \text{TEMP};
\end{align*}
\]

### FPU Flags Affected
- \( C1 \): Set to 0 if stack underflow occurred; set to 1 if stack overflow occurred.
- \( C0, C2, C3 \): Undefined.

### Floating-Point Exceptions
- \#IS: Stack underflow or overflow occurred.
#IA Source operand is an SNaN value or unsupported format.
#Z ST(0) operand is ±0.
#D Source operand is a denormal value.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**FYL2X—Compute y * log₂x**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F1</td>
<td>FYL2X</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(1) with (ST(1) * log₂ST(0)) and pop the register stack.</td>
</tr>
</tbody>
</table>

**Description**

Computes \((ST(1) \times \log₂(ST(0)))\), stores the result in register ST(1), and pops the FPU register stack. The source operand in ST(0) must be a non-zero positive number.

The following table shows the results obtained when taking the log of various classes of numbers, assuming that neither overflow nor underflow occurs.

*Table 3-61. FYL2X Results*

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>-·</th>
<th>−F</th>
<th>±0</th>
<th>+0&lt;+F&lt;+1</th>
<th>+1</th>
<th>+F&gt;+1</th>
<th>++</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-·</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>+F</td>
<td>−0</td>
<td>−F</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>+0</td>
<td>−0</td>
<td>−0</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>−0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>−F</td>
<td>+0</td>
<td>+F</td>
<td>++</td>
<td>NaN</td>
</tr>
<tr>
<td>++</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>−·</td>
<td>−·</td>
<td>*</td>
<td>++</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.
* Indicates floating-point invalid-operation (#IA) exception.
** Indicates floating-point zero-divide (#Z) exception.

If the divide-by-zero exception is masked and register ST(0) contains ±0, the instruction returns \(\infty\) with a sign that is the opposite of the sign of the source operand in register ST(1).

The FYL2X instruction is designed with a built-in multiplication to optimize the calculation of logarithms with an arbitrary positive base (b):

\[
\log_b x \leftarrow (\log_2 b)^{-1} \times \log_2 x
\]

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.
Operation

ST(1) ← ST(1) * log2ST(0);
PopRegisterStack;

FPU Flags Affected

C1 Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.
C0, C2, C3 Undefined.

Floating-Point Exceptions

#IS Stack underflow occurred.
#IA Either operand is an SNaN or unsupported format.
    Source operand in register ST(0) is a negative finite value
    (not -0).
#Z Source operand in register ST(0) is ±0.
#D Source operand is a denormal value.
#U Result is too small for destination format.
#O Result is too large for destination format.
#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

Same exceptions as in protected mode.
**FYL2XP1—Compute \( y \times \log_2(x + 1) \)**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F9</td>
<td>FYL2XP1</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(1) with ( ST(1) \times \log_2(ST(0) + 1.0) ) and pop the register stack.</td>
</tr>
</tbody>
</table>

**Description**

Computes \( ST(1) \times \log_2(ST(0) + 1.0) \), stores the result in register ST(1), and pops the FPU register stack. The source operand in ST(0) must be in the range:

\[-(1 - \sqrt{2}/2) \text{ to } (1 - \sqrt{2}/2)\]

The source operand in ST(1) can range from \(-\infty\) to \(\infty\). If the ST(0) operand is outside of its acceptable range, the result is undefined and software should not rely on an exception being generated. Under some circumstances exceptions may be generated when ST(0) is out of range, but this behavior is implementation specific and not guaranteed.

The following table shows the results obtained when taking the log epsilon of various classes of numbers, assuming that underflow does not occur.

**Table 3-62. FYL2XP1 Results**

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>( -(1 - (\sqrt{2}/2)) ) to (-0)</th>
<th>(-0)</th>
<th>(+0)</th>
<th>(+0) to (+(1 - (\sqrt{2}/2)))</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>(-)F</td>
<td>(+)F</td>
<td>(*)</td>
<td>(*)</td>
<td>(-)F</td>
<td>NaN</td>
</tr>
<tr>
<td>(-0)</td>
<td>(+0)</td>
<td>(-0)</td>
<td>(-0)</td>
<td>(-0)</td>
<td>NaN</td>
</tr>
<tr>
<td>(+0)</td>
<td>(-0)</td>
<td>(+0)</td>
<td>(+0)</td>
<td>(+0)</td>
<td>NaN</td>
</tr>
<tr>
<td>(+F)</td>
<td>(-F)</td>
<td>(-0)</td>
<td>(+0)</td>
<td>(+F)</td>
<td>NaN</td>
</tr>
<tr>
<td>(+)</td>
<td>(-)</td>
<td>(*)</td>
<td>(*)</td>
<td>(+)</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

- F Means finite floating-point value.
- * Indicates floating-point invalid-operation (#IA) exception.

This instruction provides optimal accuracy for values of epsilon [the value in register ST(0)] that are close to 0. For small epsilon (\(\varepsilon\)) values, more significant digits can be retained by using the FYL2XP1 instruction than by using \((\varepsilon+1)\) as an argument to the FYL2X instruction. The \((\varepsilon+1)\) expression is commonly found in compound interest and annuity calculations. The result can be simply converted into a value in another logarithm base by including a scale factor in the ST(1) source operand. The following
equation is used to calculate the scale factor for a particular logarithm base, where \( n \) is the logarithm base desired for the result of the FYL2XP1 instruction:

\[
\text{scale factor} \leftarrow \log_2 n
\]

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\text{ST}(1) \leftarrow \text{ST}(1) \times \log_2 (\text{ST}(0) + 1.0);
\]

PopRegisterStack;

**FPU Flags Affected**

- \( \text{C1} \) Set to 0 if stack underflow occurred.
- Set if result was rounded up; cleared otherwise.
- \( \text{C0}, \text{C2}, \text{C3} \) Undefined.

**Floating-Point Exceptions**

- #IS Stack underflow occurred.
- #IA Either operand is an SNaN value or unsupported format.
- #D Source operand is a denormal value.
- #U Result is too small for destination format.
- #O Result is too large for destination format.
- #P Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #MF If there is a pending x87 FPU exception.
- #UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
HADDPD—Packed Double-FP Horizontal Add

** Opcode Instruction 64-Bit Mode Compat/ Leg Mode Description **

| 66 0F 7C | HADDPD xmm1, xmm2/m128 | Valid | Valid | Horizontal add packed double-precision floating-point values from xmm2/m128 to xmm1. |

**Description**

Adds the double-precision floating-point values in the high and low quadwords of the destination operand and stores the result in the low quadword of the destination operand.

Adds the double-precision floating-point values in the high and low quadwords of the source operand and stores the result in the high quadword of the destination operand. See Figure 3-11.

![Figure 3-11. HADDPD—Packed Double-FP Horizontal Add](image)

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
HADDPD—Packed Double-FP Horizontal Add

**Operation**

\[
\begin{align*}
\text{xmm1}[63:0] &= \text{xmm1}[63:0] + \text{xmm1}[127:64]; \\
\text{xmm1}[127:64] &= \text{xmm2/m128}[63:0] + \text{xmm2/m128}[127:64];
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

\[
\text{HADDPD} \quad __m128d \_mm_hadd\_pd(__m128d \text{a}, __m128d \text{b})
\]

**Exceptions**

When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

**Numeric Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#XM For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).

#UD If CR0.EM[bit 2] = 1.

For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:ECX.SSE3[bit 0] = 0.

If the LOCK prefix is used.

**Real Address Mode Exceptions**

GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.

If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM If CR0.TS[bit 3] = 1.

#XM For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).
**INSTRUCTION SET REFERENCE, A-M**

#UD If CR0.EM[bit 2] = 1.
   For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
   If CR4.OSFXSR[bit 9] = 0.
   If CPUsID.01H:ECX.SSE3[bit 0] = 0.
   If the LOCK prefix is used.

**Virtual 8086 Mode Exceptions**

GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
   If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM If CR0.TS[bit 3] = 1.
#XM For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).
#UD If CR0.EM[bit 2] = 1.
   For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
   If CR4.OSFXSR[bit 9] = 0.
   If CPUsID.01H:ECX.SSE3[bit 0] = 0.
   If the LOCK prefix is used.

#PF(fault-code) For a page fault.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
   If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD

If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID feature flag SSE3 is 0.
If the LOCK prefix is used.
HADDPS—Packed Single-FP Horizontal Add

Description

Adds the single-precision floating-point values in the first and second dwords of the destination operand and stores the result in the first dword of the destination operand.

Adds single-precision floating-point values in the third and fourth dword of the destination operand and stores the result in the second dword of the destination operand.

Adds single-precision floating-point values in the first and second dword of the source operand and stores the result in the third dword of the destination operand.

Adds single-precision floating-point values in the third and fourth dword of the source operand and stores the result in the fourth dword of the destination operand. See Figure 3-12.

Figure 3-12. HADDPS—Packed Single-FP Horizontal Add
In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\begin{align*}
\text{xmm1}[31:0] &= \text{xmm1}[31:0] + \text{xmm1}[63:32]; \\
\text{xmm1}[63:32] &= \text{xmm1}[95:64] + \text{xmm1}[127:96]; \\
\text{xmm1}[95:64] &= \text{xmm2/m128}[31:0] + \text{xmm2/m128}[63:32]; \\
\text{xmm1}[127:96] &= \text{xmm2/m128}[95:64] + \text{xmm2/m128}[127:96];
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

`HADDPS __m128 _mm_hadd_ps(__m128 a, __m128 b)`

**Exceptions**

When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

**Numeric Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions**

- **#GP(0)**: For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
  - If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
- **#SS(0)**: For an illegal address in the SS segment.
- **#PF(fault-code)**: For a page fault.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#XM**: For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).
- **#UD**: If CR0.EM[bit 2] = 1.
  - For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:ECX.SSE3[bit 0] = 0.
  - If the LOCK prefix is used.
Real Address Mode Exceptions

GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM If CR0.TS[bit 3] = 1.

#XM For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).

#UD If CR0.EM[bit 2] = 1.
For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.

Virtual 8086 Mode Exceptions

GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM If CR0.TS[bit 3] = 1.

#XM For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).

#UD If CR0.EM[bit 2] = 1.
For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID feature flag SSE3 is 0.
   If the LOCK prefix is used.
HLT—Halt

Description

Stops instruction execution and places the processor in a HALT state. An enabled interrupt (including NMI and SMI), a debug exception, the BINIT# signal, the INIT# signal, or the RESET# signal will resume execution. If an interrupt (including NMI) is used to resume execution after a HLT instruction, the saved instruction pointer (CS:EIP) points to the instruction following the HLT instruction.

When a HLT instruction is executed on an Intel 64 or IA-32 processor supporting Intel Hyper-Threading Technology, only the logical processor that executes the instruction is halted. The other logical processors in the physical processor remain active, unless they are each individually halted by executing a HLT instruction.

The HLT instruction is a privileged instruction. When the processor is running in protected or virtual-8086 mode, the privilege level of a program or procedure must be 0 to execute the HLT instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

Enter Halt state;

Flags Affected

None.

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

None.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.
Compatibly Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
HSUBPD—Packed Double-FP Horizontal Subtract

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 7D /r</td>
<td>HSUBPD xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Horizontal subtract packed double-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
</tbody>
</table>

Description

The HSUBPD instruction subtracts horizontally the packed DP FP numbers of both operands.

Subtracts the double-precision floating-point value in the high quadword of the destination operand from the low quadword of the destination operand and stores the result in the low quadword of the destination operand.

Subtracts the double-precision floating-point value in the high quadword of the source operand from the low quadword of the source operand and stores the result in the high quadword of the destination operand. See Figure 3-13.

![Figure 3-13. HSUBPD—Packed Double-FP Horizontal Subtract](image)

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
HSUBPD—Packed Double-FP Horizontal Subtract

**Operation**

\[
\begin{align*}
\text{ xmm1}[63:0] &= \text{ xmm1}[63:0] - \text{ xmm1}[127:64]; \\
\text{ xmm1}[127:64] &= \text{ xmm2/m128}[63:0] - \text{ xmm2/m128}[127:64];
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

HشورPD __m128d _mm_hsub_pd(__m128d a, __m128d b)

**Exceptions**

When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

**Numeric Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
  - If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
- **#SS(0)** For an illegal address in the SS segment.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
- **#XM** For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).
- **#UD** If CR0.EM[bit 2] = 1.
  - For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:ECX.SSE3[bit 0] = 0.
  - If the LOCK prefix is used.

**Real Address Mode Exceptions**

- **GP(0)** If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
  - If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
- **#NM** If CR0.TS[bit 3] = 1.
- **#XM** For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).
INSTRUCTION SET REFERENCE, A-M

#UD    If CR0.EM[bit 2] = 1.
          For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
          If CR4.OSFXSR[bit 9] = 0.
          If CPUID.01H:ECX.SSE3[bit 0] = 0.
          If the LOCK prefix is used.

Virtual 8086 Mode Exceptions
GP(0)    If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
          If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#NM     If CR0.TS[bit 3] = 1.
#XM     For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).
#UD     If CR0.EM[bit 2] = 1.
          For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
          If CR4.OSFXSR[bit 9] = 0.
          If CPUID.01H:ECX.SSE3[bit 0] = 0.
          If the LOCK prefix is used.
#PF(fault-code)  For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)     If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)     If the memory address is in a non-canonical form.
          If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code)  For a page fault.
#NM     If CR0.TS[bit 3] = 1.
#XM     If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD     If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
          If CR0.EM[bit 2] = 1.
          If CR4.OSFXSR[bit 9] = 0.
If CPUID feature flag SSE3 is 0.
If the LOCK prefix is used.
HSUBPS—Packed Single-FP Horizontal Subtract

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 7D /r</td>
<td>HSUBPS xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Horizontal subtract packed single-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Subtracts the single-precision floating-point value in the second dword of the destination operand from the first dword of the destination operand and stores the result in the first dword of the destination operand.

Subtracts the single-precision floating-point value in the fourth dword of the destination operand from the third dword of the destination operand and stores the result in the second dword of the destination operand.

Subtracts the single-precision floating-point value in the second dword of the source operand from the first dword of the source operand and stores the result in the third dword of the destination operand.

Subtracts the single-precision floating-point value in the fourth dword of the source operand from the third dword of the source operand and stores the result in the fourth dword of the destination operand.

See Figure 3-14.
In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\begin{align*}
\text{xmm1}[31:0] &= \text{xmm1}[31:0] - \text{xmm1}[63:32]; \\
\text{xmm1}[63:32] &= \text{xmm1}[95:64] - \text{xmm1}[127:96]; \\
\text{xmm1}[95:64] &= \text{xmm2/m128}[31:0] - \text{xmm2/m128}[63:32]; \\
\text{xmm1}[127:96] &= \text{xmm2/m128}[95:64] - \text{xmm2/m128}[127:96];
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

```
HSUBPS  _m128 _mm_hsub_ps(_m128 a, _m128 b)
```

**Exceptions**

When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.
Numeric Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).
#UD If CR0.EM[bit 2] = 1.
For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.

Real Address Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#NM If CR0.TS[bit 3] = 1.
#XM For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).
#UD If CR0.EM[bit 2] = 1.
For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.

Virtual 8086 Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
INSTRUCTION SET REFERENCE, A-M

HSUBPS—Packed Single-FP Horizontal Subtract

#NM If CR0.TS[bit 3] = 1.

#XM For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 1).

#UD If CR0.EM[bit 2] = 1.
   For an unmasked Streaming SIMD Extensions numeric exception (CR4.OSXMMEXCPT[bit 10] = 0).
   If CR4.OSFXSR[bit 9] = 0.
   If the LOCK prefix is used.
   If CPUID.01H:ECX.SSE3[bit 0] = 0.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.
   If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.

#UD If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:ECX.SSE3[bit 0] = 0.
   If the LOCK prefix is used.
IDIV—Signed Divide

**Description**

Divides the (signed) value in the AX, DX:AX, or EDX:EAX (dividend) by the source operand (divisor) and stores the result in the AX (AH:AL), DX:AX, or EDX:EAX registers. The source operand can be a general-purpose register or a memory location. The action of this instruction depends on the operand size (dividend/divisor).

Non-integral results are truncated (chopped) towards 0. The remainder is always less than the divisor in magnitude. Overflow is indicated with the #DE (divide error) exception rather than with the CF flag.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. In 64-bit mode when REX.W is applied, the instruction divides the signed value in RDX:RAX by the source operand. RAX contains a 64-bit quotient; RDX contains a 64-bit remainder.

See the summary chart at the beginning of this section for encoding data and limits. See Table 3-63.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction 64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /7</td>
<td>IDIV r/m8</td>
<td>Valid</td>
<td>Signed divide AX by r/m8, with result stored in: AL ← Quotient, AH ← Remainder.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REX + F6 /7</td>
<td>IDIV r/m8*</td>
<td>Valid</td>
<td>Signed divide AX by r/m8, with result stored in AL ← Quotient, AH ← Remainder.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F7 /7</td>
<td>IDIV r/m16</td>
<td>Valid</td>
<td>Signed divide DX:AX by r/m16, with result stored in AX ← Quotient, DX ← Remainder.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F7 /7</td>
<td>IDIV r/m32</td>
<td>Valid</td>
<td>Signed divide EDX:EAX by r/m32, with result stored in EAX ← Quotient, EDX ← Remainder.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REX.W + F7 /7</td>
<td>IDIV r/m64</td>
<td>Valid</td>
<td>Signed divide RDX:RAX by r/m64, with result stored in RAX ← Quotient, RDX ← Remainder.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
IDIV—Signed Divide

Table 3-63. IDIV Results

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Dividend</th>
<th>Divisor</th>
<th>Quotient</th>
<th>Remainder</th>
<th>Quotient Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Word/byte</td>
<td>AX</td>
<td>r/m8</td>
<td>AL</td>
<td>AH</td>
<td>-128 to +127</td>
</tr>
<tr>
<td>Doubleword/word</td>
<td>DX:AX</td>
<td>r/m16</td>
<td>AX</td>
<td>DX</td>
<td>-32,768 to +32,767</td>
</tr>
<tr>
<td>Quadword/doubleword</td>
<td>EDX:EAX</td>
<td>r/m32</td>
<td>EAX</td>
<td>EDX</td>
<td>$-2^{31}$ to $2^{32} - 1$</td>
</tr>
<tr>
<td>Doublequadword/quadword</td>
<td>RDX:RAX</td>
<td>r/m64</td>
<td>RAX</td>
<td>RDX</td>
<td>$-2^{63}$ to $2^{64} - 1$</td>
</tr>
</tbody>
</table>

Operation

IF SRC = 0
THEN #DE; (* Divide error *)
FI;

IF OperandSize = 8 (* Word/byte operation *)
THEN
  temp ← AX / SRC; (* Signed division *)
  IF (temp > 7FH) or (temp < 80H)
  (* If a positive result is greater than 7FH or a negative result is less than 80H *)
  THEN #DE; (* Divide error *)
  ELSE
    AL ← temp;
    AH ← AX SignedModulus SRC;
  FI;
ELSE IF OperandSize = 16 (* Doubleword/word operation *)
THEN
  temp ← DX:AX / SRC; (* Signed division *)
  IF (temp > 7FFFH) or (temp < 8000H)
  (* If a positive result is greater than 7FFFH or a negative result is less than 8000H *)
  THEN
    #DE; (* Divide error *)
  ELSE
    AX ← temp;
    DX ← DX:AX SignedModulus SRC;
  FI;
ELSE IF OperandSize = 32 (* Quadword/doubleword operation *)
  temp ← EDX:EAX / SRC; (* Signed division *)
  IF (temp > 7FFFFFFFH) or (temp < 80000000H)
  (* If a positive result is greater than 7FFFFFFFH *)
or a negative result is less than 8000000000000000H *)
THEN
  #DE; (* Divide error *)
ELSE
  EAX ← temp;
  EDX ← EDX:AX SignedModulus SRC;
FI;
ELSE IF OperandSize = 64 (* Doublequadword/quadword operation *)
  temp ← RDX:RAX / SRC; (* Signed division *)
  IF (temp > 7FFFFFFFFFFFFFFFH) or (temp < 8000000000000000H)
  (* If a positive result is greater than 7FFFFFFFFFFFFFFFH
  or a negative result is less than 8000000000000000H *)
  THEN
    #DE; (* Divide error *)
  ELSE
    RAX ← temp;
    RDX ← RDX:RAX SignedModulus SRC;
  FI;
FI;
FI;
FI;
FI;

**Flags Affected**
The CF, OF, SF, ZF, AF, and PF flags are undefined.

**Protected Mode Exceptions**
#DE If the source operand (divisor) is 0.
The signed result (quotient) is too large for the destination.
#GP(0) If a memory operand effective address is outside the CS, DS, 
ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it 
contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS 
segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory 
reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
Real-Address Mode Exceptions

#DE  If the source operand (divisor) is 0.
      The signed result (quotient) is too large for the destination.
#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
#UD  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#DE  If the source operand (divisor) is 0.
      The signed result (quotient) is too large for the destination.
#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
#UD  If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#DE  If the source operand (divisor) is 0
      If the quotient is too large for the designated register.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.
## IMUL—Signed Multiply

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /5</td>
<td>IMUL r/m8*</td>
<td>Valid</td>
<td>Valid</td>
<td>AX ← AL ∗ r/m byte.</td>
</tr>
<tr>
<td>F7 /5</td>
<td>IMUL r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>DX:AX ← AX ∗ r/m word.</td>
</tr>
<tr>
<td>F7 /5</td>
<td>IMUL r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>EDX:EAX ← EAX ∗ r/m32.</td>
</tr>
<tr>
<td>REX.W + F7 /5</td>
<td>IMUL r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>RDX:RAX ← RAX ∗ r/m64.</td>
</tr>
<tr>
<td>0F AF /r</td>
<td>IMUL r16, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>word register ← word register ∗ r/m16.</td>
</tr>
<tr>
<td>0F AF /r</td>
<td>IMUL r32, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>doubleword register ← doubleword register ∗ r/m32.</td>
</tr>
<tr>
<td>REX.W + 0F AF /r</td>
<td>IMUL r64, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Quadword register ← Quadword register ∗ r/m64.</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r16, r/m16, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>word register ← r/m16 ∗ sign-extended immediate byte.</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r32, r/m32, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>doubleword register ← r/m32 ∗ sign-extended immediate byte.</td>
</tr>
<tr>
<td>REX.W + 6B /r ib</td>
<td>IMUL r64, r/m64, imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Quadword register ← r/m64 ∗ sign-extended immediate byte.</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r16, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>word register ← word register ∗ sign-extended immediate byte.</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r32, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>doubleword register ← doubleword register ∗ sign-extended immediate byte.</td>
</tr>
<tr>
<td>REX.W + 6B /r ib</td>
<td>IMUL r64, imm8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Quadword register ← Quadword register ∗ sign-extended immediate byte.</td>
</tr>
<tr>
<td>69 /r iw</td>
<td>IMUL r16, r/m16, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>word register ← r/m16 ∗ immediate word.</td>
</tr>
<tr>
<td>69 /r id</td>
<td>IMUL r32, r/m32, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>doubleword register ← r/m32 ∗ immediate doubleword.</td>
</tr>
<tr>
<td>REX.W + 69 /r id</td>
<td>IMUL r64, r/m64, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Quadword register ← r/m64 ∗ immediate doubleword.</td>
</tr>
<tr>
<td>69 /r iw</td>
<td>IMUL r16, imm16</td>
<td>Valid</td>
<td>Valid</td>
<td>word register ← r/m16 ∗ immediate word.</td>
</tr>
</tbody>
</table>
IMUL—Signed Multiply

### Description

Performs a signed multiplication of two operands. This instruction has three forms, depending on the number of operands.

- **One-operand form** — This form is identical to that used by the MUL instruction. Here, the source operand (in a general-purpose register or memory location) is multiplied by the value in the AL, AX, EAX, or RAX register (depending on the operand size) and the product is stored in the AX, DX:AX, EDX:EAX, or RDX:RAX registers, respectively.

- **Two-operand form** — With this form the destination operand (the first operand) is multiplied by the source operand (second operand). The destination operand is a general-purpose register and the source operand is an immediate value, a general-purpose register, or a memory location. The product is then stored in the destination operand location.

- **Three-operand form** — This form requires a destination operand (the first operand) and two source operands (the second and the third operands). Here, the first source operand (which can be a general-purpose register or a memory location) is multiplied by the second source operand (an immediate value). The product is then stored in the destination operand (a general-purpose register).

When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The CF and OF flags are set when significant bit (including the sign bit) are carried into the upper half of the result. The CF and OF flags are cleared when the result (including the sign bit) fits exactly in the lower half of the result.

The three forms of the IMUL instruction are similar in that the length of the product is calculated to twice the length of the operands. With the one-operand form, the product is stored exactly in the destination. With the two- and three-operand forms, however, the result is truncated to the length of the destination before it is stored in the destination register. Because of this truncation, the CF or OF flag should be tested to ensure that no significant bits are lost.

The two- and three-operand forms may also be used with unsigned operands because the lower half of the product is the same regardless if the operands are

### Opcode

<table>
<thead>
<tr>
<th>Opcode</th>
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<th>64-Bit Mode</th>
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<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>69 /r id</td>
<td>IMUL r32, imm32</td>
<td>Valid</td>
<td>Valid</td>
<td>doubleword register ← r/m32 * immediate doubleword.</td>
</tr>
<tr>
<td>REX.W + 69 /r id</td>
<td>IMUL r64, imm32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Quadword register ← r/m64 * immediate doubleword.</td>
</tr>
</tbody>
</table>

### NOTES:

* In 64-bit mode, r/m8 cannot be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
signed or unsigned. The CF and OF flags, however, cannot be used to determine if the upper half of the result is non-zero.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. Use of REX.W modifies the three forms of the instruction as follows.

- **One-operand form** — The source operand (in a 64-bit general-purpose register or memory location) is multiplied by the value in the RAX register and the product is stored in the RDX:RAX registers.

- **Two-operand form** — The source operand is promoted to 64 bits if it is a register or a memory location. If the source operand is an immediate, it is sign extended to 64 bits. The destination operand is promoted to 64 bits.

- **Three-operand form** — The first source operand (either a register or a memory location) and destination operand are promoted to 64 bits.

**Operation**

IF (NumberOfOperands = 1)
    THEN IF (OperandSize = 8)
        THEN
            AX ← AL * SRC (* Signed multiplication *)
            IF AL = AX
                THEN CF ← 0; OF ← 0;
                ELSE CF ← 1; OF ← 1; Fl;
            ELSE IF OperandSize = 16
                THEN
                    DX:AX ← AX * SRC (* Signed multiplication *)
                    IF sign_extend_to_32 (AX) = DX:AX
                        THEN CF ← 0; OF ← 0;
                        ELSE CF ← 1; OF ← 1; Fl;
                    ELSE IF OperandSize = 32
                        THEN
                            EDX:EAX ← EAX * SRC (* Signed multiplication *)
                            IF EAX = EDX:EAX
                                THEN CF ← 0; OF ← 0;
                                ELSE CF ← 1; OF ← 1; Fl;
                            ELSE (* OperandSize = 64 *)
                                RDX:RAX ← RAX * SRC (* Signed multiplication *)
                                IF RAX = RDX:RAX
                                    THEN CF ← 0; OF ← 0;
                                    ELSE CF ← 1; OF ← 1; Fl;
                                Fl;
                    Fl;
            Fl;
    Fl;
ELSE IF (NumberOfOperands = 2)
    THEN
        temp ← DEST * SRC (* Signed multiplication; temp is double DEST size *)
        DEST ← DEST * SRC (* Signed multiplication *)
        IF temp ≠ DEST
            THEN CF ← 1; OF ← 1;
            ELSE CF ← 0; OF ← 0; FI;
        ELSE (* NumberOfOperands = 3 *)
            DEST ← SRC1 * SRC2 (* Signed multiplication *)
            temp ← SRC1 * SRC2 (* Signed multiplication; temp is double SRC1 size *)
            IF temp ≠ DEST
                THEN CF ← 1; OF ← 1;
                ELSE CF ← 0; OF ← 0; FI;
        FI;
    FI;

**Flags Affected**

For the one operand form of the instruction, the CF and OF flags are set when significant bits are carried into the upper half of the result and cleared when the result fits exactly in the lower half of the result. For the two- and three-operand forms of the instruction, the CF and OF flags are set when the result must be truncated to fit in the destination operand size and cleared when the result fits exactly in the destination operand size. The SF, ZF, AF, and PF flags are undefined.

**Protected Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
INSTRUCTION SET REFERENCE, A-M

#SS If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
IN—Input from Port

Description

Copies the value from the I/O port specified with the second operand (source operand) to the destination operand (first operand). The source operand can be a byte-immediate or the DX register; the destination operand can be register AL, AX, or EAX, depending on the size of the port being accessed (8, 16, or 32 bits, respectively). Using the DX register as a source operand allows I/O port addresses from 0 to 65,535 to be accessed; using a byte immediate allows I/O port addresses 0 to 255 to be accessed.

When accessing an 8-bit I/O port, the opcode determines the port size; when accessing a 16- and 32-bit I/O port, the operand-size attribute determines the port size. At the machine code level, I/O instructions are shorter when accessing 8-bit I/O ports. Here, the upper eight bits of the port address will be 0.

This instruction is only useful for accessing I/O ports located in the processor’s I/O address space. See Chapter 13, “Input/Output,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information on accessing I/O ports in the I/O address space.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

IF ((PE = 1) and ((CPL > IOPL) or (VM = 1)))
    THEN (* Protected mode with CPL > IOPL or virtual-8086 mode *)
        IF (Any I/O Permission Bit for I/O port being accessed = 1)
            THEN (* I/O operation is not allowed *)
                #GP(0);
        ELSE (* I/O operation is allowed *)

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compats/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E4 ib</td>
<td>IN AL, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Input byte from imm8 I/O port address into AL.</td>
</tr>
<tr>
<td>E5 ib</td>
<td>IN AX, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Input word from imm8 I/O port address into AX.</td>
</tr>
<tr>
<td>E5 ib</td>
<td>IN EAX, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Input dword from imm8 I/O port address into EAX.</td>
</tr>
<tr>
<td>EC</td>
<td>IN AL,DX</td>
<td>Valid</td>
<td>Valid</td>
<td>Input byte from I/O port in DX into AL.</td>
</tr>
<tr>
<td>ED</td>
<td>IN AX,DX</td>
<td>Valid</td>
<td>Valid</td>
<td>Input word from I/O port in DX into AX.</td>
</tr>
<tr>
<td>ED</td>
<td>IN EAX,DX</td>
<td>Valid</td>
<td>Valid</td>
<td>Input doubleword from I/O port in DX into EAX.</td>
</tr>
</tbody>
</table>
DEST ← SRC; (* Read from selected I/O port *)
FI;
ELSE (Real Mode or Protected Mode with CPL ≤ IOPL *)
DEST ← SRC; (* Read from selected I/O port *)
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.
#UD If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, A-M

INC—Increment by 1

### Description

Adds 1 to the destination operand, while preserving the state of the CF flag. The destination operand can be a register or a memory location. This instruction allows a loop counter to be updated without disturbing the CF flag. (Use a ADD instruction with an immediate operand of 1 to perform an increment operation that does updates the CF flag.)

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, INC r16 and INC r32 are not encodable (because opcodes 40H through 47H are REX prefixes). Otherwise, the instruction's 64-bit mode default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits.

### Operation

\[
\text{DEST} \leftarrow \text{DEST} + 1;
\]

### AFlags Affected

The CF flag is not affected. The OF, SF, ZF, AF, and PF flags are set according to the result.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE /0</td>
<td>INC r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Increment r/m byte by 1.</td>
</tr>
<tr>
<td>REX + FE /0</td>
<td>INC r/m8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Increment r/m byte by 1.</td>
</tr>
<tr>
<td>FF /0</td>
<td>INC r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Increment r/m word by 1.</td>
</tr>
<tr>
<td>REX.W + FF /0</td>
<td>INC r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Increment r/m doubleword by 1.</td>
</tr>
<tr>
<td>40+ rw**</td>
<td>INC r16</td>
<td>N.E.</td>
<td>Valid</td>
<td>Increment word register by 1.</td>
</tr>
<tr>
<td>40+ rd</td>
<td>INC r32</td>
<td>N.E.</td>
<td>Valid</td>
<td>Increment doubleword register by 1.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

** 40H through 47H are REX prefixes in 64-bit mode.
Protected Mode Exceptions

#GP(0) If the destination operand is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS,
ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it
contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS
segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory
reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory
operand.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS,
ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS
segment limit.
#UD If the LOCK prefix is used but the destination is not a memory
operand.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS,
ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS
segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory
reference is made.
#UD If the LOCK prefix is used but the destination is not a memory
operand.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-
canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used but the destination is not a memory operand.
INS/INSB/INSW/INSD—Input from Port to String

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6C</td>
<td>INS m8, DX</td>
<td>Valid</td>
<td>Valid</td>
<td>Input byte from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.*</td>
</tr>
<tr>
<td>6D</td>
<td>INS m16, DX</td>
<td>Valid</td>
<td>Valid</td>
<td>Input word from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.¹</td>
</tr>
<tr>
<td>6D</td>
<td>INS m32, DX</td>
<td>Valid</td>
<td>Valid</td>
<td>Input doubleword from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.¹</td>
</tr>
<tr>
<td>6C</td>
<td>INSB</td>
<td>Valid</td>
<td>Valid</td>
<td>Input byte from I/O port specified in DX into memory location specified with ES:(E)DI or RDI.¹</td>
</tr>
<tr>
<td>6D</td>
<td>INSW</td>
<td>Valid</td>
<td>Valid</td>
<td>Input word from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.¹</td>
</tr>
<tr>
<td>6D</td>
<td>INSD</td>
<td>Valid</td>
<td>Valid</td>
<td>Input doubleword from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.¹</td>
</tr>
</tbody>
</table>

NOTES:
* In 64-bit mode, only 64-bit (RDI) and 32-bit (EDI) address sizes are supported. In non-64-bit mode, only 32-bit (EDI) and 16-bit (DI) address sizes are supported.

Description
Copies the data from the I/O port specified with the source operand (second operand) to the destination operand (first operand). The source operand is an I/O port address (from 0 to 65,535) that is read from the DX register. The destination operand is a memory location, the address of which is read from either the ES:DI, ES:EDI or the RDI registers (depending on the address-size attribute of the instruction, 16, 32 or 64, respectively). (The ES segment cannot be overridden with a segment override prefix.) The size of the I/O port being accessed (that is, the size of the source and destination operands) is determined by the opcode for an 8-bit I/O port or by the operand-size attribute of the instruction for a 16- or 32-bit I/O port.

At the assembly-code level, two forms of this instruction are allowed: the “explicit-operands” form and the “no-operands” form. The explicit-operands form (specified with the INS mnemonic) allows the source and destination operands to be specified explicitly. Here, the source operand must be “DX,” and the destination operand should be a symbol that indicates the size of the I/O port and the destination address. This explicit-operands form is provided to allow documentation; however, note that the documentation provided by this form can be misleading. That is, the
destination operand symbol must specify the correct **type** (size) of the operand (byte, word, or doubleword), but it does not have to specify the correct **location**. The location is always specified by the ES:(E)DI registers, which must be loaded correctly before the INS instruction is executed.

The no-operands form provides “short forms” of the byte, word, and doubleword versions of the INS instructions. Here also DX is assumed by the processor to be the source operand and ES:(E)DI is assumed to be the destination operand. The size of the I/O port is specified with the choice of mnemonic: INSB (byte), INSW (word), or INSD (doubleword).

After the byte, word, or doubleword is transferred from the I/O port to the memory location, the DI/EDI/RDI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the (E)DI register is incremented; if the DF flag is 1, the (E)DI register is decremented.) The (E)DI register is incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The INS, INSB, INSW, and INSD instructions can be preceded by the REP prefix for block input of ECX bytes, words, or doublewords. See “RDTSCP—Read Time-Stamp Counter and Processor ID” in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*, for a description of the REP prefix.

These instructions are only useful for accessing I/O ports located in the processor’s I/O address space. See Chapter 13, “Input/Output,” in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for more information on accessing I/O ports in the I/O address space.

In 64-bit mode, default address size is 64 bits, 32 bit address size is supported using the prefix 67H. The address of the memory destination is specified by RDI or EDI. 16-bit address size is not supported in 64-bit mode. The operand size is not promoted.

**Operation**

\[
\text{IF (}(\text{PE} = 1) \text{ and } (\text{CPL} > \text{IOPL}) \text{ or (VM = 1)))}
\]
\[
\text{THEN (} \ast \text{ Protected mode with CPL > IOPL or virtual-8086 mode } \ast \)
\]
\[
\text{IF (Any I/O Permission Bit for I/O port being accessed } = 1)\]
\[
\text{THEN (} \ast \text{ I/O operation is not allowed } \ast \)
\]
\[
\text{#GP(0)};\]
\[
\text{ELSE (} \ast \text{ I/O operation is allowed } \ast \)
\]
\[
\text{DEST } \leftarrow \text{ SRC; (} \ast \text{ Read from I/O port } \ast \)
\]
\[
\text{FI;}
\]
\[
\text{ELSE (Real Mode or Protected Mode with CPL IOPL * })\]
\[
\text{DEST } \leftarrow \text{ SRC; (} \ast \text{ Read from I/O port } \ast \)
\]
\[
\text{FI;}
\]

Non-64-bit Mode:
INSTRUCTION SET REFERENCE, A-M

IF (Byte transfer)
  THEN IF DF = 0
  THEN (E)DI ← (E)DI + 1;
  ELSE (E)DI ← (E)DI - 1; Fl;
ELSE IF (Word transfer)
  THEN IF DF = 0
  THEN (E)DI ← (E)DI + 2;
  ELSE (E)DI ← (E)DI - 2; Fl;
ELSE (* Doubleword transfer *)
  THEN IF DF = 0
  THEN (E)DI ← (E)DI + 4;
  ELSE (E)DI ← (E)DI - 4; Fl;
FI;
FI;
FI;64-bit Mode:

IF (Byte transfer)
  THEN IF DF = 0
  THEN (E|R)DI ← (E|R)DI + 1;
  ELSE (E|R)DI ← (E|R)DI - 1; Fl;
ELSE IF (Word transfer)
  THEN IF DF = 0
  THEN (E)DI ← (E)DI + 2;
  ELSE (E)DI ← (E)DI - 2; Fl;
ELSE (* Doubleword transfer *)
  THEN IF DF = 0
  THEN (E|R)DI ← (E|R)DI + 4;
  ELSE (E|R)DI ← (E|R)DI - 4; Fl;
FI;
FI;

Flags Affected
None.

Protected Mode Exceptions

#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.
If the destination is located in a non-writable segment.
If an illegal memory operand effective address in the ES segments is given.

#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.
If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
INSERTPS — Insert Packed Single Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 21 /r ib</td>
<td>INSERTPS xmm1, xmm2/m32, imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Insert a single precision floating-point value selected by imm8 from xmm2/m32 into xmm1 at the specified destination element specified by imm8 and zero out destination elements in xmm1 as indicated in imm8.</td>
</tr>
</tbody>
</table>

**Description**

Insert a single-precision floating-point value from the source operand (second operand) into a specified location in the destination register operand (first operand) and selectively zero out the data elements in the destination according to the mask field in the immediate byte (third operand). The source operand can be a memory location (32 bits) or an XMM register.

The immediate byte provides three fields:

- **COUNT_S**: The value of Imm8[7:6] selects the dword element from the source register; it is 0 if the source is a memory operand.
- **COUNT_D**: The value of Imm8[5:4] selects the target dword element in the destination register.
- **ZMASK**: Each bit of Imm8[3:0] selects a dword element in the destination register to be written with 0.0 if set to 1.

**Operation**

```
IF (SRC == REG) THEN COUNT_S ← imm8[7:6];
ELSE COUNT_S ← 0; FI;
COUNT_D ← imm8[5:4];
ZMASK ← imm8[3:0];

CASE (COUNT_S) OF
  0: TMP ← SRC[31:0];
  1: TMP ← SRC[63:32];
  2: TMP ← SRC[95:64];
  3: TMP ← SRC[127:96];

CASE (COUNT_D) OF
  0: TMP2[31:0] ← TMP;
      TMP2[127:32] ← DEST[127:32];
```
1: TMP[63:32] ← TMP;
   TMP[31:0] ← DEST[31:0];
   TMP[127:64] ← DEST[127:64];
2: TMP[95:64] ← TMP;
   TMP[63:0] ← DEST[63:0];
   TMP[127:96] ← DEST[127:96];
3: TMP[127:96] ← TMP;
   TMP[95:0] ← DEST[95:0];

IF (ZMASK[0] == 1) THEN DEST[31:0] ← 00000000H;
   ELSE DEST[31:0] ← TMP2[31:0];
   ELSE DEST[63:32] ← TMP2[63:32];
IF (ZMASK[2] == 1) THEN DEST[95:64] ← 00000000H;
   ELSE DEST[95:64] ← TMP2[95:64];
   ELSE DEST[127:96] ← TMP2[127:96];
FI;
FI;
FI;
FI;

Intel C/C++ Compiler Intrinsic Equivalent

INSERTPS  __m128 _mm_insert_ps(__m128 dst, __m128 src, const int ndx);

SIMD Floating-Point Exceptions
None

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.
INSTRUCTION SET REFERENCE, A-M

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Mode Exceptions
#GP(0) if any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Virtual 8086 Mode Exceptions
Same exceptions as in Real Address Mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in Protected Mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If TS in CR0 is set.
#UD If EM in CR0 is set.
If OSFXSR in CR4 is 0.
If CPUID feature flag ECX.SSE4_1 is 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
### INT n/INTO/INT 3—Call to Interrupt Procedure

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC</td>
<td>INT 3</td>
<td>Valid</td>
<td>Valid</td>
<td>Interrupt 3—trap to debugger.</td>
</tr>
<tr>
<td>CD ib</td>
<td>INT imm8</td>
<td>Valid</td>
<td>Valid</td>
<td>Interrupt vector number specified by immediate byte.</td>
</tr>
<tr>
<td>CE</td>
<td>INTO</td>
<td>Invalid</td>
<td>Valid</td>
<td>Interrupt 4—if overflow flag is 1.</td>
</tr>
</tbody>
</table>

### Description

The INT n instruction generates a call to the interrupt or exception handler specified with the destination operand (see the section titled “Interrupts and Exceptions” in Chapter 6 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*). The destination operand specifies an interrupt vector number from 0 to 255, encoded as an 8-bit unsigned intermediate value. Each interrupt vector number provides an index to a gate descriptor in the IDT. The first 32 interrupt vector numbers are reserved by Intel for system use. Some of these interrupts are used for internally generated exceptions.

The INT n instruction is the general mnemonic for executing a software-generated call to an interrupt handler. The INTO instruction is a special mnemonic for calling overflow exception (#OF), interrupt vector number 4. The overflow interrupt checks the OF flag in the EFLAGS register and calls the overflow interrupt handler if the OF flag is set to 1.

The INT 3 instruction generates a special one byte opcode (CC) that is intended for calling the debug exception handler. (This one byte form is valuable because it can be used to replace the first byte of any instruction with a breakpoint, including other one byte instructions, without over-writing other code). To further support its function as a debug breakpoint, the interrupt generated with the CC opcode also differs from the regular software interrupts as follows:

- Interrupt redirection does not happen when in VME mode; the interrupt is handled by a protected-mode handler.
- The virtual-8086 mode IOPL checks do not occur. The interrupt is taken without faulting at any IOPL level.

Note that the “normal” 2-byte opcode for INT 3 (CD03) does not have these special features. Intel and Microsoft assemblers will not generate the CD03 opcode from any mnemonic, but this opcode can be created by direct numeric code definition or by self-modifying code.

The action of the INT n instruction (including the INTO and INT 3 instructions) is similar to that of a far call made with the CALL instruction. The primary difference is that with the INT n instruction, the EFLAGS register is pushed onto the stack before the return address. (The return address is a far address consisting of the current values of the CS and EIP registers.) Returns from interrupt procedures are handled...
with the IRET instruction, which pops the EFLAGS information and return address from the stack.

The interrupt vector number specifies an interrupt descriptor in the interrupt descriptor table (IDT); that is, it provides index into the IDT. The selected interrupt descriptor in turn contains a pointer to an interrupt or exception handler procedure. In protected mode, the IDT contains an array of 8-byte descriptors, each of which is an interrupt gate, trap gate, or task gate. In real-address mode, the IDT is an array of 4-byte far pointers (2-byte code segment selector and a 2-byte instruction pointer), each of which point directly to a procedure in the selected segment. (Note that in real-address mode, the IDT is called the interrupt vector table, and its pointers are called interrupt vectors.)

The following decision table indicates which action in the lower portion of the table is taken given the conditions in the upper portion of the table. Each Y in the lower section of the decision table represents a procedure defined in the "Operation" section for this instruction (except #GP).

### Table 3-64. Decision Table

<table>
<thead>
<tr>
<th>PE</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>IOPL</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>&lt;3</td>
</tr>
<tr>
<td>DPL/CPL RELATIONSHIP</td>
<td>-</td>
<td>DPL&lt; CPL</td>
<td>DPL&gt; CPL</td>
<td>DPL= CPL or C</td>
<td>DPL&lt; CPL &amp; NC</td>
<td>-</td>
</tr>
<tr>
<td>INTERRUPT TYPE</td>
<td>-</td>
<td>S/W</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GATE TYPE</td>
<td>-</td>
<td>-</td>
<td>Task</td>
<td>Trap or Interrupt</td>
<td>Trap or Interrupt</td>
<td>Trap or Interrupt</td>
</tr>
<tr>
<td>REAL-ADDRESS-MODE</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PROTECTED-MODE</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>TRAP-OR-INTERRUPT-GATE</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>INTER-PRIVILEGE-LEVEL-INTERRUPT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>INTRA-PRIVILEGE-LEVEL-INTERRUPT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTERRUPT-FROM-VIRTUAL-8086-MODE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TASK-GATE</td>
<td></td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>#GP</td>
<td></td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td>Y</td>
</tr>
</tbody>
</table>

**NOTES:**
- Don't Care.
- Y Yes, action taken.
- Blank Action not taken.
When the processor is executing in virtual-8086 mode, the IOPL determines the action of the INT \( n \) instruction. If the IOPL is less than 3, the processor generates a \#GP(selector) exception; if the IOPL is 3, the processor executes a protected mode interrupt to privilege level 0. The interrupt gate’s DPL must be set to 3 and the target CPL of the interrupt handler procedure must be 0 to execute the protected mode interrupt to privilege level 0.

The interrupt descriptor table register (IDTR) specifies the base linear address and limit of the IDT. The initial base address value of the IDTR after the processor is powered up or reset is 0.

**Operation**

The following operational description applies not only to the INT \( n \) and INTO instructions, but also to external interrupts and exceptions.

\[
\text{IF } PE = 0 \\
\quad \text{THEN} \\
\quad \text{GOTO REAL-ADDRESS-MODE;}
\]

\[
\text{ELSE (* } PE = 1 *)
\]

\[
\text{IF (VM = 1 and IOPL < 3 AND INT } n) \\
\quad \text{THEN}
\]

\[
\#GP(0);
\]

\[
\text{ELSE (* Protected mode, IA-32e mode, or virtual-8086 mode interrupt *)}
\]

\[
\text{IF (IA32_EFER.LMA = 0)}
\]

\[
\quad \text{THEN (* Protected mode, or virtual-8086 mode interrupt *)}
\]

\[
\quad \text{GOTO PROTECTED-MODE;}
\]

\[
\text{ELSE (* IA-32e mode interrupt *)}
\]

\[
\quad \text{GOTO IA-32e-MODE;}
\]

\[
\quad \text{FI;}
\]

\[
\text{FI;}
\]

\[
\text{REAL-ADDRESS-MODE:}
\]

\[
\text{IF ((vector_number} \times 4) + 3) \text{ is not within IDT limit}
\]

\[
\quad \text{THEN #GP; FI;}
\]

\[
\text{IF stack not large enough for a 6-byte return information}
\]

\[
\quad \text{THEN #SS; FI;}
\]

\[
\text{Push (EFLAGS[15:0]);}
\]

\[
\text{IF ← 0; (* Clear interrupt flag *)}
\]

\[
\text{TF ← 0; (* Clear trap flag *)}
\]

\[
\text{AC ← 0; (* Clear AC flag *)}
\]

\[
\text{Push(CS);}
\]

\[
\text{Push(IP);}
\]

\[
(* \text{No error codes are pushed } *)
\]
CS ← IDT(Descriptor (vector_number * 4), selector));
EIP ← IDT(Descriptor (vector_number * 4), offset)); (* 16 bit offset AND 0000FFFFH *)
END;

PROTECTED-MODE:
IF ((vector_number * 8 + 7) is not within IDT limits
or selected IDT descriptor is not an interrupt-, trap-, or task-gate type
THEN #GP((vector_number * 8) + 2 + EXT); Fl;
(* EXT is bit 0 in error code *)
IF software interrupt (* Generated by INT n, INT 3, or INTO *)
THEN
  IF gate descriptor DPL < CPL
    THEN #GP((vector_number * 8) + 2); Fl;
    (* PE = 1, DPL < CPL, software interrupt *)
  FI;
IF gate not present
  THEN NP( (vector_number * 8) + 2 + EXT); Fl;
IF task gate (* Specified in the selected interrupt table descriptor *)
  THEN GOTO TASK-GATE;
ELSE GOTO TRAP-OR-INTERRUPT-GATE; (* PE = 1, trap/interrupt gate *)
FI;
END;

IA-32e-MODE:
IF ((vector_number * 16) + 15) is not in IDT limits
or selected IDT descriptor is not an interrupt-, or trap-gate type
THEN #GP((vector_number * 16) + 2 + EXT); Fl;
(* EXT is bit 0 in error code *)
IF software interrupt (* Generated by INT n, INT 3, but not INTO *)
THEN
  IF gate descriptor DPL < CPL
    THEN #GP((vector_number * 16) + 2); Fl;
    (* PE = 1, DPL < CPL, software interrupt *)
  ELSE (* Generated by INTO *)
    THEN #UD;
  FI;
IF gate not present
  THEN NP( (vector_number * 16) + 2 + EXT); Fl;
IF ((vector_number * 16)[IST] ≠ 0)
  NewRSP ← TSS[ISTx]; Fl;
GOTO TRAP-OR-INTERRUPT-GATE; (* Trap/interrupt gate *)
END;

TASK-GATE: (* PE = 1, task gate *)
Read segment selector in task gate (IDT descriptor);
  IF local/global bit is set to local
INT n/INTO/INT 3—Call to Interrupt Procedure

or index not within GDT limits
  THEN #GP(TSS selector); F;
Access TSS descriptor in GDT;
IF TSS descriptor specifies that the TSS is busy (low-order 5 bits set to 00001)
  THEN #GP(TSS selector); F;
IF TSS not present
  THEN #NP(TSS selector); F;
SWITCH-TASKS (with nesting) to TSS;
IF interrupt caused by fault with error code
  THEN
    IF stack limit does not allow push of error code
      THEN #SS(0); F;
      Push(error code);
    FI;
    IF EIP not within code segment limit
      THEN #GP(0); F;
END;
TRAP-OR-INTERRUPT-GATE:
  Read segment selector for trap or interrupt gate (IDT descriptor);
  IF segment selector for code segment is NULL
    THEN #GP(0H + EXT); F; (* NULL selector with EXT flag set *)
  IF segment selector is not within its descriptor table limits
    THEN #GP(selector + EXT); F;
  Read trap or interrupt handler descriptor;
  IF descriptor does not indicate a code segment
  or code segment descriptor DPL > CPL
    THEN #GP(selector + EXT); F;
  IF trap or interrupt gate segment is not present,
    THEN #NP(selector + EXT); F;
  IF code segment is non-conforming and DPL < CPL
    THEN
      IF VM = 0
        THEN
          GOTO INTER-PRIVILEGE-LEVEL-INTERRUPT;
          (* PE = 1, interrupt or trap gate, nonconforming
           code segment, DPL < CPL, VM = 0 *)
        ELSE (* VM = 1 *)
          IF code segment DPL ≠ 0
            THEN #GP; (new code segment selector);
            GOTO INTERRUPT-FROM-VIRTUAL-8086-MODE; F;
            (* PE = 1, interrupt or trap gate, DPL < CPL, VM = 1 *)
          FI;
        ELSE (* PE = 1, interrupt or trap gate, DPL ≥ CPL *)

INT n/INTO/INT 3—Call to Interrupt Procedure
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IF VM = 1
THEN #GP(new code segment selector); Fi;
IF code segment is conforming or code segment DPL = CPL
THEN
  GOTO INTRA-PRIVILEGE-LEVEL-INTERRUPT;
ELSE
  #GP(CodeSegmentSelector + EXT);
  (* PE = 1, interrupt or trap gate, nonconforming code segment, DPL > CPL *)
Fi;
FI;
END;
INTER-PRIVILEGE-LEVEL-INTERRUPT:
(* PE = 1, interrupt or trap gate, non-conforming code segment, DPL < CPL *)
(* Check segment selector and descriptor for stack of new privilege level in current TSS *)
IF current TSS is 32-bit TSS
THEN
  TSSstackAddress ← (new code segment DPL * 8) + 4;
  IF (TSSstackAddress + 7) > TSS limit
  THEN #TS(current TSS selector); Fi;
  NewSS ← TSSstackAddress + 4;
  NewESP ← stack address;
ELSE
  IF current TSS is 16-bit TSS
  THEN(* TSS is 16-bit *)
    TSSstackAddress ← (new code segment DPL * 4) + 2
    IF (TSSstackAddress + 4) > TSS limit
    THEN #TS(current TSS selector); Fi;
    NewESP ← TSSstackAddress;
    NewSS ← TSSstackAddress + 2;
  ELSE (* TSS is 64-bit *)
    NewESP ← TSS[RSP FOR NEW TARGET DPL];
    NewSS ← CodeSegmentDescriptor(DPL);
    (* null selector with RPL = new CPL *)
  FI;
FI;
IF segment selector is NULL
THEN #TS(EXT); Fi;
IF segment selector index is not within its descriptor table limits
or segment selector’s RPL ≠ DPL of code segment,
THEN #TS(SS selector + EXT); Fi;
IF (IA32_EFER.LMA = 0) (* Not IA-32e mode *)
  Read segment descriptor for stack segment in GDT or LDT;
INT n/INTO/INT 3—Call to Interrupt Procedure

IF stack segment DPL ≠ DPL of code segment, or stack segment does not indicate writable data segment
THEN #TS(SS selector + EXT); FI;
IF stack segment not present
THEN #SS(SS selector + EXT); FI;
FI

IF 32-bit gate
THEN
IF new stack does not have room for 24 bytes (error code pushed) or 20 bytes (no error code pushed)
THEN #SS(segment selector + EXT); FI;
FI
ELSE
IF 16-bit gate
THEN
IF new stack does not have room for 12 bytes (error code pushed) or 10 bytes (no error code pushed);
THEN #SS(segment selector + EXT); FI;
ELSE (* 64-bit gate *)
IF StackAddress is non-canonical
THEN #SS(0); FI;
FI;
FI;
IF (IA32_EFER.LMA = 0) (* Not IA-32e mode *)
THEN
IF instruction pointer is not within code segment limits
THEN #GP(0); FI;
SS:ESP ← TSS(NewSS:NewESP);
(* Segment descriptor information also loaded *)
ELSE
IF instruction pointer points to non-canonical address
THEN #GP(0); FI:
FI;
IF 32-bit gate
THEN
CS:EIP ← Gate(CS:EIP); (* Segment descriptor information also loaded *)
ELSE
IF 16-bit gate
THEN
CS:IP ← Gate(CS:IP);
(* Segment descriptor information also loaded *)
ELSE (* 64-bit gate *)
CS:RIP ← Gate(CS:RIP);
(* Segment descriptor information also loaded *)
INT n/INTO/INT 3—Call to Interrupt Procedure

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Fi;
FI;
IF 32-bit gate
THEN
Push(far pointer to old stack);
(* Old SS and ESP, 3 words padded to 4 *)
Push(EFLAGS);
Push(far pointer to return instruction);
(* Old CS and EIP, 3 words padded to 4 *)
Push(ErrorCode); (* If needed, 4 bytes *)
ELSE
IF 16-bit gate
THEN
Push(far pointer to old stack);
(* Old SS and SP, 2 words *)
Push(EFLAGS(15-0));
Push(far pointer to return instruction);
(* Old CS and IP, 2 words *)
Push(ErrorCode); (* If needed, 2 bytes *)
ELSE (* 64-bit gate *)
Push(far pointer to old stack);
(* Old SS and SP, each an 8-byte push *)
Push(RFLAGS); (* 8-byte push *)
Push(far pointer to return instruction);
(* Old CS and RIP, each an 8-byte push *)
Push(ErrorCode); (* If needed, 8-bytes *)

FI;
CPL ← CodeSegmentDescriptor(DPL);
CS(RPL) ← CPL;
IF interrupt gate
THEN IF ← 0 (* Interrupt flag set to 0: disabled *); FI;
TF ← 0;
VM ← 0;
RF ← 0;
NT ← 0;
END;
INTERRUPT-FROM-VIRTUAL-8086-MODE:
(* Check segment selector and descriptor for privilege level 0 stack in current TSS *)
IF current TSS is 32-bit TSS
THEN
TSSstackAddress ← (new code segment DPL * 8) + 4;
IF (TSSstackAddress + 7) > TSS limit
THEN #TS(current TSS selector); FI;
INT n/INTO/INT 3—Call to Interrupt Procedure

NewSS ← TSSstackAddress + 4;
NewESP ← stack address;
ELSE (* TSS is 16-bit *)
    TSSstackAddress ← (new code segment DPL + 4) + 2;
    IF (TSSstackAddress + 4) > TSS limit
        THEN #TS(current TSS selector); Fl;
NewESP ← TSSstackAddress;
NewSS ← TSSstackAddress + 2;
Fl;
IF segment selector is NULL
    THEN #TS(EXT); Fl;
IF segment selector index is not within its descriptor table limits
or segment selector’s RPL ≠ DPL of code segment
    THEN #TS(SS selector + EXT); Fl;
Access segment descriptor for stack segment in GDT or LDT;
IF stack segment DPL ≠ DPL of code segment,
or stack segment does not indicate writable data segment
    THEN #TS(SS selector + EXT); Fl;
IF stack segment not present
    THEN #SS(SS selector + EXT); Fl;
IF 32-bit gate
    THEN
        IF new stack does not have room for 40 bytes (error code pushed)
or 36 bytes (no error code pushed)
            THEN #SS(segment selector + EXT); Fl;
    ELSE IF 16-bit gate
        THEN
            IF new stack does not have room for 20 bytes (error code pushed)
or 18 bytes (no error code pushed)
                THEN #SS(segment selector + EXT); Fl;
        ELSE (* 64-bit gate *)
            IF StackAddress is non-canonical
                THEN #SS(0);
        Fl;
    Fl;
IF instruction pointer is not within code segment limits
    THEN #GP(0); Fl;
tempEFLAGS ← EFLAGS;
VM ← 0;
TF ← 0;
RF ← 0;
NT ← 0;
IF service through interrupt gate
THEN IF = 0; FI;
TempSS ← SS;
TempESP ← ESP;
SS:ESP ← TSS(SS0:ESP0); (* Change to level 0 stack segment *)
(* Following pushes are 16 bits for 16-bit gate and 32 bits for 32-bit gates;
Segment selector pushes in 32-bit mode are padded to two words *)
Push(GS);
Push(FS);
Push(DS);
Push(ES);
Push(TempSS);
Push(TempESP);
Push(TempEFlags);
Push(CS);
Push(EIP);
GS ← 0; (* Segment registers NULLified, invalid in protected mode *)
FS ← 0;
DS ← 0;
ES ← 0;
CS ← Gate(CS);
IF OperandSize = 32
    THEN
        EIP ← Gate(instruction pointer);
        ELSE (* OperandSize is 16 *)
            EIP ← Gate(instruction pointer) AND 0000FFFFH;
        FI;
    (* Start execution of new routine in Protected Mode *)
END;
INTRA-PRIVILEGE-LEVEL-INTERRUPT:
(* PE = 1, DPL = CPL or conforming segment *)
IF 32-bit gate and IA32_EFER.LMA = 0
    THEN
        IF current stack does not have room for 16 bytes (error code pushed)
            or 12 bytes (no error code pushed)
            THEN #SS(0); FI;
        ELSE IF 16-bit gate
            IF current stack does not have room for 8 bytes (error code pushed)
                or 6 bytes (no error code pushed)
                THEN #SS(0); FI;
            ELSE (* 64-bit gate*)
                IF StackAddress is non-canonical
                    THEN #SS(0);
                FI;
        FI;
    ELSE IF 16-bit gate
        IF current stack does not have room for 8 bytes (error code pushed)
            or 6 bytes (no error code pushed)
            THEN #SS(0); FI;
        ELSE (* 64-bit gate*)
            IF StackAddress is non-canonical
                THEN #SS(0);
            FI;
        FI;
INT n/INTO/INT 3—Call to Interrupt Procedure

Fl;
IF instruction pointer not within code segment limit
    THEN #GP(0); Fl;
IF 32-bit gate
    THEN
        Push (EFLAGS);
        Push (far pointer to return instruction); (* 3 words padded to 4 *)
        CS:EIP ← Gate(CS:EIP); (* Segment descriptor information also loaded *)
        Push (ErrorCode); (* If any *)
    ELSE
        IF 16-bit gate
            THEN
                Push (FLAGS);
                Push (far pointer to return location); (* 2 words *)
                CS:IP ← Gate(CS:IP);
                (* Segment descriptor information also loaded *)
                Push (ErrorCode); (* If any *)
            ELSE (* 64-bit gate*)
                Push(far pointer to old stack);
                (* Old SS and SP, each an 8-byte push *)
                Push(RFLAGS); (* 8-byte push *)
                Push(far pointer to return instruction);
                (* Old CS and RIP, each an 8-byte push *)
                Push(ErrorCode); (* If needed, 8 bytes *)
                CS:RIP ← GATE(CS:RIP);
                (* Segment descriptor information also loaded *)
            FI;
        FI;
    CS(RPL) ← CPL;
    IF interrupt gate
        THEN IF ← 0; Fl; (* Interrupt flag set to 0: disabled *)
        TF ← 0;
        NT ← 0;
        VM ← 0;
        RF ← 0;
END;

Flags Affected

The EFLAGS register is pushed onto the stack. The IF, TF, NT, AC, RF, and VM flags may be cleared, depending on the mode of operation of the processor when the INT instruction is executed (see the “Operation” section). If the interrupt uses a task gate, any flags may be set or cleared, controlled by the EFLAGS image in the new task’s TSS.
Protected Mode Exceptions

#GP(0) If the instruction pointer in the IDT or in the interrupt-, trap-, or task gate is beyond the code segment limits.

#GP(selector) If the segment selector in the interrupt-, trap-, or task gate is NULL.
If an interrupt-, trap-, or task gate, code segment, or TSS segment selector index is outside its descriptor table limits.
If the interrupt vector number is outside the IDT limits.
If an IDT descriptor is not an interrupt-, trap-, or task-selector.
If an interrupt is generated by the INT n, INT 3, or INTO instruction and the DPL of an interrupt-, trap-, or task-selector is less than the CPL.
If the segment selector in an interrupt- or trap-gate does not point to a segment descriptor for a code segment.
If the segment selector for a TSS has its local/global bit set for local.
If a TSS segment descriptor specifies that the TSS is busy or not available.

#SS(0) If pushing the return address, flags, or error code onto the stack exceeds the bounds of the stack segment and no stack switch occurs.

#SS(selector) If the SS register is being loaded and the segment pointed to is marked not present.
If pushing the return address, flags, error code, or stack segment pointer exceeds the bounds of the new stack segment when a stack switch occurs.

#NP(selector) If code segment, interrupt-, trap-, or task gate, or TSS is not present.

#TS(selector) If the RPL of the stack segment selector in the TSS is not equal to the DPL of the code segment being accessed by the interrupt or trap gate.
If DPL of the stack segment descriptor pointed to by the stack segment selector in the TSS is not equal to the DPL of the code segment descriptor for the interrupt or trap gate.
If the stack segment selector in the TSS is NULL.
If the stack segment for the TSS is not a writable data segment.
If segment-selector index for stack segment is outside descriptor table limits.

#PF(fault-code) If a page fault occurs.

#UD If the LOCK prefix is used.
Real-Address Mode Exceptions

#GP   If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
      If the interrupt vector number is outside the IDT limits.

#SS   If stack limit violation on push.
      If pushing the return address, flags, or error code onto the stack exceeds the bounds of the stack segment.

#UD   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) (For INT n, INTO, or BOUND instruction) If the IOPL is less than 3 or the DPL of the interrupt-, trap-, or task-gate descriptor is not equal to 3.
      If the instruction pointer in the IDT or in the interrupt-, trap-, or task gate is beyond the code segment limits.

#GP(selector) If the segment selector in the interrupt-, trap-, or task gate is NULL.
      If a interrupt-, trap-, or task gate, code segment, or TSS segment selector index is outside its descriptor table limits.
      If the interrupt vector number is outside the IDT limits.
      If an IDT descriptor is not an interrupt-, trap-, or task-descriptor.
      If an interrupt is generated by the INT n instruction and the DPL of an interrupt-, trap-, or task-descriptor is less than the CPL.
      If the segment selector in an interrupt- or trap-gate does not point to a segment descriptor for a code segment.
      If the segment selector for a TSS has its local/global bit set for local.

#SS(selector) If the SS register is being loaded and the segment pointed to is marked not present.
      If pushing the return address, flags, error code, stack segment pointer, or data segments exceeds the bounds of the stack segment.

#NP(selector) If code segment, interrupt-, trap-, or task gate, or TSS is not present.

#TS(selector) If the RPL of the stack segment selector in the TSS is not equal to the DPL of the code segment being accessed by the interrupt or trap gate.
      If DPL of the stack segment descriptor for the TSS’s stack segment is not equal to the DPL of the code segment descriptor for the interrupt or trap gate.
      If the stack segment selector in the TSS is NULL.
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If the stack segment for the TSS is not a writable data segment.
If segment-selector index for stack segment is outside descriptor table limits.

#PF(fault-code) If a page fault occurs.
#BP If the INT 3 instruction is executed.
#OF If the INTO instruction is executed and the OF flag is set.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0) If the instruction pointer in the 64-bit interrupt gate or 64-bit trap gate is non-canonical.
#GP(selector) If the segment selector in the 64-bit interrupt or trap gate is NULL.
If the interrupt vector number is outside the IDT limits.
If the interrupt vector number points to a gate which is in non-canonical space.
If the interrupt vector number points to a descriptor which is not a 64-bit interrupt gate or 64-bit trap gate.
If the descriptor pointed to by the gate selector is outside the descriptor table limit.
If the descriptor pointed to by the gate selector is in non-canonical space.
If the descriptor pointed to by the gate selector is not a code segment.
If the descriptor pointed to by the gate selector doesn’t have the L-bit set, or has both the L-bit and D-bit set.
If the descriptor pointed to by the gate selector has DPL > CPL.

#SS(0) If a push of the old EFLAGS, CS selector, EIP, or error code is in non-canonical space with no stack switch.
#SS(selector) If a push of the old SS selector, ESP, EFLAGS, CS selector, EIP, or error code is in non-canonical space on a stack switch (either CPL change or no-CPL with IST).
#NP(selector) If the 64-bit interrupt-gate, 64-bit trap-gate, or code segment is not present.
INT n/INTO/INT 3—Call to Interrupt Procedure

#TS(selector)  If an attempt to load RSP from the TSS causes an access to non-canonical space.
    If the RSP from the TSS is outside descriptor table limits.
#PF(fault-code)  If a page fault occurs.
#UD  If the LOCK prefix is used.
INVD—Invalidate Internal Caches

**Description**

Invalidates (flushes) the processor’s internal caches and issues a special-function bus cycle that directs external caches to also flush themselves. Data held in internal caches is not written back to main memory.

After executing this instruction, the processor does not wait for the external caches to complete their flushing operation before proceeding with instruction execution. It is the responsibility of hardware to respond to the cache flush signal.

The INVD instruction is a privileged instruction. When the processor is running in protected mode, the CPL of a program or procedure must be 0 to execute this instruction.

Use this instruction with care. Data cached internally and not written back to main memory will be lost. Unless there is a specific requirement or benefit to flushing caches without writing back modified cache lines (for example, testing or fault recovery where cache coherency with main memory is not a concern), software should use the WBINVD instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

The INVD instruction is implementation dependent; it may be implemented differently on different families of Intel 64 or IA-32 processors. This instruction is not supported on IA-32 processors earlier than the Intel486 processor.

**Operation**

- Flush(InternalCaches);
- SignalFlush(ExternalCaches);
- Continue (* Continue execution * )

**Flags Affected**

None.
Protected Mode Exceptions
#GP(0) If the current privilege level is not 0.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) The INVD instruction cannot be executed in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
INVLPG—Invalidate TLB Entry

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01/7</td>
<td>INVLPG m</td>
<td>Valid</td>
<td>Valid</td>
<td>Invalidate TLB Entry for page that contains m.</td>
</tr>
</tbody>
</table>

**Description**

Invalidates (flushes) the translation lookaside buffer (TLB) entry specified with the source operand. The source operand is a memory address. The processor determines the page that contains that address and flushes the TLB entry for that page.

The INVLPG instruction is a privileged instruction. When the processor is running in protected mode, the CPL of a program or procedure must be 0 to execute this instruction.

The INVLPG instruction normally flushes the TLB entry only for the specified page; however, in some cases, it flushes the entire TLB. See “MOV—Move to/from Control Registers” in this chapter for further information on operations that flush the TLB.

This instruction’s operation is the same in all non-64-bit modes. It also operates the same in 64-bit mode, except if the memory address is in non-canonical form. In this case, INVLPG is the same as a NOP.

**IA-32 Architecture Compatibility**

The INVLPG instruction is implementation dependent, and its function may be implemented differently on different families of Intel 64 or IA-32 processors. This instruction is not supported on IA-32 processors earlier than the Intel486 processor.

**Operation**

Flush(RelevantTLBEntries);
Continue; (* Continue execution *)

**Flags Affected**

None.

**Protected Mode Exceptions**

- **#GP(0)**     If the current privilege level is not 0.
- **#UD**        Operand is a register.
  If the LOCK prefix is used.
**Real-Address Mode Exceptions**

#UD  
Operand is a register.
If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#GP(0)  
The INVLPG instruction cannot be executed at the virtual-8086 mode.

**64-Bit Mode Exceptions**

#GP(0)  
If the current privilege level is not 0.

#UD  
Operand is a register.
If the LOCK prefix is used.
IRET/IRETD—Interrupt Return

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CF</td>
<td>IRET</td>
<td>Valid</td>
<td>Valid</td>
<td>Interrupt return (16-bit operand size).</td>
</tr>
<tr>
<td>CF</td>
<td>IRETD</td>
<td>Valid</td>
<td>Valid</td>
<td>Interrupt return (32-bit operand size).</td>
</tr>
<tr>
<td>REX.w + CF</td>
<td>IRETQ</td>
<td>Valid</td>
<td>N.E.</td>
<td>Interrupt return (64-bit operand size).</td>
</tr>
</tbody>
</table>

Description

Returns program control from an exception or interrupt handler to a program or procedure that was interrupted by an exception, an external interrupt, or a software-generated interrupt. These instructions are also used to perform a return from a nested task. (A nested task is created when a CALL instruction is used to initiate a task switch or when an interrupt or exception causes a task switch to an interrupt or exception handler.) See the section titled “Task Linking” in Chapter 7 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

IRET and IRETD are mnemonics for the same opcode. The IRETD mnemonic (interrupt return double) is intended for use when returning from an interrupt when using the 32-bit operand size; however, most assemblers use the IRET mnemonic interchangeably for both operand sizes.

In Real-Address Mode, the IRET instruction preforms a far return to the interrupted program or procedure. During this operation, the processor pops the return instruction pointer, return code segment selector, and EFLAGS image from the stack to the EIP, CS, and EFLAGS registers, respectively, and then resumes execution of the interrupted program or procedure.

In Protected Mode, the action of the IRET instruction depends on the settings of the NT (nested task) and VM flags in the EFLAGS register and the VM flag in the EFLAGS image stored on the current stack. Depending on the setting of these flags, the processor performs the following types of interrupt returns:

- Return from virtual-8086 mode.
- Return to virtual-8086 mode.
- Intra-privilege level return.
- Inter-privilege level return.
- Return from nested task (task switch).

If the NT flag (EFLAGS register) is cleared, the IRET instruction performs a far return from the interrupt procedure, without a task switch. The code segment being returned to must be equally or less privileged than the interrupt handler routine (as indicated by the RPL field of the code segment selector popped from the stack).
As with a real-address mode interrupt return, the IRET instruction pops the return instruction pointer, return code segment selector, and EFLAGS image from the stack to the EIP, CS, and EFLAGS registers, respectively, and then resumes execution of the interrupted program or procedure. If the return is to another privilege level, the IRET instruction also pops the stack pointer and SS from the stack, before resuming program execution. If the return is to virtual-8086 mode, the processor also pops the data segment registers from the stack.

If the NT flag is set, the IRET instruction performs a task switch (return) from a nested task (a task called with a CALL instruction, an interrupt, or an exception) back to the calling or interrupted task. The updated state of the task executing the IRET instruction is saved in its TSS. If the task is re-entered later, the code that follows the IRET instruction is executed.

If the NT flag is set and the processor is in IA-32e mode, the IRET instruction causes a general protection exception.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.W prefix promotes operation to 64 bits (IRETQ). See the summary chart at the beginning of this section for encoding data and limits.

See “Changes to Instruction Behavior in VMX Non-Root Operation” in Chapter 22 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B, for more information about the behavior of this instruction in VMX non-root operation.

Operation

IF PE = 0
THEN
    GOTO REAL-ADDRESS-MODE;
ELSE
    IF (IA32_EFER.LMA = 0)
        THEN (* Protected mode *)
            GOTO PROTECTED-MODE;
        ELSE (* IA-32e mode *)
            GOTO IA-32e-MODE;
    FI;
FI;
REAL-ADDRESS-MODE;
    IF OperandSize = 32
        THEN
            IF top 12 bytes of stack not within stack limits
                THEN #SS; FI;
            tempEIP ← 4 bytes at end of stack
            IF tempEIP[31:16] is not zero THEN #GP(0); FI;
            EIP ← Pop();
            CS ← Pop(); (* 32-bit pop, high-order 16 bits discarded *)
            tempEFLAGS ← Pop();
    ELSE
        GOTO IA-32e-MODE;
    FI;
    GOTO IA-32e-MODE;
**INSTRUCTION SET REFERENCE, A-M**

EFLAGS ← (tempEFLAGS AND 257FD5H) OR (EFLAGS AND 1A0000H);
ELSE (* OperandSize = 16 *)
    IF top 6 bytes of stack are not within stack limits
        THEN #SS; Fl;
    EIP ← Pop(); (* 16-bit pop; clear upper 16 bits *)
    CS ← Pop(); (* 16-bit pop *)
    EFLAGS[15:0] ← Pop();
    Fl;
END;

PROTECTED-MODE:
    IF VM = 1 (* Virtual-8086 mode: PE = 1, VM = 1 *)
        THEN
            GOTO RETURN-FROM-VIRTUAL-8086-MODE; (* PE = 1, VM = 1 *)
        Fl;
    IF NT = 1
        THEN
            GOTO TASK-RETURN; (* PE = 1, VM = 0, NT = 1 *)
        Fl;
    IF OperandSize = 32
        THEN
            IF top 12 bytes of stack not within stack limits
                THEN #SS(0); Fl;
            tempEIP ← Pop();
            tempCS ← Pop();
            tempEFLAGS ← Pop();
            ELSE (* OperandSize = 16 *)
                IF top 6 bytes of stack not within stack limits
                    THEN #SS(0); Fl;
                tempEIP ← Pop();
                tempCS ← Pop();
                tempEFLAGS ← Pop();
                tempEIP ← tempEIP AND FFFFH;
                tempEFLAGS ← tempEFLAGS AND FFFFH;
            Fl;
    IF tempEFLAGS(VM) = 1 and CPL = 0
        THEN
            GOTO RETURN-TO-VIRTUAL-8086-MODE;
        ELSE
            GOTO PROTECTED-MODE-RETURN;
        Fl;
    IA-32e-MODE:
        IF NT = 1
            THEN #GP(0);
ELSE IF OperandSize = 32
    THEN
        IF top 12 bytes of stack not within stack limits
            THEN #SS(0); Fl;
        tempEIP ← Pop();
        tempCS ← Pop();
        tempEFLAGS ← Pop();
        ELSE IF OperandSize = 16
            THEN
            IF top 6 bytes of stack not within stack limits
                THEN #SS(0); Fl;
            tempEIP ← Pop();
            tempCS ← Pop();
            tempEFLAGS ← Pop();
            tempEIP ← tempEIP AND FFFFH;
            tempEFLAGS ← tempEFLAGS AND FFFFH;
        FI;
        ELSE (* OperandSize = 64 *)
            THEN
                tempRIP ← Pop();
                tempCS ← Pop();
                tempEFLAGS ← Pop();
                tempRSP ← Pop();
                tempSS ← Pop();
            FI;
        GOTO IA-32e-MODE-RETURN;
    FI;
RETURN-FROM-VIRTUAL-8086-MODE:
(* Processor is in virtual-8086 mode when IRET is executed and stays in virtual-8086 mode *)
    IF IOPL = 3 (* Virtual mode: PE = 1, VM = 1, IOPL = 3 *)
        THEN IF OperandSize = 32
            THEN
            IF top 12 bytes of stack not within stack limits
                THEN #SS(0); Fl;
            IF instruction pointer not within code segment limits
                THEN #GP(0); Fl;
            EIP ← Pop();
            CS ← Pop(); (* 32-bit pop, high-order 16 bits discarded *)
            EFLAGS ← Pop();
            (* VM, IOPL,VIP and VIF EFLAG bits not modified by pop *)
        ELSE (* OperandSize = 16 *)
            IF top 6 bytes of stack not within stack limits
                THEN #SS(0); Fl;
            IF instruction pointer not within code segment limits
                THEN #GP(0); Fl;
            ELSE IF OperandSize = 32
                THEN #SS(0); Fl;
            ELSE IF OperandSize = 16
                THEN #SS(0); Fl;
            IF instruction pointer not within code segment limits
                THEN #GP(0); Fl;
            ELSE (* OperandSize = 64 *)
                THEN
                    tempRIP ← Pop();
                    tempCS ← Pop();
                    tempEFLAGS ← Pop();
                    tempRSP ← Pop();
                    tempSS ← Pop();
                FI;
            GOTO IA-32e-MODE-RETURN;
THEN #GP(0); FI;
EIP ← Pop();
EIP ← EIP AND 0000FFFFH;
CS ← Pop(); (* 16-bit pop *)
EFLAGS[15:0] ← Pop(); (* IOPL in EFLAGS not modified by pop *)
FI;
ELSE
#GP(0); (* Trap to virtual-8086 monitor: PE = 1, VM = 1, IOPL < 3 *)
FI;
END;

RETURN-TO-VIRTUAL-8086-MODE:
(* Interrupted procedure was in virtual-8086 mode: PE = 1, CPL=0, VM = 1 in flag image *)
If top 24 bytes of stack are not within stack segment limits
THEN #SS(0); FI;
If instruction pointer not within code segment limits
THEN #GP(0); FI;
CS ← tempCS;
EIP ← tempEIP;
EFLAGS ← tempEFLAGS;
TempESP ← Pop();
TempSS ← Pop();
ES ← Pop(); (* Pop 2 words; throw away high-order word *)
DS ← Pop(); (* Pop 2 words; throw away high-order word *)
FS ← Pop(); (* Pop 2 words; throw away high-order word *)
GS ← Pop(); (* Pop 2 words; throw away high-order word *)
SS:ESP ← TempSS:TempESP;
CPL ← 3;
(* Resume execution in Virtual-8086 mode *)
END;

TASK-RETURN; (* PE = 1, VM = 0, NT = 1 *)
Read segment selector in link field of current TSS;
If local/global bit is set to local
or index not within GDT limits
THEN #TS (TSS selector); FI;
Access TSS for task specified in link field of current TSS;
If TSS descriptor type is not TSS or if the TSS is marked not busy
THEN #TS (TSS selector); FI;
If TSS not present
THEN #NP(TSS selector); FI;
SWITCH-TASKS (without nesting) to TSS specified in link field of current TSS;
Mark the task just abandoned as NOT BUSY;
IF EIP is not within code segment limit
THEN #GP(0); Fl;
END;

PROTECTED-MODE-RETURN: (* PE = 1 *)
IF return code segment selector is NULL
THEN GP(0); Fl;
IF return code segment selector addresses descriptor beyond descriptor table limit
THEN GP(selector); Fl;
Read segment descriptor pointed to by the return code segment selector;
IF return code segment descriptor is not a code segment
THEN #GP(selector); Fl;
IF return code segment selector RPL < CPL
THEN #GP(selector); Fl;
IF return code segment descriptor is conforming
and return code segment DPL > return code segment selector RPL
THEN GP(selector); Fl;
IF return code segment selector is not present
THEN #NP(selector); Fl;
IF return code segment selector RPL > CPL
THEN GOTO RETURN-OUTER-PRIVILEGE-LEVEL;
ELSE GOTO RETURN-TO-SAME-PRIVILEGE-LEVEL; Fl;
END;

RETURN-TO-SAME-PRIVILEGE-LEVEL: (* PE = 1, RPL = CPL *)
IF new mode ≠ 64-Bit Mode
THEN
IF tempEIP is not within code segment limits
THEN #GP(0); Fl;
EIP ← tempEIP;
ELSE (* new mode = 64-bit mode *)
IF tempRIP is non-canonical
THEN #GP(0); Fl;
RIP ← tempRIP;
FI;
CS ← tempCS; (* Segment descriptor information also loaded *)
EFLAGS (CF, PF, AF, ZF, SF, TF, DF, OF, NT) ← tempEFLAGS;
IF OperandSize = 32 or OperandSize = 64
THEN EFLAGS(RF, AC, ID) ← tempEFLAGS; Fl;
IF CPL ≤ IOPL
THEN EFLAGS(IF) ← tempEFLAGS; Fl;
IF CPL = 0
THEN (* VM = 0 in flags image *)
INSTRUCTION SET REFERENCE, A-M

EFLAGS(IOPL) ← tempEFLAGS;
IF OperandSize = 32 or OperandSize = 64
    THEN EFLAGS(VIF, VIP) ← tempEFLAGS; Fl;
FI;
END;

RETURN-TO-OUTER-PRIVILEGE-LEVEL:
IF OperandSize = 32
    THEN
        IF top 8 bytes on stack are not within limits
            THEN #SS(0); Fl;
        ELSE (* OperandSize = 16 *)
            IF top 4 bytes on stack are not within limits
                THEN #SS(0); Fl;
        FI;
    Read return segment selector;
    IF stack segment selector is NULL
        THEN #GP(0); Fl;
    IF return stack segment selector index is not within its descriptor table limits
        THEN #GP(SSselector); Fl;
    Read segment descriptor pointed to by return segment selector;
    IF stack segment selector RPL ≠ RPL of the return code segment selector
        or the stack segment descriptor does not indicate a writable data segment;
        or the stack segment DPL ≠ RPL of the return code segment selector
        THEN #GP(SS selector); Fl;
    IF stack segment is not present
        THEN #SS(SS selector); Fl;
    IF new mode ≠ 64-Bit Mode
        THEN
            IF tempEIP is not within code segment limits
                THEN #GP(0); Fl;
            EIP ← tempEIP;
        ELSE (* new mode = 64-bit mode *)
            IF tempRIP is non-canonical
                THEN #GP(0); Fl;
            RIP ← tempRIP;
        Fl;
    CS ← tempCS;
    EFLAGS (CF, PF, AF, ZF, SF, DF, OF, NT) ← tempEFLAGS;
    IF OperandSize = 32
        THEN EFLAGS(RF, AC, ID) ← tempEFLAGS; Fl;
    IF CPL ≤ IOPL
        THEN EFLAGS(IF) ← tempEFLAGS; Fl;
IF CPL = 0 THEN
   EFLAGS(IOP) ← tempEFLAGS;
   IF OperandSize = 32 THEN EFLAGS(VM, VIF, VIP) ← tempEFLAGS; FI;
   IF OperandSize = 64 THEN EFLAGS(VIF, VIP) ← tempEFLAGS; FI;
   FI;
CPL ← RPL of the return code segment selector;
FOR each of segment register (ES, FS, GS, and DS) DO
   IF segment register points to data or non-conforming code segment and CPL > segment descriptor DPL (* Stored in hidden part of segment register *) THEN (* Segment register invalid *)
      SegmentSelector ← 0; (* NULL segment selector *)
   FI;
OD;
END;

IA-32e-MODE-RETURN: (* IA32_EFER.LMA = 1, PE = 1 *)
IF ( (return code segment selector is NULL) or (return RIP is non-canonical) or (SS selector is NULL going back to compatibility mode) or (SS selector is NULL going back to CPL3 64-bit mode) or (RPL < CPL going back to non-CPL3 64-bit mode for a NULL SS selector) )
   THEN GP(0); FI;
IF return code segment selector addresses descriptor beyond descriptor table limit THEN GP(selector); FI;
Read segment descriptor pointed to by the return code segment selector;
IF return code segment descriptor is not a code segment THEN #GP(selector); FI;
IF return code segment selector RPL < CPL THEN #GP(selector); FI;
IF return code segment descriptor is conforming and return code segment DPL > return code segment selector RPL THEN #GP(selector); FI;
IF return code segment descriptor is not present THEN #NP(selector); FI;
IF return code segment selector RPL > CPL THEN GOTO RETURN-OUTER-PRIVILEGE-LEVEL; ELSE GOTO RETURN-TO-SAME-PRIVILEGE-LEVEL; FI;
END;
**Flags Affected**

All the flags and fields in the EFLAGS register are potentially modified, depending on the mode of operation of the processor. If performing a return from a nested task to a previous task, the EFLAGS register will be modified according to the EFLAGS image stored in the previous task’s TSS.

**Protected Mode Exceptions**

- **#GP(0)**  
  If the return code or stack segment selector is NULL.  
  If the return instruction pointer is not within the return code segment limit.

- **#GP(selector)**  
  If a segment selector index is outside its descriptor table limits.  
  If the return code segment selector RPL is greater than the CPL.  
  If the DPL of a conforming-code segment is greater than the return code segment selector RPL.  
  If the DPL for a nonconforming-code segment is not equal to the RPL of the code segment selector.  
  If the stack segment descriptor DPL is not equal to the RPL of the return code segment selector.  
  If the stack segment is not a writable data segment.  
  If the stack segment selector RPL is not equal to the RPL of the return code segment selector.  
  If the segment descriptor for a code segment does not indicate it is a code segment.  
  If the segment selector for a TSS has its local/global bit set for local.  
  If a TSS segment descriptor specifies that the TSS is not busy.  
  If a TSS segment descriptor specifies that the TSS is not available.

- **#SS(0)**  
  If the top bytes of stack are not within stack limits.

- **#NP(selector)**  
  If the return code or stack segment is not present.

- **#PF(fault-code)**  
  If a page fault occurs.

- **#AC(0)**  
  If an unaligned memory reference occurs when the CPL is 3 and alignment checking is enabled.

- **#UD**  
  If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP**  
  If the return instruction pointer is not within the return code segment limit.

- **#SS**  
  If the top bytes of stack are not within stack limits.
Virtual-8086 Mode Exceptions

#GP(0) If the return instruction pointer is not within the return code segment limit.
   IF IOPL not equal to 3.
#PF(fault-code) If a page fault occurs.
#SS(0) If the top bytes of stack are not within stack limits.
#AC(0) If an unaligned memory reference occurs and alignment checking is enabled.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

#GP(0) If EFLAGS.NT[bit 14] = 1.
Other exceptions same as in Protected Mode.

64-Bit Mode Exceptions

#GP(0) If EFLAGS.NT[bit 14] = 1.
   If the return code segment selector is NULL.
   If the stack segment selector is NULL going back to compatibility mode.
   If the stack segment selector is NULL going back to CPL3 64-bit mode.
   If a NULL stack segment selector RPL is not equal to CPL going back to non-CPL3 64-bit mode.
   If the return instruction pointer is not within the return code segment limit.
   If the return instruction pointer is non-canonical.

#GP(Selector) If a segment selector index is outside its descriptor table limits.
   If a segment descriptor memory address is non-canonical.
   If the segment descriptor for a code segment does not indicate it is a code segment.
   If the proposed new code segment descriptor has both the D-bit and L-bit set.
   If the DPL for a nonconforming-code segment is not equal to the RPL of the code segment selector.
   If CPL is greater than the RPL of the code segment selector.
   If the DPL of a conforming-code segment is greater than the return code segment selector RPL.
   If the stack segment is not a writable data segment.
   If the stack segment descriptor DPL is not equal to the RPL of the return code segment selector.
If the stack segment selector RPL is not equal to the RPL of the return code segment selector.

#SS(0) If an attempt to pop a value off the stack violates the SS limit.
If an attempt to pop a value off the stack causes a non-canonical address to be referenced.

#NP(selector) If the return code or stack segment is not present.

#PF(fault-code) If a page fault occurs.

#AC(0) If an unaligned memory reference occurs when the CPL is 3 and alignment checking is enabled.

#UD If the LOCK prefix is used.
Jcc—Jump if Condition Is Met

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>77 cb</td>
<td>JA rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>73 cb</td>
<td>JAE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if above or equal (CF=0).</td>
</tr>
<tr>
<td>72 cb</td>
<td>JB rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if below (CF=1).</td>
</tr>
<tr>
<td>76 cb</td>
<td>JBE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>72 cb</td>
<td>JC rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if carry (CF=1).</td>
</tr>
<tr>
<td>E3 cb</td>
<td>JCXZ rel8</td>
<td>N.E.</td>
<td>Valid</td>
<td>Jump short if CX register is 0.</td>
</tr>
<tr>
<td>E3 cb</td>
<td>JECXZ rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if ECX register is 0.</td>
</tr>
<tr>
<td>E3 cb</td>
<td>JRCXZ rel8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Jump short if RCX register is 0.</td>
</tr>
<tr>
<td>74 cb</td>
<td>JE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if equal (ZF=1).</td>
</tr>
<tr>
<td>7F cb</td>
<td>JG rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if greater (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>7D cb</td>
<td>JGE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if greater or equal (SF=OF).</td>
</tr>
<tr>
<td>7C cb</td>
<td>JL rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if less (SF≠OF).</td>
</tr>
<tr>
<td>7E cb</td>
<td>JLE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if less or equal (ZF=1 or SF≠OF).</td>
</tr>
<tr>
<td>76 cb</td>
<td>JNA rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not above (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>72 cb</td>
<td>JNAE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not above or equal (CF=1).</td>
</tr>
<tr>
<td>73 cb</td>
<td>JNB rel8</td>
<td>Valid</td>
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<td>Jump short if not below (CF=0).</td>
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<tr>
<td>77 cb</td>
<td>JNBE rel8</td>
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<td>Valid</td>
<td>Jump short if not below or equal (CF=0 and ZF=0).</td>
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<td>73 cb</td>
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<td>Jump short if not carry (CF=0).</td>
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<tr>
<td>75 cb</td>
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</tr>
<tr>
<td>7E cb</td>
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<td>Valid</td>
<td>Jump short if not greater (ZF=1 or SF≠OF).</td>
</tr>
<tr>
<td>7C cb</td>
<td>JNGE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not greater or equal (SF≠OF).</td>
</tr>
<tr>
<td>7D cb</td>
<td>JNL rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not less (SF=OF).</td>
</tr>
<tr>
<td>7F cb</td>
<td>JNLE rel8</td>
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<td>Valid</td>
<td>Jump short if not less or equal (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>71 cb</td>
<td>JNO rel8</td>
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<td>Valid</td>
<td>Jump short if not overflow (OF=0).</td>
</tr>
<tr>
<td>7B cb</td>
<td>JNP rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not parity (PF=0).</td>
</tr>
<tr>
<td>79 cb</td>
<td>JNS rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not sign (SF=0).</td>
</tr>
</tbody>
</table>
## INSTRUCTION SET REFERENCE, A-M

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>75 cb</td>
<td>JNZ rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not zero (ZF=0).</td>
</tr>
<tr>
<td>70 cb</td>
<td>JO rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if overflow (OF=1).</td>
</tr>
<tr>
<td>7A cb</td>
<td>JP rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if parity (PF=1).</td>
</tr>
<tr>
<td>7A cb</td>
<td>JPE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if parity even (PF=1).</td>
</tr>
<tr>
<td>7B cb</td>
<td>JPO rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if parity odd (PF=0).</td>
</tr>
<tr>
<td>7B cb</td>
<td>JS rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if sign (SF=1).</td>
</tr>
<tr>
<td>74 cb</td>
<td>JZ rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if zero (ZF ← 1).</td>
</tr>
<tr>
<td>0F 87 cw</td>
<td>JA rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if above (CF=0 and ZF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 87 cd</td>
<td>JA rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>0F 83 cw</td>
<td>JAE rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if above or equal (CF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 83 cd</td>
<td>JAE rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if above or equal (CF=0).</td>
</tr>
<tr>
<td>0F 82 cw</td>
<td>JB rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if below (CF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 82 cd</td>
<td>JB rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if below (CF=1).</td>
</tr>
<tr>
<td>0F 86 cw</td>
<td>JBE rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if below or equal (CF=1 or ZF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 86 cd</td>
<td>JBE rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>0F 82 cw</td>
<td>JC rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if carry (CF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 82 cd</td>
<td>JC rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if carry (CF=1).</td>
</tr>
<tr>
<td>0F 84 cw</td>
<td>JE rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if equal (ZF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 84 cd</td>
<td>JE rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if equal (ZF=1).</td>
</tr>
<tr>
<td>0F 84 cw</td>
<td>JZ rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if 0 (ZF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 84 cd</td>
<td>JZ rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if 0 (ZF=1).</td>
</tr>
<tr>
<td>0F 8F cw</td>
<td>JG rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if greater (ZF=0 and SF=OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8F cd</td>
<td>JG rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if greater (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>0F 8D cw</td>
<td>JGE rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if greater or equal (SF=OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8D cd</td>
<td>JGE rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if greater or equal (SF=OF).</td>
</tr>
</tbody>
</table>

**Jcc—Jump if Condition Is Met**
**Jcc—Jump if Condition Is Met**

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<tr>
<th>Opcode</th>
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<tbody>
<tr>
<td>0F 8C cw</td>
<td>JL rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if less (SF ≠ OF). Not supported in 64-bit mode.</td>
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<td>0F 8C cd</td>
<td>JL rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if less (SF ≠ OF).</td>
</tr>
<tr>
<td>0F 8E cw</td>
<td>JLE rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if less or equal (ZF=1 or SF ≠ OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8E cd</td>
<td>JLE rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if less or equal (ZF=1 or SF ≠ OF).</td>
</tr>
<tr>
<td>0F 86 cw</td>
<td>JNA rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not above (CF=1 or ZF=1). Not supported in 64-bit mode.</td>
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<tr>
<td>0F 86 cd</td>
<td>JNA rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not above (CF=1 or ZF=1).</td>
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<tr>
<td>0F 82 cw</td>
<td>JNAE rel16</td>
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<td>Valid</td>
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<td>0F 82 cd</td>
<td>JNAE rel32</td>
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<td>Valid</td>
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<tr>
<td>0F 83 cw</td>
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<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not below (CF=0). Not supported in 64-bit mode.</td>
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<td>0F 83 cd</td>
<td>JNB rel32</td>
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<tr>
<td>0F 87 cw</td>
<td>JNBE rel16</td>
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<td>Jump near if not below or equal (CF=0 and ZF=0). Not supported in 64-bit mode.</td>
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<tr>
<td>0F 87 cd</td>
<td>JNBE rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not below or equal (CF=0 and ZF=0).</td>
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<tr>
<td>0F 83 cw</td>
<td>JNC rel16</td>
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<td>0F 83 cd</td>
<td>JNC rel32</td>
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<td>Valid</td>
<td>Jump near if not carry (CF=0).</td>
</tr>
<tr>
<td>0F 85 cw</td>
<td>JNE rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not equal (ZF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 85 cd</td>
<td>JNE rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not equal (ZF=0).</td>
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<tr>
<td>0F 8E cw</td>
<td>JNG rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not greater (ZF=1 or SF ≠ OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8E cd</td>
<td>JNG rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not greater (ZF=1 or SF ≠ OF).</td>
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<tr>
<td>0F 8C cw</td>
<td>JNGE rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not greater or equal (SF ≠ OF). Not supported in 64-bit mode.</td>
</tr>
</tbody>
</table>
## INSTRUCTION SET REFERENCE, A-M

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
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<tbody>
<tr>
<td>0F 8C cd</td>
<td>JNGE rel32</td>
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<td>Valid</td>
<td>Jump near if not greater or equal (SF≠OF).</td>
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<td>0F 8D cd</td>
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<td>Jump near if not less or equal (ZF=0 and SF=OF). Not supported in 64-bit mode.</td>
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<tr>
<td>0F 8F cd</td>
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<td>Valid</td>
<td>Jump near if not less or equal (ZF=0 and SF=OF).</td>
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<tr>
<td>0F 81 cw</td>
<td>JNO rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not overflow (OF=0). Not supported in 64-bit mode.</td>
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<tr>
<td>0F 81 cd</td>
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<td>Valid</td>
<td>Jump near if not overflow (OF=0).</td>
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<tr>
<td>0F 8B cw</td>
<td>JNP rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not parity (PF=0). Not supported in 64-bit mode.</td>
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<td>JNP rel32</td>
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<td>Jump near if not parity (PF=0).</td>
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<tr>
<td>0F 89 cw</td>
<td>JNS rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not sign (SF=0). Not supported in 64-bit mode.</td>
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<tr>
<td>0F 89 cd</td>
<td>JNS rel32</td>
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<td>Valid</td>
<td>Jump near if not sign (SF=0).</td>
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<tr>
<td>0F 85 cw</td>
<td>JNZ rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not zero (ZF=0). Not supported in 64-bit mode.</td>
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<tr>
<td>0F 85 cd</td>
<td>JNZ rel32</td>
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<td>Valid</td>
<td>Jump near if not zero (ZF=0).</td>
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<tr>
<td>0F 80 cw</td>
<td>JO rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if overflow (OF=1). Not supported in 64-bit mode.</td>
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<tr>
<td>0F 80 cd</td>
<td>JO rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if overflow (OF=1).</td>
</tr>
<tr>
<td>0F 8A cw</td>
<td>JP rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if parity (PF=1). Not supported in 64-bit mode.</td>
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<tr>
<td>0F 8A cd</td>
<td>JP rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if parity (PF=1).</td>
</tr>
<tr>
<td>0F 8A cw</td>
<td>JPE rel16</td>
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<td>0F 8A cd</td>
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<td>Valid</td>
<td>Jump near if parity even (PF=1).</td>
</tr>
<tr>
<td>0F 8B cw</td>
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<td>N.S.</td>
<td>Valid</td>
<td>Jump near if parity odd (PF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8B cd</td>
<td>JPO rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if parity odd (PF=0).</td>
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<tr>
<td>0F 88 cw</td>
<td>JS rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if sign (SF=1). Not supported in 64-bit mode.</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-M

Jcc—Jump if Condition Is Met

**Description**

Checks the state of one or more of the status flags in the EFLAGS register (CF, OF, PF, SF, and ZF) and, if the flags are in the specified state (condition), performs a jump to the target instruction specified by the destination operand. A condition code (cc) is associated with each instruction to indicate the condition being tested for. If the condition is not satisfied, the jump is not performed and execution continues with the instruction following the Jcc instruction.

The target instruction is specified with a relative offset (a signed offset relative to the current value of the instruction pointer in the EIP register). A relative offset (rel8, rel16, or rel32) is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed, 8-bit or 32-bit immediate value, which is added to the instruction pointer. Instruction coding is most efficient for offsets of –128 to +127. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared, resulting in a maximum instruction pointer size of 16 bits.

The conditions for each Jcc mnemonic are given in the “Description” column of the table on the preceding page. The terms “less” and “greater” are used for comparisons of signed integers and the terms “above” and “below” are used for unsigned integers.

Because a particular state of the status flags can sometimes be interpreted in two ways, two mnemonics are defined for some opcodes. For example, the JA (jump if above) instruction and the JNBE (jump if not below or equal) instruction are alternate mnemonics for the opcode 77H.

The Jcc instruction does not support far jumps (jumps to other code segments). When the target for the conditional jump is in a different segment, use the opposite condition from the condition being tested for the Jcc instruction, and then access the target with an unconditional far jump (JMP instruction) to the other segment. For example, the following conditional far jump is illegal:

```
JZ FARLABEL;
```

To accomplish this far jump, use the following two instructions:

```
JNZ BEYOND;
JMP FARLABEL;
BEYOND:
```

The JRCXZ, JECXZ and JCXZ instructions differ from other Jcc instructions because they do not check status flags. Instead, they check RCX, ECX or CX for 0. The register

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<tr>
<td>0F 88 cd</td>
<td>JS rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if sign (SF=1).</td>
</tr>
<tr>
<td>0F 84 cw</td>
<td>JZ rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if 0 (ZF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 84 cd</td>
<td>JZ rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if 0 (ZF=1).</td>
</tr>
</tbody>
</table>
checked is determined by the address-size attribute. These instructions are useful when used at the beginning of a loop that terminates with a conditional loop instruction (such as LOOPNE). They can be used to prevent an instruction sequence from entering a loop when RCX, ECX or CX is 0. This would cause the loop to execute $2^{64}$, $2^{32}$ or 64K times (not zero times).

All conditional jumps are converted to code fetches of one or two cache lines, regardless of jump address or cacheability.

In 64-bit mode, operand size is fixed at 64 bits. JMP Short is RIP = RIP + 8-bit offset sign extended to 64 bits. JMP Near is RIP = RIP + 32-bit offset sign extended to 64-bits.

**Operation**

IF condition

THEN

$$\text{tempEIP} \leftarrow \text{EIP} + \text{SignExtend} (\text{DEST})$$

IF OperandSize = 16

THEN $$\text{tempEIP} \leftarrow \text{tempEIP AND 0000FFFFH}$$

FI;

IF tempEIP is not within code segment limit

THEN #GP(0);

ELSE EIP $\leftarrow$ tempEIP

FI;

FI;

**Protected Mode Exceptions**

#GP(0) If the offset being jumped to is beyond the limits of the CS segment.

#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP If the offset being jumped to is beyond the limits of the CS segment or is outside of the effective address space from 0 to FFFFH. This condition can occur if a 32-bit address size override prefix is used.

#UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

Same exceptions as in real address mode.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.
#UD If the LOCK prefix is used.
JMP—Jump

### Description

Transfers program control to a different point in the instruction stream without recording return information. The destination (target) operand specifies the address of the instruction being jumped to. This operand can be an immediate value, a general-purpose register, or a memory location.

This instruction can be used to execute four different types of jumps:

- **Near jump**—A jump to an instruction within the current code segment (the segment currently pointed to by the CS register), sometimes referred to as an intrasegment jump.

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</tr>
</thead>
<tbody>
<tr>
<td>EB cb</td>
<td>JMP rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short, RIP = RIP + 8-bit displacement sign extended to 64-bits</td>
</tr>
<tr>
<td>E9 cw</td>
<td>JMP rel16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near, relative displacement relative to next instruction. Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>E9 cd</td>
<td>JMP rel32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near, relative, RIP = RIP + 32-bit displacement sign extended to 64-bits</td>
</tr>
<tr>
<td>FF /4</td>
<td>JMP r/m16</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near, absolute indirect, address = sign-extended r/m16. Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>FF /4</td>
<td>JMP r/m32</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near, absolute indirect, address = sign-extended r/m32. Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>FF /4</td>
<td>JMP r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Jump near, absolute indirect, RIP = 64-Bit offset from register or memory</td>
</tr>
<tr>
<td>EA cd</td>
<td>JMP ptr16:16</td>
<td>Inv.</td>
<td>Valid</td>
<td>Jump far, absolute, address given in operand</td>
</tr>
<tr>
<td>EA cp</td>
<td>JMP ptr16:32</td>
<td>Inv.</td>
<td>Valid</td>
<td>Jump far, absolute, address given in operand</td>
</tr>
<tr>
<td>FF /5</td>
<td>JMP m16:16</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump far, absolute indirect, address given in m16:16</td>
</tr>
<tr>
<td>FF /5</td>
<td>JMP m16:32</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump far, absolute indirect, address given in m16:32.</td>
</tr>
<tr>
<td>REX.W +</td>
<td>JMP m16:64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Jump far, absolute indirect, address given in m16:64.</td>
</tr>
</tbody>
</table>
JMP—Jump

- **Short jump**—A near jump where the jump range is limited to –128 to +127 from the current EIP value.
- **Far jump**—A jump to an instruction located in a different segment than the current code segment but at the same privilege level, sometimes referred to as an intersegment jump.
- **Task switch**—A jump to an instruction located in a different task.

A task switch can only be executed in protected mode (see Chapter 7, in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, for information on performing task switches with the JMP instruction).

**Near and Short Jumps.** When executing a near jump, the processor jumps to the address (within the current code segment) that is specified with the target operand. The target operand specifies either an absolute offset (that is an offset from the base of the code segment) or a relative offset (a signed displacement relative to the current value of the instruction pointer in the EIP register). A near jump to a relative offset of 8-bits (rel8) is referred to as a short jump. The CS register is not changed on near and short jumps.

An absolute offset is specified indirectly in a general-purpose register or a memory location (r/m16 or r/m32). The operand-size attribute determines the size of the target operand (16 or 32 bits). Absolute offsets are loaded directly into the EIP register. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared, resulting in a maximum instruction pointer size of 16 bits.

A relative offset (rel8, rel16, or rel32) is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed 8-, 16-, or 32-bit immediate value. This value is added to the value in the EIP register. (Here, the EIP register contains the address of the instruction following the JMP instruction). When using relative offsets, the opcode (for short vs. near jumps) and the operand-size attribute (for near relative jumps) determines the size of the target operand (8, 16, or 32 bits).

**Far Jumps in Real-Address or Virtual-8086 Mode.** When executing a far jump in real-address or virtual-8086 mode, the processor jumps to the code segment and offset specified with the target operand. Here the target operand specifies an absolute far address either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). With the pointer method, the segment and address of the called procedure is encoded in the instruction, using a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address immediate. With the indirect method, the target operand specifies a memory location that contains a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address immediate. The far address is loaded directly into the CS and EIP registers. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared.

**Far Jumps in Protected Mode.** When the processor is operating in protected mode, the JMP instruction can be used to perform the following three types of far jumps:

- A far jump to a conforming or non-conforming code segment.
- A far jump through a call gate.
• A task switch.

(The JMP instruction cannot be used to perform inter-privilege-level far jumps.)

In protected mode, the processor always uses the segment selector part of the far address to access the corresponding descriptor in the GDT or LDT. The descriptor type (code segment, call gate, task gate, or TSS) and access rights determine the type of jump to be performed.

If the selected descriptor is for a code segment, a far jump to a code segment at the same privilege level is performed. (If the selected code segment is at a different privilege level and the code segment is non-conforming, a general-protection exception is generated.) A far jump to the same privilege level in protected mode is very similar to one carried out in real-address or virtual-8086 mode. The target operand specifies an absolute far address either directly with a pointer ($ptr16:16$ or $ptr16:32$) or indirectly with a memory location ($m16:16$ or $m16:32$). The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The new code segment selector and its descriptor are loaded into CS register, and the offset from the instruction is loaded into the EIP register. Note that a call gate (described in the next paragraph) can also be used to perform far call to a code segment at the same privilege level. Using this mechanism provides an extra level of indirection and is the preferred method of making jumps between 16-bit and 32-bit code segments.

When executing a far jump through a call gate, the segment selector specified by the target operand identifies the call gate. (The offset part of the target operand is ignored.) The processor then jumps to the code segment specified in the call gate descriptor and begins executing the instruction at the offset specified in the call gate. No stack switch occurs. Here again, the target operand can specify the far address of the call gate either directly with a pointer ($ptr16:16$ or $ptr16:32$) or indirectly with a memory location ($m16:16$ or $m16:32$).

Executing a task switch with the JMP instruction is somewhat similar to executing a jump through a call gate. Here the target operand specifies the segment selector of the task gate for the task being switched to (and the offset part of the target operand is ignored). The task gate in turn points to the TSS for the task, which contains the segment selectors for the task’s code and stack segments. The TSS also contains the EIP value for the next instruction that was to be executed before the task was suspended. This instruction pointer value is loaded into the EIP register so that the task begins executing again at this next instruction.

The JMP instruction can also specify the segment selector of the TSS directly, which eliminates the indirection of the task gate. See Chapter 7 in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A, for detailed information on the mechanics of a task switch.

Note that when you execute a task switch with a JMP instruction, the nested task flag (NT) is not set in the EFLAGS register and the new TSS’s previous task link field is not loaded with the old task’s TSS selector. A return to the previous task can thus not be carried out by executing the IRET instruction. Switching tasks with the JMP instruction differs in this regard from the CALL instruction which does set the NT flag.
and save the previous task link information, allowing a return to the calling task with an IRET instruction.

**In 64-Bit Mode** — The instruction's operation size is fixed at 64 bits. If a selector points to a gate, then RIP equals the 64-bit displacement taken from gate; else RIP equals the zero-extended offset from the far pointer referenced in the instruction.

See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF near jump
  IF 64-bit Mode
    THEN
      IF near relative jump
        THEN
          tempRIP ← RIP + DEST; (* RIP is instruction following JMP instruction*)
        ELSE (* Near absolute jump *)
          tempRIP ← DEST;
        FI:
      ELSE
        IF near relative jump
          THEN
            tempEIP ← EIP + DEST; (* EIP is instruction following JMP instruction*)
          ELSE (* Near absolute jump *)
            tempEIP ← DEST;
          FI:
        FI;
  IF (IA32_EFER.LMA = 0 or target mode = Compatibility mode) and tempEIP outside code segment limit
    THEN #GP(0); FI
  IF 64-bit mode and tempRIP is not canonical
    THEN #GP(0);
  FI;
  IF OperandSize = 32
    THEN
      EIP ← tempEIP;
    ELSE
      IF OperandSize = 16
        THEN (* OperandSize = 16 *)
          EIP ← tempEIP AND 0000FFFFH;
        ELSE (* OperandSize = 64 *)
          RIP ← tempRIP;
        FI;
    FI;
INSTRUCTION SET REFERENCE, A-M

JMP—Jump

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THEN GP(new code segment selector); Fi;
IF DPL > CPL
    THEN #GP(segment selector); Fi;
IF segment not present
    THEN #NP(segment selector); Fi;
tempEIP ← DEST(Offset);
IF OperandSize = 16
    THEN tempEIP ← tempEIP AND 0000FFFFH;
   Fi;
IF (IA32_EFER.LMA = 0 or target mode = Compatibility mode) and
tempEIP outside code segment limit
    THEN #GP(0); Fi
IF tempEIP is non-canonical
    THEN #GP(0); Fi;
CS ← DEST(segment selector); (* Segment descriptor information also loaded *)
CS(RPL) ← CPL
EIP ← tempEIP;
END;
NONCONFORMING-CODE-SEGMENT:
IF L-Bit = 1 and D-BIT = 1 and IA32_EFER.LMA = 1
    THEN GP(new code segment selector); Fi;
IF (RPL > CPL) OR (DPL ≠ CPL)
    THEN #GP(code segment selector); Fi;
IF segment not present
    THEN #NP(segment selector); Fi;
tempEIP ← DEST(Offset);
IF OperandSize = 16
    THEN tempEIP ← tempEIP AND 0000FFFFH; Fi;
IF (IA32_EFER.LMA = 0 OR target mode = Compatibility mode)
and tempEIP outside code segment limit
    THEN #GP(0); Fi
IF tempEIP is non-canonical THEN #GP(0); Fi;
CS ← DEST(segment selector); (* Segment descriptor information also loaded *)
CS(RPL) ← CPL;
EIP ← tempEIP;
END;
CALL-GATE:
IF call gate DPL < CPL
or call gate DPL < call gate segment-selector RPL
    THEN #GP(call gate selector); Fi;
IF call gate not present
    THEN #NP(call gate selector); Fi;
IF call gate code-segment selector is NULL
INSTRUCTION SET REFERENCE, A-M

THEN #GP(0); Fl;
IF call gate code-segment selector index outside descriptor table limits
  THEN #GP(code segment selector); Fl;
Read code segment descriptor;
IF code-segment segment descriptor does not indicate a code segment
  or code-segment segment descriptor is conforming and DPL > CPL
  or code-segment segment descriptor is non-conforming and DPL ≠ CPL
    THEN #GP(code segment selector); Fl;
IF IA32_EFER.LMA = 1 and (code-segment descriptor is not a 64-bit code segment
  or code-segment segment descriptor has both L-Bit and D-bit set)
    THEN #GP(code segment selector); Fl;
IF code segment is not present
    THEN #NP(code-segment selector); Fl;
IF instruction pointer is not within code-segment limit
    THEN #GP(0); Fl;
tempEIP ← DEST(Offset);
IF GateSize = 16
    THEN tempEIP ← tempEIP AND 0000FFFFH; Fl;
IF (IA32_EFER.LMA = 0 OR target mode = Compatibility mode) AND tempEIP
  outside code segment limit
    THEN #GP(0); Fl;
CS ← DEST[SegmentSelector]; (* Segment descriptor information also loaded *)
CS(RPL) ← CPL;
EIP ← tempEIP;
END;
TASK-GATE:
IF task gate DPL < CPL
  or task gate DPL < task gate segment-selector RPL
    THEN #GP(task gate selector); Fl;
IF task gate not present
    THEN #NP(task gate selector); Fl;
Read the TSS segment selector in the task-gate descriptor;
IF TSS segment selector local/global bit is set to local
  or index not within GDT limits
or TSS descriptor specifies that the TSS is busy
    THEN #GP(TSS selector); Fl;
IF TSS not present
    THEN #NP(TSS selector); Fl;
SWITCH-TASKS to TSS;
IF EIP not within code segment limit
    THEN #GP(0); Fl;
END;
TASK-STATE-SEGMENT:
IF TSS DPL < CPL

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or TSS DPL < TSS segment-selector RPL
or TSS descriptor indicates TSS not available
THEN #GP(TSS selector); FI;
IF TSS is not present
THEN #NP(TSS selector); FI;
SWITCH-TASKS to TSS;
IF EIP not within code segment limit
THEN #GP(0); FI;
END;

Flags Affected
All flags are affected if a task switch occurs; no flags are affected if a task switch does not occur.

Protected Mode Exceptions
#GP(0) If offset in target operand, call gate, or TSS is beyond the code segment limits.
If the segment selector in the destination operand, call gate, task gate, or TSS is NULL.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#GP(selector) If the segment selector index is outside descriptor table limits.
If the segment descriptor pointed to by the segment selector in the destination operand is not for a conforming-code segment, nonconforming-code segment, call gate, task gate, or task state segment.
If the DPL for a nonconforming-code segment is not equal to the CPL
(When not using a call gate.) If the RPL for the segment’s segment selector is greater than the CPL.
If the DPL for a conforming-code segment is greater than the CPL.
If the DPL from a call-gate, task-gate, or TSS segment descriptor is less than the CPL or than the RPL of the call-gate, task-gate, or TSS’s segment selector.
If the segment descriptor for selector in a call gate does not indicate it is a code segment.
If the segment descriptor for the segment selector in a task gate does not indicate an available TSS.
If the segment selector for a TSS has its local/global bit set for local.
If a TSS segment descriptor specifies that the TSS is busy or not available.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NP (selector) If the code segment being accessed is not present.
If call gate, task gate, or TSS not present.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3. (Only occurs when fetching target from memory.)

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If the target operand is beyond the code segment limits.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made. (Only occurs when fetching target from memory.)

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same as 64-bit mode exceptions.

64-Bit Mode Exceptions

#GP(0) If a memory address is non-canonical.
JMP—Jump

If target offset in destination operand is non-canonical.
If target offset in destination operand is beyond the new code segment limit.
If the segment selector in the destination operand is NULL.
If the code segment selector in the 64-bit gate is NULL.

#GP(selector)
If the code segment or 64-bit call gate is outside descriptor table limits.
If the code segment or 64-bit call gate overlaps non-canonical space.
If the segment descriptor from a 64-bit call gate is in non-canonical space.
If the segment descriptor pointed to by the segment selector in the destination operand is not for a conforming-code segment, nonconforming-code segment, 64-bit call gate.
If the segment descriptor pointed to by the segment selector in the destination operand is a code segment, and has both the D-bit and the L-bit set.
If the DPL for a nonconforming-code segment is not equal to the CPL, or the RPL for the segment’s segment selector is greater than the CPL.
If the DPL for a conforming-code segment is greater than the CPL.
If the DPL from a 64-bit call-gate is less than the CPL or than the RPL of the 64-bit call-gate.
If the upper type field of a 64-bit call gate is not 0x0.
If the segment selector from a 64-bit call gate is beyond the descriptor table limits.
If the code segment descriptor pointed to by the selector in the 64-bit gate doesn't have the L-bit set and the D-bit clear.
If the segment descriptor for a segment selector from the 64-bit call gate does not indicate it is a code segment.
If the code segment is non-confirming and CPL ≠ DPL.
If the code segment is confirming and CPL < DPL.

#NP(selector)
If a code segment or 64-bit call gate is not present.

#UD
(64-bit mode only) If a far jump is direct to an absolute address in memory.
If the LOCK prefix is used.

#PF(fault-code)
If a page fault occurs.

#AC(0)
If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
LAHF—Load Status Flags into AH Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
</table>

**NOTES:**
* Valid in specific stepping. See Description section.

**Description**
This instruction executes as described above in compatibility mode and legacy mode. It is valid in 64-bit mode only if CPUID.80000001H:ECX.LAHF-SAHF[bit 0] = 1.

**Operation**
IF 64-Bit Mode
THEN
    IF CPUID.80000001H:ECX.LAHF-SAHF[bit 0] = 1;
    THEN AH ← RFLAGS(SF:ZF:0:AF:0:PF:1:CF);
    ELSE #UD;
    FI;
ELSE
    AH ← EFLAGS(SF:ZF:0:AF:0:PF:1:CF);
FI;

**Flags Affected**
None. The state of the flags in the EFLAGS register is not affected.

**Protected Mode Exceptions**
#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**
Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**
Same exceptions as in protected mode.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.
64-Bit Mode Exceptions

#UD  If CPUID.80000001H:ECX.LAHF-SAHF[bit 0] = 0.
     If the LOCK prefix is used.
LAR—Load Access Rights Byte

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 02</td>
<td>LAR r16, r16/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>( r16 \leftarrow r16/m16 ) masked by FF00H.</td>
</tr>
<tr>
<td>0F 02</td>
<td>LAR r32, r32/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>( r32 \leftarrow r32/m16 ) masked by 00FF00H</td>
</tr>
<tr>
<td>REX.W +</td>
<td>LAR r64, r32/m16</td>
<td>Valid</td>
<td>N.E.</td>
<td>( r64 \leftarrow r32/m16 ) masked by 00FF00H and zero extended</td>
</tr>
</tbody>
</table>

NOTES:
1. For all loads (regardless of source or destination sizing) only bits 16-0 are used. Other bits are ignored.

Description

Loads the access rights from the segment descriptor specified by the second operand (source operand) into the first operand (destination operand) and sets the ZF flag in the flag register. The source operand (which can be a register or a memory location) contains the segment selector for the segment descriptor being accessed. If the source operand is a memory address, only 16 bits of data are accessed. The destination operand is a general-purpose register.

The processor performs access checks as part of the loading process. Once loaded in the destination register, software can perform additional checks on the access rights information.

When the operand size is 32 bits, the access rights for a segment descriptor include the type and DPL fields and the S, P, AVL, D/B, and G flags, all of which are located in the second doubleword (bytes 4 through 7) of the segment descriptor. The doubleword is masked by 00FF00H before it is loaded into the destination operand. When the operand size is 16 bits, the access rights include the type and DPL fields. Here, the two lower-order bytes of the doubleword are masked by FF00H before being loaded into the destination operand.

This instruction performs the following checks before it loads the access rights in the destination register:
- Checks that the segment selector is not NULL.
- Checks that the segment selector points to a descriptor that is within the limits of the GDT or LDT being accessed
- Checks that the descriptor type is valid for this instruction. All code and data segment descriptors are valid for (can be accessed with) the LAR instruction. The valid system segment and gate descriptor types are given in Table 3-65.
• If the segment is not a conforming code segment, it checks that the specified segment descriptor is visible at the CPL (that is, if the CPL and the RPL of the segment selector are less than or equal to the DPL of the segment selector).

If the segment descriptor cannot be accessed or is an invalid type for the instruction, the ZF flag is cleared and no access rights are loaded in the destination operand.

The LAR instruction can only be executed in protected mode and IA-32e mode.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.W prefix permits access to 64-bit registers as destination.

When the destination operand size is 64 bits, the access rights are loaded from the second doubleword (bytes 4 through 7) of the segment descriptor. The doubleword is masked by 00FXFF00H and zero extended to 64 bits before it is loaded into the destination operand.

<table>
<thead>
<tr>
<th>Type</th>
<th>Protected Mode</th>
<th>IA-32e Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Valid</td>
<td>Name</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>Available 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>LDT</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>Busy 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>16-bit call gate</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>16-bit/32-bit task gate</td>
<td>Yes</td>
</tr>
<tr>
<td>6</td>
<td>16-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>7</td>
<td>16-bit trap gate</td>
<td>No</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>9</td>
<td>Available 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>A</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>B</td>
<td>Busy 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>C</td>
<td>32-bit call gate</td>
<td>Yes</td>
</tr>
<tr>
<td>D</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>E</td>
<td>32-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>F</td>
<td>32-bit trap gate</td>
<td>No</td>
</tr>
</tbody>
</table>

### Operation

\[
\text{IF Offset(SRC)} > \text{descriptor table limit}
\]

THEN

LAR—Load Access Rights Byte
ZF = 0;
ELSE
    IF SegmentDescriptor(Type) ≠ conforming code segment
    and (CPL > DPL) or (RPL > DPL)
    or segment type is not valid for instruction
    THEN
    ZF ← 0
    ELSE
    TEMP ← Read segment descriptor;
    IF OperandSize = 64
    THEN
    DEST ← (ACCESSRIGHTWORD(TEMP) AND 00000000_00FxFF00H);
    ELSE (* OperandSize = 32*)
    DEST ← (ACCESSRIGHTWORD(TEMP) AND 00FxFF00H);
    ELSE (* OperandSize = 16 *)
    DEST ← (ACCESSRIGHTWORD(TEMP) AND FF00H);
    FI;
    FI;
FI:

Flags Affected
The ZF flag is set to 1 if the access rights are loaded successfully; otherwise, it is set to 0.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and the memory operand effective address is unaligned while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD The LAR instruction is not recognized in real-address mode.
Virtual-8086 Mode Exceptions
#UD The LAR instruction cannot be executed in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If the memory operand effective address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory operand effective address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and the memory operand effective address is unaligned while the current privilege level is 3.
#UD If the LOCK prefix is used.
LDDQU—Load Unaligned Integer 128 Bits

Description

The instruction is functionally similar to MOVDQU xmm, m128 for loading from memory. That is: 16 bytes of data starting at an address specified by the source memory operand (second operand) are fetched from memory and placed in a destination register (first operand). The source operand need not be aligned on a 16-byte boundary. Up to 32 bytes may be loaded from memory; this is implementation dependent.

This instruction may improve performance relative to MOVDQU if the source operand crosses a cache line boundary. In situations that require the data loaded by LDDQU be modified and stored to the same location, use MOVDQU or MOVDQA instead of LDDQU. To move a double quadword to or from memory locations that are known to be aligned on 16-byte boundaries, use the MOVDQA instruction.

Implementation Notes

• If the source is aligned to a 16-byte boundary, based on the implementation, the 16 bytes may be loaded more than once. For that reason, the usage of LDDQU should be avoided when using uncached or write-combining (WC) memory regions. For uncached or WC memory regions, keep using MOVDQU.

• This instruction is a replacement for MOVDQU (load) in situations where cache line splits significantly affect performance. It should not be used in situations where store-load forwarding is performance critical. If performance of store-load forwarding is critical to the application, use MOVDQA store-load pairs when data is 128-bit aligned or MOVDQU store-load pairs when data is 128-bit unaligned.

• If the memory address is not aligned on 16-byte boundary, some implementations may load up to 32 bytes and return 16 bytes in the destination. Some processor implementations may issue multiple loads to access the appropriate 16 bytes. Developers of multi-threaded or multi-processor software should be aware that on these processors the loads will be performed in a non-atomic way.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

\[ \text{xmm}[127:0] = \text{m128}; \]
Intel C/C++ Compiler Intrinsic Equivalent
LDDQU __m128i _mm_lddqu_si128(__m128i const *p)

Numeric Exceptions
None.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.

Virtual 8086 Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
#PF(fault-code) If a page fault occurs.
LDMXCSR—Load MXCSR Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,AE/2</td>
<td>LDMXCSR m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Load MXCSR register from m32.</td>
</tr>
</tbody>
</table>

Description

Loads the source operand into the MXCSR control/status register. The source operand is a 32-bit memory location. See “MXCSR Control and Status Register” in Chapter 10, of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a description of the MXCSR register and its contents.

The LDMXCSR instruction is typically used in conjunction with the STMXCSR instruction, which stores the contents of the MXCSR register in memory.

The default MXCSR value at reset is 1F80H.

If a LDMXCSR instruction clears a SIMD floating-point exception mask bit and sets the corresponding exception flag bit, a SIMD floating-point exception will not be immediately generated. The exception will be generated only upon the execution of the next SSE or SSE2 instruction that causes that particular SIMD floating-point exception to be reported.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

MXCSR ← m32;

C/C++ Compiler Intrinsic Equivalent

_mmx_setcsr(unsigned int i)

Numeric Exceptions

None.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
For an attempt to set reserved bits in MXCSR.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
LDMXCSR—Load MXCSR Register

INSTRUCTION SET REFERENCE, A-M

If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to FFFFH.
For an attempt to set reserved bits in MXCSR.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual 8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
For an attempt to set reserved bits in MXCSR.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
LDS/LES/LFS/LGS/LSS—Load Far Pointer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C5 /r</td>
<td>LDS</td>
<td>Invalid</td>
<td>Valid</td>
<td>Load DS:r16 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r16,m16:16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C5 /r</td>
<td>LDS</td>
<td>Invalid</td>
<td>Valid</td>
<td>Load DS:r32 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r32,m16:32</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF B2 /r</td>
<td>LSS</td>
<td>Valid</td>
<td>Valid</td>
<td>Load SS:r16 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r16,m16:16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF B2 /r</td>
<td>LSS</td>
<td>Valid</td>
<td>Valid</td>
<td>Load SS:r32 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r32,m16:32</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REX + OF B2 /r</td>
<td>LSS</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load SS:r64 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r64,m16:64</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C4 /r</td>
<td>LES</td>
<td>Invalid</td>
<td>Valid</td>
<td>Load ES:r16 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r16,m16:16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C4 /r</td>
<td>LES</td>
<td>Invalid</td>
<td>Valid</td>
<td>Load ES:r32 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r32,m16:32</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF B4 /r</td>
<td>LFS</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FS:r16 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r16,m16:16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF B4 /r</td>
<td>LFS</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FS:r32 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r32,m16:32</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REX + OF B4 /r</td>
<td>LFS</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load FS:r64 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r64,m16:64</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF B5 /r</td>
<td>LGS</td>
<td>Valid</td>
<td>Valid</td>
<td>Load GS:r16 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r16,m16:16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF B5 /r</td>
<td>LGS</td>
<td>Valid</td>
<td>Valid</td>
<td>Load GS:r32 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r32,m16:32</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REX + OF B5 /r</td>
<td>LGS</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load GS:r64 with far pointer from memory.</td>
</tr>
<tr>
<td></td>
<td>r64,m16:64</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Description

Loads a far pointer (segment selector and offset) from the second operand (source operand) into a segment register and the first operand (destination operand). The source operand specifies a 48-bit or a 32-bit pointer in memory depending on the current setting of the operand-size attribute (32 bits or 16 bits, respectively). The instruction opcode and the destination operand specify a segment register/general-purpose register pair. The 16-bit segment selector from the source operand is loaded into the segment register specified with the opcode (DS, SS, ES, FS, or GS). The 32-bit or 16-bit offset is loaded into the register specified with the destination operand.
INSTRUCTION SET REFERENCE, A-M

If one of these instructions is executed in protected mode, additional information from the segment descriptor pointed to by the segment selector in the source operand is loaded in the hidden part of the selected segment register.

Also in protected mode, a NULL selector (values 0000 through 0003) can be loaded into DS, ES, FS, or GS registers without causing a protection exception. (Any subsequent reference to a segment whose corresponding segment register is loaded with a NULL selector, causes a general-protection exception (#GP) and no memory reference to the segment occurs.)

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.W promotes operation to specify a source operand referencing an 80-bit pointer (16-bit selector, 64-bit offset) in memory. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). See the summary chart at the beginning of this section for encoding data and limits.

Operation

64-BIT_MODE
IF SS is loaded
THEN
  IF SegmentSelector = NULL and ( (RPL = 3) or (RPL ≠ 3 and RPL ≠ CPL) )
  THEN #GP(0);
  ELSE IF descriptor is in non-canonical space
  THEN #GP(0); FI;
  ELSE IF Segment selector index is not within descriptor table limits
    or segment selector RPL ≠ CPL
    or access rights indicate nonwritable data segment
    or DPL ≠ CPL
  THEN #GP(selector); FI;
  ELSE IF Segment marked not present
  THEN #SS(selector); FI;
  FI;
  SS ← SegmentSelector(SRC);
  SS ← SegmentDescriptor([SRC]);
ELSE IF attempt to load DS, or ES
  THEN #UD;
ELSE IF FS, or GS is loaded with non-NUL segment selector
  THEN IF Segment selector index is not within descriptor table limits
    or access rights indicate segment neither data nor readable code segment
    or segment is data or nonconforming-code segment
    and ( RPL > DPL or CPL > DPL )
  THEN #GP(selector); FI;
  ELSE IF Segment marked not present
  THEN #NP(selector); FI;
LDS/LES/LFS/LGS/LSS—Load Far Pointer

**INSTRUCTION SET REFERENCE, A-M**

FI;
SegmentRegister ← SegmentSelector(SRC);
SegmentRegister ← SegmentDescriptor([SRC]);
FI;
ELSE IF FS, or GS is loaded with a NULL selector:
THEN
SegmentRegister ← NULLSelector;
SegmentRegister(DescriptorValidBit) ← 0; FI; (* Hidden flag; not accessible by software *)
FI;
DEST ← Offset(SRC);

PRETENDED MODE OR COMPATIBILITY MODE;
IF SS is loaded
THEN
IF SegmentSelector = NULL
THEN #GP(0);
ELSE IF Segment selector index is not within descriptor table limits
or segment selector RPL \neq CPL
or access rights indicate nonwritable data segment
or DPL \neq CPL
THEN #GP(selector); FI;
ELSE IF Segment marked not present
THEN #SS(selector); FI;
FI;
SS ← SegmentSelector(SRC);
SS ← SegmentDescriptor([SRC]);
ELSE IF DS, ES, FS, or GS is loaded with non-NULL segment selector
THEN IF Segment selector index is not within descriptor table limits
or access rights indicate segment neither data nor readable code segment
or segment is data or nonconforming-code segment
and (RPL > DPL or CPL > DPL)
THEN #GP(selector); FI;
ELSE IF Segment marked not present
THEN #NP(selector); FI;
FI;
SegmentRegister ← SegmentSelector(SRC) AND RPL;
SegmentRegister ← SegmentDescriptor([SRC]);
FI;
ELSE IF DS, ES, FS, or GS is loaded with a NULL selector:
THEN
SegmentRegister ← NULLSelector;
SegmentRegister(DescriptorValidBit) ← 0; FI; (* Hidden flag; not accessible by software *)
INSTRUCTION SET REFERENCE, A-M

FI;
DEST ← Offset(SRC);

Real-Address or Virtual-8086 Mode
SegmentRegister ← SegmentSelector(SRC); FI;
DEST ← Offset(SRC);

Flags Affected
None.

Protected Mode Exceptions
#UD If source operand is not a memory location.
   If the LOCK prefix is used.
#GP(0) If a NULL selector is loaded into the SS register.
   If a memory operand effective address is outside the CS, DS,
   ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register is used to access memory and it
   contains a NULL segment selector.
#GP(selector) If the SS register is being loaded and any of the following is true:
   the segment selector index is not within the descriptor table
   limits, the segment selector RPL is not equal to CPL, the
   segment is a non-writable data segment, or DPL is not equal to
   CPL.
   If the DS, ES, FS, or GS register is being loaded with a non-NULL
   segment selector and any of the following is true: the segment
   selector index is not within descriptor table limits, the segment
   is neither a data nor a readable code segment, or the segment is
   a data or nonconforming-code segment and both RPL and CPL
   are greater than DPL.
#SS(0) If a memory operand effective address is outside the SS
   segment limit.
#SS(selector) If the SS register is being loaded and the segment is marked not
   present.
#NP(selector) If DS, ES, FS, or GS register is being loaded with a non-NULL
   segment selector and the segment is marked not present.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory
   reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS,
   ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
#UD  If source operand is not a memory location.
    If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#UD  If source operand is not a memory location.
    If the LOCK prefix is used.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#GP(0) If the memory address is in a non-canonical form.
    If a NULL selector is attempted to be loaded into the SS register in compatibility mode.
    If a NULL selector is attempted to be loaded into the SS register in CPL3 and 64-bit mode.
    If a NULL selector is attempted to be loaded into the SS register in non-CPL3 and 64-bit mode where its RPL is not equal to CPL.
#GP(Selector) If the FS, or GS register is being loaded with a non-NULL segment selector and any of the following is true: the segment selector index is not within descriptor table limits, the memory address of the descriptor is non-canonical, the segment is neither a data nor a readable code segment, or the segment is a data or nonconforming-code segment and both RPL and CPL are greater than DPL.
    If the SS register is being loaded and any of the following is true: the segment selector index is not within the descriptor table limits, the memory address of the descriptor is non-canonical, the segment selector RPL is not equal to CPL, the segment is a nonwritable data segment, or DPL is not equal to CPL.
#SS(0)  If a memory operand effective address is non-canonical
#SS(Selector)  If the SS register is being loaded and the segment is marked not present.
INSTRUCTION SET REFERENCE, A-M

#NP(selector)   If FS, or GS register is being loaded with a non-NULL segment selector and the segment is marked not present.

#PF(fault-code) If a page fault occurs.

#AC(0)   If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD   If source operand is not a memory location.
   If the LOCK prefix is used.
LEA—Load Effective Address

**Description**
Computes the effective address of the second operand (the source operand) and stores it in the first operand (destination operand). The source operand is a memory address (offset part) specified with one of the processors addressing modes; the destination operand is a general-purpose register. The address-size and operand-size attributes affect the action performed by this instruction, as shown in the following table. The operand-size attribute of the instruction is determined by the chosen register; the address-size attribute is determined by the attribute of the code segment.

**Table 3-66. Non-64-bit Mode LEA Operation with Address and Operand Size Attributes**

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Address Size</th>
<th>Action Performed</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>16</td>
<td>16-bit effective address is calculated and stored in requested 16-bit register destination.</td>
</tr>
<tr>
<td>16</td>
<td>32</td>
<td>32-bit effective address is calculated. The lower 16 bits of the address are stored in the requested 16-bit register destination.</td>
</tr>
<tr>
<td>32</td>
<td>16</td>
<td>16-bit effective address is calculated. The 16-bit address is zero-extended and stored in the requested 32-bit register destination.</td>
</tr>
<tr>
<td>32</td>
<td>32</td>
<td>32-bit effective address is calculated and stored in the requested 32-bit register destination.</td>
</tr>
</tbody>
</table>

Different assemblers may use different algorithms based on the size attribute and symbolic reference of the source operand.

In 64-bit mode, the instruction’s destination operand is governed by operand size attribute, the default operand size is 32 bits. Address calculation is governed by address size attribute, the default address size is 64-bits. In 64-bit mode, address size of 16 bits is not encodable. See Table 3-67.
Table 3-67. 64-bit Mode LEA Operation with Address and Operand Size Attributes

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Address Size</th>
<th>Action Performed</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>32</td>
<td>32-bit effective address is calculated (using 67H prefix). The lower 16 bits of the address are stored in the requested 16-bit register destination (using 66H prefix).</td>
</tr>
<tr>
<td>16</td>
<td>64</td>
<td>64-bit effective address is calculated (default address size). The lower 16 bits of the address are stored in the requested 16-bit register destination (using 66H prefix).</td>
</tr>
<tr>
<td>32</td>
<td>32</td>
<td>32-bit effective address is calculated (using 67H prefix) and stored in the requested 32-bit register destination.</td>
</tr>
<tr>
<td>32</td>
<td>64</td>
<td>64-bit effective address is calculated (default address size) and the lower 32 bits of the address are stored in the requested 32-bit register destination.</td>
</tr>
<tr>
<td>64</td>
<td>32</td>
<td>32-bit effective address is calculated (using 67H prefix), zero-extended to 64-bits, and stored in the requested 64-bit register destination (using REX.W).</td>
</tr>
<tr>
<td>64</td>
<td>64</td>
<td>64-bit effective address is calculated (default address size) and all 64-bits of the address are stored in the requested 64-bit register destination (using REX.W).</td>
</tr>
</tbody>
</table>

Operation

IF OperandSize = 16 and AddressSize = 16
THEN
    DEST ← EffectiveAddress(SRC); (* 16-bit address *)
ELSE IF OperandSize = 16 and AddressSize = 32
THEN
    temp ← EffectiveAddress(SRC); (* 32-bit address *)
    DEST ← temp[0:15]; (* 16-bit address *)
FI;
ELSE IF OperandSize = 32 and AddressSize = 16
THEN
    temp ← EffectiveAddress(SRC); (* 16-bit address *)
    DEST ← ZeroExtend(temp); (* 32-bit address *)
FI;
ELSE IF OperandSize = 32 and AddressSize = 32
THEN
    DEST ← EffectiveAddress(SRC); (* 32-bit address *)
FI;
ELSE IF OperandSize = 16 and AddressSize = 64
THEN
    temp ← EffectiveAddress(SRC); (* 64-bit address *)
LEA—Load Effective Address

DEST ← temp[0:15]; (* 16-bit address *)
FI;
ELSE IF OperandSize = 32 and AddressSize = 64
THEN
    temp ← EffectiveAddress(SRC); (* 64-bit address *)
    DEST ← temp[0:31]; (* 16-bit address *)
FI;
ELSE IF OperandSize = 64 and AddressSize = 64
THEN
    DEST ← EffectiveAddress(SRC); (* 64-bit address *)
FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#UD If source operand is not a memory location.
    If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
LEAVE—High Level Procedure Exit

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C9</td>
<td>LEAVE</td>
<td>Valid</td>
<td>Valid</td>
<td>Set SP to BP, then pop BP.</td>
</tr>
<tr>
<td>C9</td>
<td>LEAVE</td>
<td>N.E.</td>
<td>Valid</td>
<td>Set ESP to EBP, then pop EBP.</td>
</tr>
<tr>
<td>C9</td>
<td>LEAVE</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set RSP to RBP, then pop RBP.</td>
</tr>
</tbody>
</table>

Description

Releases the stack frame set up by an earlier ENTER instruction. The LEAVE instruction copies the frame pointer (in the EBP register) into the stack pointer register (ESP), which releases the stack space allocated to the stack frame. The old frame pointer (the frame pointer for the calling procedure that was saved by the ENTER instruction) is then popped from the stack into the EBP register, restoring the calling procedure’s stack frame.

A RET instruction is commonly executed following a LEAVE instruction to return program control to the calling procedure.

See “Procedure Calls for Block-Structured Languages” in Chapter 7 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for detailed information on the use of the ENTER and LEAVE instructions.

In 64-bit mode, the instruction’s default operation size is 64 bits; 32-bit operation cannot be encoded. See the summary chart at the beginning of this section for encoding data and limits.

Operation

IF StackAddressSize = 32
    THEN
        ESP ← EBP;
        ELSE IF StackAddressSize = 64
            THEN RSP ← RBP; FI;
        ELSE IF StackAddressSize = 16
            THEN SP ← BP; FI;
        FI;
    FI;

IF OperandSize = 32
    THEN EBP ← Pop();
    ELSE IF OperandSize = 64
        THEN RBP ← Pop(); FI;
    ELSE IF OperandSize = 16
        THEN BP ← Pop(); FI;
    FI;
Flags Affected
None.

Protected Mode Exceptions
#SS(0) If the EBP register points to a location that is not within the limits of the current stack segment.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If the EBP register points to a location outside of the effective address space from 0 to FFFFH.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If the EBP register points to a location outside of the effective address space from 0 to FFFFH.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If the stack address is in a non-canonical form.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
LFENCE—Load Fence

Description
Performs a serializing operation on all load-from-memory instructions that were issued prior the LFENCE instruction. This serializing operation guarantees that every load instruction that precedes in program order the LFENCE instruction is globally visible before any load instruction that follows the LFENCE instruction is globally visible. The LFENCE instruction is ordered with respect to load instructions, other LFENCE instructions, any MFENCE instructions, and any serializing instructions (such as the CPUID instruction). It is not ordered with respect to store instructions or the SFENCE instruction.

Weakly ordered memory types can be used to achieve higher processor performance through such techniques as out-of-order issue and speculative reads. The degree to which a consumer of data recognizes or knows that the data is weakly ordered varies among applications and may be unknown to the producer of this data. The LFENCE instruction provides a performance-efficient way of insuring load ordering between routines that produce weakly-ordered results and routines that consume that data.

It should be noted that processors are free to speculatively fetch and cache data from system memory regions that are assigned a memory-type that permits speculative reads (that is, the WB, WC, and WT memory types). The PREFETCHh instruction is considered a hint to this speculative behavior. Because this speculative fetching can occur at any time and is not tied to instruction execution, the LFENCE instruction is not ordered with respect to PREFETCHh instructions or any other speculative fetching mechanism (that is, data could be speculative loaded into the cache just before, during, or after the execution of an LFENCE instruction).

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
Wait_On_Following_Loads_Until(preceding_loads_globally_visible);

Intel C/C++ Compiler Intrinsic Equivalent
void _mm_lfence(void)

Exceptions (All Modes of Operation)
#UD If the LOCK prefix is used.
**Description**

Loads the values in the source operand into the global descriptor table register (GDTR) or the interrupt descriptor table register (IDTR). The source operand specifies a 6-byte memory location that contains the base address (a linear address) and the limit (size of table in bytes) of the global descriptor table (GDT) or the interrupt descriptor table (IDT). If operand-size attribute is 32 bits, a 16-bit limit (lower 2 bytes of the 6-byte data operand) and a 32-bit base address (upper 4 bytes of the data operand) are loaded into the register. If the operand-size attribute is 16 bits, a 16-bit limit (lower 2 bytes) and a 24-bit base address (third, fourth, and fifth byte) are loaded. Here, the high-order byte of the operand is not used and the high-order byte of the base address in the GDTR or IDTR is filled with zeros.

The LGDT and LIDT instructions are used only in operating-system software; they are not used in application programs. They are the only instructions that directly load a linear address (that is, not a segment-relative address) and a limit in protected mode. They are commonly executed in real-address mode to allow processor initialization prior to switching to protected mode.

In 64-bit mode, the instruction’s operand size is fixed at 8+2 bytes (an 8-byte base and a 2-byte limit). See the summary chart at the beginning of this section for encoding data and limits.

See “SGDT—Store Global Descriptor Table Register” in Chapter 4, *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*, for information on storing the contents of the GDTR and IDTR.

**Operation**

IF Instruction is LIDT
THEN
    IF OperandSize = 16
    THEN
        IDTR(Limit) ← SRC[0:15];
        IDTR(Base) ← SRC[16:47] AND 00FFFFFFH;
    ELSE IF 32-bit Operand Size
    THEN

**LGDT/LIDT**—Load Global/Interrupt Descriptor Table Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 /2</td>
<td>LGDT m16&amp;32</td>
<td>N.E.</td>
<td>Valid</td>
<td>Load m into GDTR.</td>
</tr>
<tr>
<td>0F 01 /3</td>
<td>LIDT m16&amp;32</td>
<td>N.E.</td>
<td>Valid</td>
<td>Load m into IDTR.</td>
</tr>
<tr>
<td>0F 01 /2</td>
<td>LGDT m16&amp;64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load m into GDTR.</td>
</tr>
<tr>
<td>0F 01 /3</td>
<td>LIDT m16&amp;64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load m into IDTR.</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-M

```
IDTR(Limit) ← SRC[0:15];
IDTR(Base) ← SRC[16:47];
FI;
ELSE IF 64-bit Operand Size (* In 64-Bit Mode *)
THEN
  IDTR(Limit) ← SRC[0:15];
  IDTR(Base) ← SRC[16:79];
FI;
ELSE (* Instruction is LGDT *)
  IF OperandSize = 16
  THEN
    GDTR(Limit) ← SRC[0:15];
    GDTR(Base) ← SRC[16:47] AND 00FFFFFFH;
  ELSE IF 32-bit Operand Size
  THEN
    GDTR(Limit) ← SRC[0:15];
    GDTR(Base) ← SRC[16:47];
  FI;
  ELSE IF 64-bit Operand Size (* In 64-Bit Mode *)
  THEN
    GDTR(Limit) ← SRC[0:15];
    GDTR(Base) ← SRC[16:79];
  FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#UD            If source operand is not a memory location.
               If the LOCK prefix is used.
#GP(0)         If the current privilege level is not 0.
               If a memory operand effective address is outside the CS, DS,
               ES, FS, or GS segment limit.
               If the DS, ES, FS, or GS register is used to access memory and it
               contains a NULL segment selector.
#SS(0)         If a memory operand effective address is outside the SS
               segment limit.
#PF(fault-code) If a page fault occurs.
```
Real-Address Mode Exceptions
#UD If source operand is not a memory location.
   If the LOCK prefix is used.
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual-8086 Mode Exceptions
#UD If source operand is not a memory location.
   If the LOCK prefix is used.
#GP(0) The LGDT and LIDT instructions are not recognized in virtual-8086 mode.
#GP If the current privilege level is not 0.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the current privilege level is not 0.
   If the memory address is in a non-canonical form.
#UD If source operand is not a memory location.
   If the LOCK prefix is used.
#PF(fault-code) If a page fault occurs.
LLDT—Load Local Descriptor Table Register

**Description**

Loads the source operand into the segment selector field of the local descriptor table register (LDTR). The source operand (a general-purpose register or a memory location) contains a segment selector that points to a local descriptor table (LDT). After the segment selector is loaded in the LDTR, the processor uses the segment selector to locate the segment descriptor for the LDT in the global descriptor table (GDT). It then loads the segment limit and base address for the LDT from the segment descriptor into the LDTR. The segment registers DS, ES, SS, FS, GS, and CS are not affected by this instruction, nor is the LDTR field in the task state segment (TSS) for the current task.

If bits 2-15 of the source operand are 0, LDTR is marked invalid and the LLDT instruction completes silently. However, all subsequent references to descriptors in the LDT (except by the LAR, VERR, VERW or LSL instructions) cause a general protection exception (#GP).

The operand-size attribute has no effect on this instruction.

The LLDT instruction is provided for use in operating-system software; it should not be used in application programs. This instruction can only be executed in protected mode or 64-bit mode.

In 64-bit mode, the operand size is fixed at 16 bits.

**Operation**

IF SRC(Offset) > descriptor table limit
    THEN #GP(segment selector); FI;

IF segment selector is valid
    Read segment descriptor;
    IF SegmentDescriptor(Type) ≠ LDT
        THEN #GP(segment selector); FI;
    IF segment descriptor is not present
        THEN #NP(segment selector); FI;
    LDTR(SegmentSelector) ← SRC;
    LDTR(SegmentDescriptor) ← GDTSegmentDescriptor;

**Opcode Instruction 64-Bit Mode**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /2</td>
<td>LLDT r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Load segment selector r/m16 into LDTR.</td>
</tr>
</tbody>
</table>
ELSE LDTR ← INVALID
Fl;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the current privilege level is not 0.
If a memory operand effective address is outside the CS, DS,
ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment
selector.
#GP(selector) If the selector operand does not point into the Global Descriptor
Table or if the entry in the GDT is not a Local Descriptor Table.
Segment selector is beyond GDT limit.
#SS(0) If a memory operand effective address is outside the SS
segment limit.
#NP(selector) If the LDT descriptor is not present.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD The LLDT instruction is not recognized in real-address mode.

Virtual-8086 Mode Exceptions
#UD The LLDT instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-
canonical form.
#GP(0) If the current privilege level is not 0.
If the memory address is in a non-canonical form.
#GP(selector) If the selector operand does not point into the Global Descriptor
Table or if the entry in the GDT is not a Local Descriptor Table.
Segment selector is beyond GDT limit.
#NP(selector) If the LDT descriptor is not present.
INSTRUCTION SET REFERENCE, A-M

#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.
**LMSW—Load Machine Status Word**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 /6</td>
<td>LMSW r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Loads r/m16 in machine status word of CR0.</td>
</tr>
</tbody>
</table>

**Description**

Loads the source operand into the machine status word, bits 0 through 15 of register CR0. The source operand can be a 16-bit general-purpose register or a memory location. Only the low-order 4 bits of the source operand (which contains the PE, MP, EM, and TS flags) are loaded into CR0. The PG, CD, NW, AM, WP, NE, and ET flags of CR0 are not affected. The operand-size attribute has no effect on this instruction.

If the PE flag of the source operand (bit 0) is set to 1, the instruction causes the processor to switch to protected mode. While in protected mode, the LMSW instruction cannot be used to clear the PE flag and force a switch back to real-address mode.

The LMSW instruction is provided for use in operating-system software; it should not be used in application programs. In protected or virtual-8086 mode, it can only be executed at CPL 0.

This instruction is provided for compatibility with the Intel 286 processor; programs and procedures intended to run on the Pentium 4, Intel Xeon, P6 family, Pentium, Intel486, and Intel386 processors should use the MOV (control registers) instruction to load the whole CR0 register. The MOV CR0 instruction can be used to set and clear the PE flag in CR0, allowing a procedure or program to switch between protected and real-address modes.

This instruction is a serializing instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode. Note that the operand size is fixed at 16 bits.

See “Changes to Instruction Behavior in VMX Non-Root Operation” in Chapter 22 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*, for more information about the behavior of this instruction in VMX non-root operation.

**Operation**

\[ CR0[0:3] \leftarrow SRC[0:3]; \]

**Flags Affected**

None.
INSTRUCTION SET REFERENCE, A-M

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the current privilege level is not 0.
If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.
LOCK—Assert LOCK# Signal Prefix

The LOCK prefix can be prepended only to the following instructions and only to those forms of the instructions where the destination operand is a memory operand: ADD, ADC, AND, BTC, BTR, BTS, CMPXCHG, CMPXCH8B, DEC, INC, NEG, NOT, OR, SBB, SUB, XOR, XADD, and XCHG. If the LOCK prefix is used with one of these instructions and the source operand is a memory operand, an undefined opcode exception (#UD) may be generated. An undefined opcode exception will also be generated if the LOCK prefix is used with any instruction not in the above list. The XCHG instruction always asserts the LOCK# signal regardless of the presence or absence of the LOCK prefix.

The LOCK prefix is typically used with the BTS instruction to perform a read-modify-write operation on a memory location in shared memory environment.

The integrity of the LOCK prefix is not affected by the alignment of the memory field. Memory locking is observed for arbitrarily misaligned fields.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

Beginning with the P6 family processors, when the LOCK prefix is prefixed to an instruction and the memory area being accessed is cached internally in the processor, the LOCK# signal is generally not asserted. Instead, only the processor’s cache is locked. Here, the processor’s cache coherency mechanism insures that the operation is carried out atomically with regards to memory. See “Effects of a Locked Operation on Internal Processor Caches” in Chapter 8 of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, the for more information on locking of caches.
INSTRUCTION SET REFERENCE, A-M

Operation
AssertLOCK#(DurationOfAccompanyingInstruction);

Flags Affected
None.

Protected Mode Exceptions
#UD If the LOCK prefix is used with an instruction not listed: ADD, ADC, AND, BTC, BTR, BTS, CMPXCHG, CMPXCH8B, DEC, INC, NEG, NOT, OR, SBB, SUB, XOR, XADD, XCHG.
Other exceptions can be generated by the instruction when the LOCK prefix is applied.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
LODS/LODSB/LODSW/LODSD/LODSQ—Load String

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>LODS m8</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load byte at address DS:(E)SI into AL. For 64-bit mode load byte at address (R)SI into AL.</td>
</tr>
<tr>
<td>AD</td>
<td>LODS m16</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load word at address DS:(E)SI into AX. For 64-bit mode load word at address (R)SI into AX.</td>
</tr>
<tr>
<td>AD</td>
<td>LODS m32</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load dword at address DS:(E)SI into EAX. For 64-bit mode load dword at address (R)SI into EAX.</td>
</tr>
<tr>
<td>REX.W + AD</td>
<td>LODS m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load qword at address (R)SI into RAX.</td>
</tr>
<tr>
<td>AC</td>
<td>LODSB</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load byte at address DS:(E)SI into AL. For 64-bit mode load byte at address (R)SI into AL.</td>
</tr>
<tr>
<td>AD</td>
<td>LODSW</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load word at address DS:(E)SI into AX. For 64-bit mode load word at address (R)SI into AX.</td>
</tr>
<tr>
<td>AD</td>
<td>LODSD</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load dword at address DS:(E)SI into EAX. For 64-bit mode load dword at address (R)SI into EAX.</td>
</tr>
<tr>
<td>REX.W + AD</td>
<td>LODSQ</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load qword at address (R)SI into RAX.</td>
</tr>
</tbody>
</table>

Description

Loads a byte, word, or doubleword from the source operand into the AL, AX, or EAX register, respectively. The source operand is a memory location, the address of which is read from the DS:EDI or the DS:SI registers (depending on the address-size attribute of the instruction, 32 or 16, respectively). The DS segment may be overridden with a segment override prefix.

At the assembly-code level, two forms of this instruction are allowed: the “explicit-operands” form and the “no-operands” form. The explicit-operands form (specified with the LODS mnemonic) allows the source operand to be specified explicitly. Here, the source operand should be a symbol that indicates the size and location of the source value. The destination operand is then automatically selected to match the size of the source operand (the AL register for byte operands, AX for word operands, and EAX for doubleword operands). This explicit-operands form is provided to allow documentation; however, note that the documentation provided by this form can be misleading. That is, the source operand symbol must specify the correct type (size) of the operand (byte, word, or doubleword), but it does not have to specify the
INSTRUCTION SET REFERENCE, A-M

correct location. The location is always specified by the DS:(E)SI registers, which must be loaded correctly before the load string instruction is executed.

The no-operands form provides “short forms” of the byte, word, and doubleword versions of the LODS instructions. Here also DS:(E)SI is assumed to be the source operand and the AL, AX, or EAX register is assumed to be the destination operand. The size of the source and destination operands is selected with the mnemonic: LODSB (byte loaded into register AL), LODSW (word loaded into AX), or LODSD (doubleword loaded into EAX).

After the byte, word, or doubleword is transferred from the memory location into the AL, AX, or EAX register, the (E)SI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the (E)SI register is incremented; if the DF flag is 1, the ESI register is decremented.) The (E)SI register is incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

In 64-bit mode, use of the REX.W prefix promotes operation to 64 bits. LODS/LODSQ load the quadword at address (R)SI into RAX. The (R)SI register is then incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register.

The LODS, LODSB, LODSW, and LODSD instructions can be preceded by the REP prefix for block loads of ECX bytes, words, or doublewords. More often, however, these instructions are used within a LOOP construct because further processing of the data moved into the register is usually necessary before the next transfer can be made. See “RDTSCP—Read Time-Stamp Counter and Processor ID” in Chapter 4, Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B, for a description of the REP prefix.

Operation

IF AL ← SRC; (* Byte load *)
   THEN AL ← SRC; (* Byte load *)
   IF DF = 0
      THEN (E)SI ← (E)SI + 1;
      ELSE (E)SI ← (E)SI – 1;
   FI;
ELSE IF AX ← SRC; (* Word load *)
   THEN IF DF = 0
      THEN (E)SI ← (E)SI + 2;
      ELSE (E)SI ← (E)SI – 2;
   IF;
   FI;
ELSE IF EAX ← SRC; (* Doubleword load *)
   THEN IF DF = 0
      THEN (E)SI ← (E)SI + 4;
      ELSE (E)SI ← (E)SI – 4;
ELSE IF RAX ← SRC; (* Quadword load *)
    THEN IF DF = 0
        THEN (R)SI ← (R)SI + 8;
        ELSE (R)SI ← (R)SI - 8;
    FI;
FI;
FI;
Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
LOOP/LOOPcc—Loop According to ECX Counter

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E2 cb</td>
<td>LOOP rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement count; jump short if count ≠ 0.</td>
</tr>
<tr>
<td>E1 cb</td>
<td>LOOPE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement count; jump short if count ≠ 0 and ZF = 1.</td>
</tr>
<tr>
<td>E0 cb</td>
<td>LOOPNE rel8</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement count; jump short if count ≠ 0 and ZF = 0.</td>
</tr>
</tbody>
</table>

**Description**

Performs a loop operation using the RCX, ECX or CX register as a counter (depending on whether address size is 64 bits, 32 bits, or 16 bits). Note that the LOOP instruction ignores REX.W; but 64-bit address size can be over-ridden using a 67H prefix.

Each time the LOOP instruction is executed, the count register is decremented, then checked for 0. If the count is 0, the loop is terminated and program execution continues with the instruction following the LOOP instruction. If the count is not zero, a near jump is performed to the destination (target) operand, which is presumably the instruction at the beginning of the loop.

The target instruction is specified with a relative offset (a signed offset relative to the current value of the instruction pointer in the IP/EIP/RIP register). This offset is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed, 8-bit immediate value, which is added to the instruction pointer. Offsets of –128 to +127 are allowed with this instruction.

Some forms of the loop instruction (LOOPcc) also accept the ZF flag as a condition for terminating the loop before the count reaches zero. With these forms of the instruction, a condition code (cc) is associated with each instruction to indicate the condition being tested for. Here, the LOOPcc instruction itself does not affect the state of the ZF flag; the ZF flag is changed by other instructions in the loop.

**Operation**

\[
\text{IF } \text{AddressSize} = 32 \\
\quad \text{THEN} \text{ Count is ECX; } \\
\text{ELSE IF } \text{AddressSize} = 64 \\
\quad \text{Count is RCX; } \\
\text{ELSE Count is CX; } \\
\text{FI; } \\
\text{Count } \leftarrow \text{ Count } - \text{ 1; } \\
\text{IF Instruction is not LOOP} \\
\quad \text{THEN } \\
\]

LOOP/LOOPcc—Loop According to ECX Counter
IF (Instruction ← LOOPE) or (Instruction ← LOOPZ)
THEN IF (ZF = 1) and (Count ≠ 0)
    THEN BranchCond ← 1;
    ELSE BranchCond ← 0;
    Fl;
ELSE (Instruction = LOOPNE) or (Instruction = LOOPNZ)
    IF (ZF = 0) and (Count ≠ 0)
        THEN BranchCond ← 1;
        ELSE BranchCond ← 0;
        Fl;
    ELSE (* Instruction = LOOP *)
        IF (Count ≠ 0)
            THEN BranchCond ← 1;
            ELSE BranchCond ← 0;
            Fl;
    Fl;
IF BranchCond = 1
THEN
    IF OperandSize = 32
        THEN EIP ← EIP + SignExtend(DEST);
        ELSE IF OperandSize = 64
            THEN RIP ← RIP + SignExtend(DEST);
                Fl;
            ELSE IF OperandSize = 16
                THEN EIP ← EIP AND 0000FFFFH;
                Fl;
            ELSE IF OperandSize = (32 or 64)
                THEN IF (R/E)IP < CS.Base or (R/E)IP > CS.Limit
                    #GP; Fl;
                Fl;
            ELSE
                Terminate loop and continue program execution at (R/E)IP;
            Fl;
    ELSE
        Flags Affected
        None.
Protected Mode Exceptions

#GP(0) If the offset being jumped to is beyond the limits of the CS segment.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If the offset being jumped to is beyond the limits of the CS segment or is outside of the effective address space from 0 to FFFFH. This condition can occur if a 32-bit address size override prefix is used.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0) If the offset being jumped to is in a non-canonical form.

#UD If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, A-M

LSL—Load Segment Limit

Description
Loads the unscrambled segment limit from the segment descriptor specified with the second operand (source operand) into the first operand (destination operand) and sets the ZF flag in the EFLAGS register. The source operand (which can be a register or a memory location) contains the segment selector for the segment descriptor being accessed. The destination operand is a general-purpose register.

The processor performs access checks as part of the loading process. Once loaded in the destination register, software can compare the segment limit with the offset of a pointer.

The segment limit is a 20-bit value contained in bytes 0 and 1 and in the first 4 bits of byte 6 of the segment descriptor. If the descriptor has a byte granular segment limit (the granularity flag is set to 0), the destination operand is loaded with a byte granular value (byte limit). If the descriptor has a page granular segment limit (the granularity flag is set to 1), the LSL instruction will translate the page granular limit (page limit) into a byte limit before loading it into the destination operand. The translation is performed by shifting the 20-bit “raw” limit left 12 bits and filling the low-order 12 bits with 1s.

When the operand size is 32 bits, the 32-bit byte limit is stored in the destination operand. When the operand size is 16 bits, a valid 32-bit limit is computed; however, the upper 16 bits are truncated and only the low-order 16 bits are loaded into the destination operand.

This instruction performs the following checks before it loads the segment limit into the destination register:

• Checks that the segment selector is not NULL.
• Checks that the segment selector points to a descriptor that is within the limits of the GDT or LDT being accessed.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 03 /r</td>
<td>LSL r16, r16/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Load: r16 ← segment limit, selector r16/m16.</td>
</tr>
<tr>
<td>0F 03 /r</td>
<td>LSL r32, r32/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Load: r32 ← segment limit, selector r32/m16.</td>
</tr>
<tr>
<td>REX.W + 0F 03 /r</td>
<td>LSL r64, r32/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Load: r64 ← segment limit, selector r32/m16.</td>
</tr>
</tbody>
</table>

NOTES:
* For all loads (regardless of destination sizing), only bits 16-0 are used. Other bits are ignored.
Checks that the descriptor type is valid for this instruction. All code and data segment descriptors are valid for (can be accessed with) the LSL instruction. The valid special segment and gate descriptor types are given in the following table.

If the segment is not a conforming code segment, the instruction checks that the specified segment descriptor is visible at the CPL (that is, if the CPL and the RPL of the segment selector are less than or equal to the DPL of the segment selector).

If the segment descriptor cannot be accessed or is an invalid type for the instruction, the ZF flag is cleared and no value is loaded in the destination operand.

### Table 3-68. Segment and Gate Descriptor Types

<table>
<thead>
<tr>
<th>Type</th>
<th>Protected Mode</th>
<th>IA-32e Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Name</td>
<td>Valid</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>Available 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>LDT</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>Busy 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>16-bit call gate</td>
<td>No</td>
</tr>
<tr>
<td>5</td>
<td>16-bit/32-bit task gate</td>
<td>No</td>
</tr>
<tr>
<td>6</td>
<td>16-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>7</td>
<td>16-bit trap gate</td>
<td>No</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>9</td>
<td>Available 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>A</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>B</td>
<td>Busy 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>C</td>
<td>32-bit call gate</td>
<td>No</td>
</tr>
<tr>
<td>D</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>E</td>
<td>32-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>F</td>
<td>32-bit trap gate</td>
<td>No</td>
</tr>
</tbody>
</table>

### Operation

```plaintext
IF SRC(Offset) > descriptor table limit
    THEN ZF ← 0; Fl;
```

LSL—Load Segment Limit
Read segment descriptor;

IF SegmentDescriptor(Type) \neq\ conforming code segment
and (CPL > DPL) OR (RPL > DPL)
or Segment type is not valid for instruction
THEN
    ZF \leftarrow 0;
ELSE
    temp \leftarrow \text{SegmentLimit}([SRC]);
    \text{IF} (G \leftarrow 1)
        \text{THEN} temp \leftarrow \text{ShiftLeft}(12, \text{temp}) \text{ OR } 00000FFFH;
    \text{ELSE IF} \text{OperandSize} = 32
        \text{THEN} DEST \leftarrow \text{temp; FI;}
    \text{ELSE IF} \text{OperandSize} = 64 (* REX.W used *)
        \text{THEN} DEST (* Zero-extended *) \leftarrow \text{temp; FI;}
    \text{ELSE (* OperandSize = 16 *)}
        DEST \leftarrow \text{temp AND FFFFH;}
    \text{FI;}
\text{FI;}

\textbf{Flags Affected}

The ZF flag is set to 1 if the segment limit is loaded successfully; otherwise, it is set to 0.

\textbf{Protected Mode Exceptions}

\#GP(0) \quad \text{If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.}

\text{IF the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.}

\#SS(0) \quad \text{If a memory operand effective address is outside the SS segment limit.}

\#PF(fault-code) \quad \text{If a page fault occurs.}

\#AC(0) \quad \text{If alignment checking is enabled and the memory operand effective address is unaligned while the current privilege level is 3.}

\#UD \quad \text{If the LOCK prefix is used.}

\textbf{Real-Address Mode Exceptions}

\#UD \quad \text{The LAR instruction cannot be executed in real-address mode.}

\textbf{Virtual-8086 Mode Exceptions}

\#UD \quad \text{The LAR instruction cannot be executed in virtual-8086 mode.}
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If the memory operand effective address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory operand effective address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and the memory operand effective address is unaligned while the current privilege level is 3.
#UD If the LOCK prefix is used.
**LTR—Load Task Register**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /3</td>
<td>LTR r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Load r/m16 into task register.</td>
</tr>
</tbody>
</table>

**Description**

Loads the source operand into the segment selector field of the task register. The source operand (a general-purpose register or a memory location) contains a segment selector that points to a task state segment (TSS). After the segment selector is loaded in the task register, the processor uses the segment selector to locate the segment descriptor for the TSS in the global descriptor table (GDT). It then loads the segment limit and base address for the TSS from the segment descriptor into the task register. The task pointed to by the task register is marked busy, but a switch to the task does not occur.

The LTR instruction is provided for use in operating-system software; it should not be used in application programs. It can only be executed in protected mode when the CPL is 0. It is commonly used in initialization code to establish the first task to be executed.

The operand-size attribute has no effect on this instruction.

In 64-bit mode, the operand size is still fixed at 16 bits. The instruction references a 16-byte descriptor to load the 64-bit base.

**Operation**

IF SRC is a NULL selector
    THEN #GP(0);

IF SRC(Offset) > descriptor table limit OR IF SRC(type) ≠ global
    THEN #GP(segment selector); Fl;

Read segment descriptor;

IF segment descriptor is not for an available TSS
    THEN #GP(segment selector); Fl;
IF segment descriptor is not present
    THEN #NP(segment selector); Fl;

TSSSegmentDescriptor(busy) ← 1;
(* Locked read-modify-write operation on the entire descriptor when setting busy flag *)

TaskRegister(SegmentSelector) ← SRC;
TaskRegister(SegmentDescriptor) ← TSSSegmentDescriptor;
Flags Affected
None.

Protected Mode Exceptions

#GP(0)  If the current privilege level is not 0.
        If a memory operand effective address is outside the CS, DS,
        ES, FS, or GS segment limit.
        If the source operand contains a NULL segment selector.
        If the DS, ES, FS, or GS register is used to access memory and it
        contains a NULL segment selector.

#GP(selector)  If the source selector points to a segment that is not a TSS or to
        one for a task that is already busy.
        If the selector points to LDT or is beyond the GDT limit.

#NP(selector)  If the TSS is marked not present.

#SS(0)  If a memory operand effective address is outside the SS
        segment limit.

#PF(fault-code)  If a page fault occurs.

#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions

#UD  The LTR instruction is not recognized in real-address mode.

Virtual-8086 Mode Exceptions

#UD  The LTR instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-
        canonical form.

#GP(0)  If the current privilege level is not 0.
        If the memory address is in a non-canonical form.
        If the source operand contains a NULL segment selector.

#GP(selector)  If the source selector points to a segment that is not a TSS or to
        one for a task that is already busy.
        If the selector points to LDT or is beyond the GDT limit.
        If the descriptor type of the upper 8-byte of the 16-byte
descriptor is non-zero.
#NP(selector)  If the TSS is marked not present.
#PF(fault-code)  If a page fault occurs.
#UD  If the LOCK prefix is used.
MASKMOVDQU—Store Selected Bytes of Double Quadword

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F F7</td>
<td>MASKMOVDQU xmm1, xmm2</td>
<td>Valid</td>
<td>Valid</td>
<td>Selectively write bytes from xmm1 to memory location using the byte mask in xmm2. The default memory location is specified by DS:EDI.</td>
</tr>
</tbody>
</table>

**Description**

Stores selected bytes from the source operand (first operand) into an 128-bit memory location. The mask operand (second operand) selects which bytes from the source operand are written to memory. The source and mask operands are XMM registers. The location of the first byte of the memory location is specified by DI/EDI and DS registers. The memory location does not need to be aligned on a natural boundary. (The size of the store address depends on the address-size attribute.)

The most significant bit in each byte of the mask operand determines whether the corresponding byte in the source operand is written to the corresponding byte location in memory: 0 indicates no write and 1 indicates write.

The MASKMOVDQU instruction generates a non-temporal hint to the processor to minimize cache pollution. The non-temporal hint is implemented by using a write combining (WC) memory type protocol (see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10, of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MASKMOVDQU instructions if multiple processors might use different memory types to read/write the destination memory locations.

Behavior with a mask of all 0s is as follows:

- No data will be written to memory.
- Signaling of breakpoints (code or data) is not guaranteed; different processor implementations may signal or not signal these breakpoints.
- Exceptions associated with addressing memory and page faults may still be signaled (implementation dependent).
- If the destination memory region is mapped as UC or WP, enforcement of associated semantics for these memory types is not guaranteed (that is, is reserved) and is implementation-specific.

The MASKMOVDQU instruction can be used to improve performance of algorithms that need to merge data on a byte-by-byte basis. MASKMOVDQU should not cause a read for ownership; doing so generates unnecessary bandwidth since data is to be written directly using the byte-mask without allocating old data prior to the store.
INSTRUCTION SET REFERENCE, A-M

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

IF (MASK[7] = 1)
THEN DEST[DI/EDI] ← SRC[7:0] ELSE (* Memory location unchanged *); Fl;
IF (MASK[15] = 1)
THEN DEST[DI/EDI +1] ← SRC[15:8] ELSE (* Memory location unchanged *); Fl;
(* Repeat operation for 3rd through 14th bytes in source operand *)
IF (MASK[127] = 1)
THEN DEST[DI/EDI +15] ← SRC[127:120] ELSE (* Memory location unchanged *); Fl;

Intel C/C++ Compiler Intrinsic Equivalent

void _mm_maskmoveu_si128(__m128i d, __m128i n, char * p)

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments. (even if mask is all 0s).
If the destination operand is in a nonwritable segment.
If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) For an illegal address in the SS segment (even if mask is all 0s).

#PF(fault-code) For a page fault (implementation specific).

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH. (even if mask is all 0s).

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
**Virtual-8086 Mode Exceptions**
Same exceptions as in real address mode.

- **#PF(fault-code)** For a page fault (implementation specific).
- **#UD** If the LOCK prefix is used.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
- **#GP(0)** If the memory address is in a non-canonical form.
- **#SS(0)** If a memory address referencing the SS segment is in a non-canonical form.
- **#PF(fault-code)** For a page fault (implementation specific).
- **#NM** If CR0.TS[bit 3] ≠ 1.
- **#UD** If CR0.E[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
  - If the LOCK prefix is used.
MASKMOVQ—Store Selected Bytes of Quadword

**Description**

Stores selected bytes from the source operand (first operand) into a 64-bit memory location. The mask operand (second operand) selects which bytes from the source operand are written to memory. The source and mask operands are MMX technology registers. The location of the first byte of the memory location is specified by DI/EDI and DS registers. (The size of the store address depends on the address-size attribute.)

The most significant bit in each byte of the mask operand determines whether the corresponding byte in the source operand is written to the corresponding byte location in memory: 0 indicates no write and 1 indicates write.

The MASKMOVQ instruction generates a non-temporal hint to the processor to minimize cache pollution. The non-temporal hint is implemented by using a write combining (WC) memory type protocol (see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10, of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MASKMOVQ instructions if multiple processors might use different memory types to read/write the destination memory locations.

This instruction causes a transition from x87 FPU to MMX technology state (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]).

The behavior of the MASKMOVQ instruction with a mask of all 0s is as follows:

- No data will be written to memory.
- Transition from x87 FPU to MMX technology state will occur.
- Exceptions associated with addressing memory and page faults may still be signaled (implementation dependent).
- Signaling of breakpoints (code or data) is not guaranteed (implementation dependent).
- If the destination memory region is mapped as UC or WP, enforcement of associated semantics for these memory types is not guaranteed (that is, is reserved) and is implementation-specific.
The MASKMOVQ instruction can be used to improve performance for algorithms that need to merge data on a byte-by-byte basis. It should not cause a read for ownership; doing so generates unnecessary bandwidth since data is to be written directly using the byte-mask without allocating old data prior to the store.

In 64-bit mode, the memory address is specified by DS:RDI.

**Operation**

\[
\begin{align*}
\text{IF} & \ (\text{MASK}[7] = 1) \\
& \quad \text{THEN} \ \text{DEST}[\text{DI/EDI}] \leftarrow \text{SRC}[7:0] \ \text{ELSE} \ (* \ \text{Memory location unchanged} *) ; \ F1; \\
\text{IF} & \ (\text{MASK}[15] = 1) \\
& \quad \text{THEN} \ \text{DEST}[\text{DI/EDI} + 1] \leftarrow \text{SRC}[15:8] \ \text{ELSE} \ (* \ \text{Memory location unchanged} *) ; \ F1; \\
& \quad (* \ \text{Repeat operation for 3rd through 6th bytes in source operand} *) \\
\text{IF} & \ (\text{MASK}[63] = 1) \\
& \quad \text{THEN} \ \text{DEST}[\text{DI/EDI} + 15] \leftarrow \text{SRC}[63:56] \ \text{ELSE} \ (* \ \text{Memory location unchanged} *) ; \ F1;
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

```c
void _mm_maskmove_si64(__m64d, __m64n, char * p)
```

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments (even if mask is all 0s).
  - If the destination operand is in a nonwritable segment.
  - If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)** For an illegal address in the SS segment (even if mask is all 0s).
- **#PF(fault-code)** For a page fault (implementation specific).
- **#NM** If CR0.TS[bit 3] = 1.
- **#MF** If there is a pending FPU exception.
- **#UD** If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01:H:EDX.SSE[bit 25] = 0.
  - If Mod field of the ModR/M byte not 11B.
  - If the LOCK prefix is used.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- **GP** If any part of the operand lies outside the effective address space from 0 to FFFFH. (even if mask is all 0s).
- **#NM** If CR0.TS[bit 3] = 1.
INSTRUCTION SET REFERENCE, A-M

#MF If there is a pending FPU exception.
#UD If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault (implementation specific).
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#PF(fault-code) For a page fault (implementation specific).
#NM If CR0.TS[bit 3] = 1.
#MF If there is a pending FPU exception.
#UD If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If Mod field of the ModR/M byte not 11B.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MAXPD—Return Maximum Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
</table>
| 66 0F 5F /r | MAXPD xmm1, xmm2/m128 | Valid       | Valid           | Return the maximum double-precision floating-point values between xmm2/m128 and xmm1.

Description

Performs a SIMD compare of the packed double-precision floating-point values in the destination operand (first operand) and the source operand (second operand), and returns the maximum value for each pair of values to the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is forwarded unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MAXPD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

\[
\text{DEST}[63:0] \leftarrow \begin{cases} 
\text{IF} & \left( (\text{DEST}[63:0] = 0.0) \text{ and } (\text{SRC}[63:0] = 0.0) \right) \\
\text{THEN} & \text{SRC}[63:0]; \\
\text{ELSE IF} & (\text{DEST}[63:0] = \text{SNaN}) \text{ THEN } \text{SRC}[63:0]; \text{ Fl; } \\
\text{ELSE IF} & (\text{SRC}[63:0] = \text{SNaN}) \text{ THEN } \text{SRC}[63:0]; \text{ Fl; } \\
\text{ELSE IF} & (\text{DEST}[63:0] > \text{SRC}[63:0]) \\
\text{THEN} & \text{DEST}[63:0]; \\
\text{ELSE} & \text{SRC}[63:0]; \text{ Fl; Fl;} 
\end{cases}
\]

\[
\text{DEST}[127:64] \leftarrow \begin{cases} 
\text{IF} & \left( (\text{DEST}[127:64] = 0.0) \text{ and } (\text{SRC}[127:64] = 0.0) \right) \\
\text{THEN} & \text{SRC}[127:64]; \\
\text{ELSE IF} & (\text{DEST}[127:64] = \text{SNaN}) \text{ THEN } \text{SRC}[127:64]; \text{ Fl; } \\
\text{ELSE IF} & (\text{SRC}[127:64] = \text{SNaN}) \text{ THEN } \text{SRC}[127:64]; \text{ Fl; } \\
\text{ELSE IF} & (\text{DEST}[127:64] > \text{SRC}[63:0]) \\
\text{THEN} & \text{DEST}[127:64]; \\
\end{cases}
\]
MAXPD—Return Maximum Packed Double-Precision Floating-Point Values

Intel C/C++ Compiler Intrinsic Equivalent
MAXPD __m128d_mm_max_pd(__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
MAXPS—Return Maximum Packed Single-Precision Floating-Point Values

Description

Performs a SIMD compare of the packed single-precision floating-point values in the destination operand (first operand) and the source operand (second operand), and returns the maximum value for each pair of values to the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MAXPS can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

\[
\text{DEST}[31:0] \leftarrow \begin{cases} 
\text{IF (\text{DEST}[31:0] = 0.0) and (\text{SRC}[31:0] = 0.0)} & \text{THEN SR}[31:0]; \\
\text{ELSE IF (\text{DEST}[31:0] = SNaN) THEN SR}[31:0]; F; \\
\text{ELSE IF (\text{SRC}[31:0] = SNaN) THEN SR}[31:0]; F; \\
\text{ELSE IF (\text{DEST}[31:0] > SRC}[31:0]); F; \\
\text{THEN DEST}[31:0]; \\
\text{ELSE SRC}[31:0]; F; F; \\
\end{cases} \\
\text{(* Repeat operation for 2nd and 3rd doublewords *)};
\]

\[
\text{DEST}[127:64] \leftarrow \begin{cases} 
\text{IF (\text{DEST}[127:96] = 0.0) and (\text{SRC}[127:96] = 0.0)} & \text{THEN SR}[127:96]; \\
\text{ELSE IF (\text{DEST}[127:96] = SNaN) THEN SR}[127:96]; \\
\text{ELSE IF (\text{SRC}[127:96] = SNaN) THEN SR}[127:96]; \\
\text{ELSE IF (\text{DEST}[127:96] > SRC}[127:96]); \\
\end{cases} \\
\]

 Opcode Instruction 64-Bit Mode Compat/ Leg Mode Description

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 5F</td>
<td>MAXPS xmm1,</td>
<td>Valid</td>
<td>Valid</td>
<td>Return the maximum single-precision floating-point values between xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>/r</td>
<td>xmm2/m128</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

INSTRUCTION SET REFERENCE, A-M
THEN DEST[127:96];
ELSE SRC[127:96]; Fl; Fl;

**Intel C/C++ Compiler Intrinsic Equivalent**

MAXPS __m128d _mm_max_ps(__m128d a, __m128d b)

**SIMD Floating-Point Exceptions**

Invalid (including QNaN source operand), Denormal.

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
  - If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP** If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
  - If any part of the operand lies outside the effective address space from 0 to FFFFH.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
   If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.
MAXSD—Return Maximum Scalar Double-Precision Floating-Point Value

**Description**

Compares the low double-precision floating-point values in the destination operand (first operand) and the source operand (second operand), and returns the maximum value to the low quadword of the destination operand. The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. When the source operand is a memory operand, only 64 bits are accessed. The high quadword of the destination operand remains unchanged.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MAXSD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\text{DEST}[63:0] \leftarrow \begin{cases} 
\text{IF (DEST}[63:0] = 0.0) \text{ and (SRC}[63:0] = 0.0) \\
\text{THEN SRC}[63:0]; \text{FI;}
\text{IF (DEST}[63:0] = \text{SNaN})
\text{THEN SRC}[63:0];
\text{ELSE IF (SRC}[63:0] = \text{SNaN})
\text{THEN SRC}[63:0]; \text{FI;}
\text{ELSE IF (DEST}[63:0] > \text{SRC}[63:0])
\text{THEN DEST}[63:0];
\text{ELSE SRC}[63:0]; \text{FI; FI;}
\end{cases}
\]

(* DEST[127:64] is unchanged *):
INSTRUCTION SET REFERENCE, A-M

Intel C/C++ Compiler Intrinsic Equivalent
MAXSD __m128d_mm_max_sd(__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
MAXSD—Return Maximum Scalar Double-Precision Floating-Point Value

#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MAXSS—Return Maximum Scalar Single-Precision Floating-Point Value

Description

Compares the low single-precision floating-point values in the destination operand (first operand) and the source operand (second operand), and returns the maximum value to the low doubleword of the destination operand. The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. When the source operand is a memory operand, only 32 bits are accessed. The three high-order doublewords of the destination operand remain unchanged.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MAXSS can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

\[
\text{DEST}[63:0] \leftarrow \begin{cases} 
\text{SRC}[31:0] & \text{if } \left(\text{DEST}[31:0] = 0.0 \text{ and } \text{SRC}[31:0] = 0.0\right) \\
\text{DEST}[31:0] > \text{SRC}[31:0] & \text{then } \text{DEST}[31:0]; \\
\text{SRC}[31:0] & \text{else if } \left(\text{DEST}[31:0] = \text{SNaN}\right) \text{ then } \text{SRC}[31:0]; \\
\text{SRC}[31:0] & \text{else if } \left(\text{SRC}[31:0] = \text{SNaN}\right) \text{ then } \text{SRC}[31:0]; \\
\text{DEST}[31:0] > \text{SRC}[31:0] & \text{then } \text{DEST}[31:0]; \\
\text{SRC}[31:0] & \text{else}; \\
\end{cases}
\]

(* DEST[127:32] is unchanged *)

Intel C/C++ Compiler Intrinsic Equivalent

__m128d _mm_max_ss(__m128d a, __m128d b)
**SIMD Floating-Point Exceptions**

Invalid (including QNaN source operand), Denormal.

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- **GP** If any part of the operand lies outside the effective address space from 0 to FFFFH.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  - If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

Same exceptions as in real address mode.

- **#PF(fault-code)** For a page fault.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  For a page fault.
#NM  If CR0.TS[bit 3] = 1.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MFENCE—Memory Fence

<table>
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<tr>
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<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AE /6</td>
<td>MFENCE</td>
<td>Valid</td>
<td>Valid</td>
<td>Serializes load and store operations.</td>
</tr>
</tbody>
</table>

**Description**

Performs a serializing operation on all load-from-memory and store-to-memory instructions that were issued prior the MFENCE instruction. This serializing operation guarantees that every load and store instruction that precedes in program order the MFENCE instruction is globally visible before any load or store instruction that follows the MFENCE instruction is globally visible. The MFENCE instruction is ordered with respect to all load and store instructions, other MFENCE instructions, any SFENCE and LFENCE instructions, and any serializing instructions (such as the CPUID instruction).

Weakly ordered memory types can be used to achieve higher processor performance through such techniques as out-of-order issue, speculative reads, write-combining, and write-collapsing. The degree to which a consumer of data recognizes or knows that the data is weakly ordered varies among applications and may be unknown to the producer of this data. The MFENCE instruction provides a performance-efficient way of ensuring load and store ordering between routines that produce weakly-ordered results and routines that consume that data.

It should be noted that processors are free to speculatively fetch and cache data from system memory regions that are assigned a memory-type that permits speculative reads (that is, the WB, WC, and WT memory types). The PREFETCHh instruction is considered a hint to this speculative behavior. Because this speculative fetching can occur at any time and is not tied to instruction execution, the MFENCE instruction is not ordered with respect to PREFETCHh instructions or any other speculative fetching mechanism (that is, data could be speculatively loaded into the cache just before, during, or after the execution of an MFENCE instruction).

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

Wait_On_Following_Loads_And_Stores_Until(preceding_loads_and_stores_globally_visible);

**Intel C/C++ Compiler Intrinsic Equivalent**

void _mm_mfence(void)

**Exceptions (All Modes of Operation)**

#UD If CPUID.01H:EDX.SSE2[bit 26] = 0. If the LOCK prefix is used.
MINPD—Return Minimum Packed Double-Precision Floating-Point Values

**Description**

Performs a SIMD compare of the packed double-precision floating-point values in the destination operand (first operand) and the source operand (second operand), and returns the minimum value for each pair of values to the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MINPD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\begin{align*}
\text{DEST}[63:0] \leftarrow & \quad \text{IF } ((\text{DEST}[63:0] = 0.0) \text{ and } (\text{SRC}[63:0] = 0.0)) \\
& \quad \text{THEN SRC}[63:0]; \text{Fl;} \\
& \quad \text{ELSE IF } (\text{DEST}[63:0] = \text{SNaN}) \text{ THEN SRC}[63:0]; \text{Fl;} \\
& \quad \text{ELSE IF } (\text{SRC}[63:0] = \text{SNaN}) \text{ THEN SRC}[63:0]; \text{Fl;} \\
& \quad \text{ELSE IF } (\text{DEST}[63:0] < \text{SRC}[63:0]) \\
& \quad \quad \text{THEN DEST}[63:0] \\
& \quad \quad \text{ELSE SRC}[63:0]; \text{Fl;} \text{ Fl;} \\
\text{DEST}[127:64] \leftarrow & \quad \text{IF } ((\text{DEST}[127:64] = 0.0) \text{ and } (\text{SRC}[127:64] = 0.0)) \\
& \quad \text{THEN SRC}[127:64]; \text{Fl;} \\
& \quad \text{ELSE IF } (\text{DEST}[127:64] = \text{SNaN}) \text{ THEN SRC}[127:64]; \text{Fl;} \\
& \quad \text{ELSE IF } (\text{SRC}[127:64] = \text{SNaN}) \text{ THEN SRC}[127:64]; \text{Fl;} \\
& \quad \text{ELSE IF } (\text{DEST}[127:64] < \text{SRC}[63:0])
\end{align*}
\]

**Opcode Instruction 64-Bit Mode**

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<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
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</thead>
<tbody>
<tr>
<td>66 0F 5D /r</td>
<td>MINPD xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Return the minimum double-precision floating-point values between xmm2/m128 and xmm1.</td>
</tr>
</tbody>
</table>
THEN DEST[127:64] ELSE SRC[127:64]; FI; FI;

Intel C/C++ Compiler Intrinsic Equivalent
MINPD __m128d_mm_min_pd(__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
    If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE2[bit 26] = 0.
    If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
    If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, A-M

MINPS—Return Minimum Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 5D/1r</td>
<td>MINPS xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Return the minimum single-precision floating-point values between xmm2/m128 and xmm1.</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD compare of the packed single-precision floating-point values in the destination operand (first operand) and the source operand (second operand), and returns the minimum value for each pair of values to the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MINPS can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

\[
\text{DEST}[63:0] \leftarrow \begin{cases} 
\text{IF } ((\text{DEST}[31:0] = 0.0) \text{ and } (\text{SRC}[31:0] = 0.0)) \\
\text{THEN SRC}[31:0]; \text{ ELSE IF } (\text{DEST}[31:0] = \text{SNaN}) \text{ THEN SRC}[31:0]; \text{ ELSE IF } (\text{SRC}[31:0] = \text{SNaN}) \text{ THEN SRC}[31:0]; \text{ ELSE IF } \neg(\text{DEST}[31:0] > \text{SRC}[31:0]) \\
\text{THEN DEST}[31:0]; \text{ ELSE SRC}[31:0]; \text{ FI; FI; FI;) 
\end{cases}
\]

(* Repeat operation for 2nd and 3rd doublewords *);

\[
\text{DEST}[127:64] \leftarrow \begin{cases} 
\text{IF } ((\text{DEST}[127:96] = 0.0) \text{ and } (\text{SRC}[127:96] = 0.0)) \\
\text{THEN SRC}[127:96]; \text{ ELSE IF } (\text{DEST}[127:96] = \text{SNaN}) \text{ THEN SRC}[127:96]; \text{ ELSE IF } (\text{SRC}[127:96] = \text{SNaN}) \text{ THEN SRC}[127:96]; \text{ ELSE IF } \neg(\text{DEST}[127:96] > \text{SRC}[127:96]) \\
\text{THEN DEST}[127:96]; \text{ ELSE SRC}[127:96]; \text{ FI; FI; FI;) 
\end{cases}
\]
THEN DEST[127:96]
ELSE SRC[127:96]; Fi; Fi;

**Intel C/C++ Compiler Intrinsic Equivalent**

MINPS __m128d_mm_min_ps(__m128d a, __m128d b)

**SIMD Floating-Point Exceptions**

Invalid (including QNaN source operand), Denormal.

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
  
  If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

- **#SS(0)** If a memory operand effective address is outside the SS segment limit.

- **#PF(fault-code)** For a page fault.

- **#NM** If CR0.TS[bit 3] = 1.


- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXMMXCEPT[bit 10] = 0.

  - If CR0.EM[bit 2] = 1.
  
  - If CR4.OSFXSR[bit 9] = 0.

  - If CPUID.01H:EDX.SSE[bit 25] = 0.

  - If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP** If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

  - If any part of the operand lies outside the effective address space from 0 to FFFFH.

- **#NM** If CR0.TS[bit 3] = 1.


- **#UD** If an unmasked SIMD floating-point exception and CR4.OSXMMXCEPT[bit 10] = 0.

  - If CR0.EM[bit 2] = 1.

  - If CR4.OSFXSR[bit 9] = 0.
MINPS—Return Minimum Packed Single-Precision Floating-Point Values

If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**
Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, A-M

MINSD—Return Minimum Scalar Double-Precision Floating-Point Value

Description

Compares the low double-precision floating-point values in the destination operand (first operand) and the source operand (second operand), and returns the minimum value to the low quadword of the destination operand. The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. When the source operand is a memory operand, only the 64 bits are accessed. The high quadword of the destination operand remains unchanged.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MINSD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

\[
\text{DEST}[63:0] \leftarrow \begin{cases} 
\text{IF } ((\text{DEST}[63:0] = 0.0) \text{ and } (\text{SRC}[63:0] = 0.0)) \text{ THEN SRC}[63:0]; \\
\text{ELSE IF } (\text{DEST}[63:0] = \text{SNaN}) \text{ THEN SRC}[63:0]; \text{ Fl}; \\
\text{ELSE IF } (\text{SRC}[63:0] = \text{SNaN}) \text{ THEN SRC}[63:0]; \text{ Fl}; \\
\text{ELSE IF } (\text{DEST}[63:0] < \text{SRC}[63:0]) \text{ THEN DEST}[63:0]; \\
\text{ELSE SRC}[63:0]; \text{ Fl}; \text{ Fl}; 
\end{cases}
\]

(* DEST[127:64] is unchanged *):

Intel C/C++ Compiler Intrinsic Equivalent

\[
\text{MINSD } \_m128d\_mm\_min\_sd(\_m128d\ a, \_m128d\ b)
\]
SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
INSTRUCTION SET REFERENCE, A-M

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MINSS—Return Minimum Scalar Single-Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 5D /r</td>
<td>MINSS xmm1, xmm2/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Return the minimum scalar single-precision floating-point value between xmm2/mem32 and xmm1.</td>
</tr>
</tbody>
</table>

Description

Compares the low single-precision floating-point values in the destination operand (first operand) and the source operand (second operand), and returns the minimum value to the low doubleword of the destination operand. The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. When the source operand is a memory operand, only 32 bits are accessed. The three high-order doublewords of the destination operand remain unchanged.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MINSD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

\[
\text{DEST}[63:0] \leftarrow \begin{cases} 
\text{IF ((DEST}[31:0] = 0.0) AND (SRC}[31:0] = 0.0)) \\
\text{THEN SRC}[31:0]; \\
\text{ELSE IF (DEST}[31:0] = \text{SNaN}) \text{THEN SRC}[31:0]; F; \\
\text{ELSE IF (SRC}[31:0] = \text{SNaN}) \text{THEN SRC}[31:0]; F; \\
\text{ELSE IF (DEST}[31:0] < SRC}[31:0]) \\
\text{THEN DEST}[31:0] \\
\text{ELSE SRC}[31:0]; F; F; \\
\end{cases}
\]

(* DEST[127:32] is unchanged *):

Intel C/C++ Compiler Intrinsic Equivalent

MINSS _m128d _mm_min_ss(_m128d a, _m128d b)
SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE[bit 25] = 0.
  If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MONITOR—Set Up Monitor Address

Description

The MONITOR instruction arms address monitoring hardware using an address specified in EAX (the address range that the monitoring hardware checks for store operations can be determined by using CPUID). A store to an address within the specified address range triggers the monitoring hardware. The state of monitor hardware is used by MWAIT.

The content of EAX is an effective address (in 64-bit mode, RAX is used). By default, the DS segment is used to create a linear address that is monitored. Segment overrides can be used.

ECX and EDX are also used. They communicate other information to MONITOR. ECX specifies optional extensions. EDX specifies optional hints; it does not change the architectural behavior of the instruction. For the Pentium 4 processor (family 15, model 3), no extensions or hints are defined. Undefined hints in EDX are ignored by the processor; undefined extensions in ECX raises a general protection fault.

The address range must use memory of the write-back type. Only write-back memory will correctly trigger the monitoring hardware. Additional information on determining what address range to use in order to prevent false wake-ups is described in Chapter 8, "Multiple-Processor Management" of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

The MONITOR instruction is ordered as a load operation with respect to other memory transactions. The instruction is subject to the permission checking and faults associated with a byte load. Like a load, MONITOR sets the A-bit but not the D-bit in page tables.

The MONITOR CPUID feature flag (ECX bit 3; CPUID executed EAX = 1) indicates the availability of MONITOR and MWAIT in the processor. When set, MONITOR may be executed only at privilege level 0 (use at any other privilege level results in an invalid-opcode exception). The operating system or system BIOS may disable this instruction by using the IA32_MISC_ENABLES MSR; disabling MONITOR clears the CPUID feature flag and causes execution to generate an illegal opcode exception.

The instruction’s operation is the same in non-64-bit modes and 64-bit mode.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 C8</td>
<td>MONITOR</td>
<td>Valid</td>
<td>Valid</td>
<td>Sets up a linear address range to be monitored by hardware and activates the monitor. The address range should be a write-back memory caching type. The address is DS:EAX (DS:RAX in 64-bit mode).</td>
</tr>
</tbody>
</table>
Operation
MONITOR sets up an address range for the monitor hardware using the content of EAX (RAX in 64-bit mode) as an effective address and puts the monitor hardware in armed state. Always use memory of the write-back caching type. A store to the specified address range will trigger the monitor hardware. The content of ECX and EDX are used to communicate other information to the monitor hardware.

Intel C/C++ Compiler Intrinsic Equivalent
MONITOR  void _mm_monitor(void const *p, unsigned extensions,unsigned hints)

Numeric Exceptions
None

Protected Mode Exceptions
#GP(0) If the value in EAX is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
If ECX ≠ 0.
#SS(0) If the value in EAX is outside the SS segment limit.
#PF(fault-code) For a page fault.
#UD If CPUID.01H:ECX.MONITOR[bit 3] = 0.
If current privilege level is not 0.

Real Address Mode Exceptions
#GP If the CS, DS, ES, FS, or GS register is used to access memory and the value in EAX is outside of the effective address space from 0 to FFFFH.
If ECX ≠ 0.
#SS If the SS register is used to access memory and the value in EAX is outside of the effective address space from 0 to FFFFH.
#UD If CPUID.01H:ECX.MONITOR[bit 3] = 0.

Virtual 8086 Mode Exceptions
#UD The MONITOR instruction is not recognized in virtual-8086 mode (even if CPUID.01H:ECX.MONITOR[bit 3] = 1).

Compatibility Mode Exceptions
Same exceptions as in protected mode.
64-Bit Mode Exceptions

#GP(0) If the linear address of the operand in the CS, DS, ES, FS, or GS segment is in a non-canonical form.
   If RCX ≠ 0.
#SS(0) If the SS register is used to access memory and the value in EAX is in a non-canonical form.
#PF(fault-code) For a page fault.
#UD If the current privilege level is not 0.
   If CPUID.01H:ECX.MONITOR[bit 3] = 0.
## MOV—Move

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>88 /r</td>
<td>MOV r/m8,r8</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r8 to r/m8.</td>
</tr>
<tr>
<td>REX + 88 /r</td>
<td>MOV r/m8***,r8***</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r8 to r/m8.</td>
</tr>
<tr>
<td>89 /r</td>
<td>MOV r/m16,r16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r16 to r/m16.</td>
</tr>
<tr>
<td>89 /r</td>
<td>MOV r/m32,r32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r32 to r/m32.</td>
</tr>
<tr>
<td>REX.W + 89 /r</td>
<td>MOV r/m64,r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r64 to r/m64.</td>
</tr>
<tr>
<td>8A /r</td>
<td>MOV r8,r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r/m8 to r8.</td>
</tr>
<tr>
<td>REX + 8A /r</td>
<td>MOV r8***,r/m8***</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r/m8 to r8.</td>
</tr>
<tr>
<td>8B /r</td>
<td>MOV r16,r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r/m16 to r16.</td>
</tr>
<tr>
<td>8B /r</td>
<td>MOV r32,r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r/m32 to r32.</td>
</tr>
<tr>
<td>REX.W + 8B /r</td>
<td>MOV r64,r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r/m64 to r64.</td>
</tr>
<tr>
<td>8C /r</td>
<td>MOV r/m16,Sreg**</td>
<td>Valid</td>
<td>Valid</td>
<td>Move segment register to r/m16.</td>
</tr>
<tr>
<td>REX.W + 8C /r</td>
<td>MOV r/m64,Sreg**</td>
<td>Valid</td>
<td>Valid</td>
<td>Move zero extended 16-bit segment register to r/m64.</td>
</tr>
<tr>
<td>8E /r</td>
<td>MOV Sreg,r/m16**</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r/m16 to segment register.</td>
</tr>
<tr>
<td>REX.W + 8E /r</td>
<td>MOV Sreg,r/m64**</td>
<td>Valid</td>
<td>Valid</td>
<td>Move lower 16 bits of r/m64 to segment register.</td>
</tr>
<tr>
<td>A0</td>
<td>MOV AL,moffs8*</td>
<td>Valid</td>
<td>Valid</td>
<td>Move byte at (seg:offset) to AL.</td>
</tr>
<tr>
<td>REX.W + A0</td>
<td>MOV AL,moffs8*</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move byte at (offset) to AL.</td>
</tr>
<tr>
<td>A1</td>
<td>MOV AX,moffs16*</td>
<td>Valid</td>
<td>Valid</td>
<td>Move word at (seg:offset) to AX.</td>
</tr>
<tr>
<td>A1</td>
<td>MOV EAX,moffs32*</td>
<td>Valid</td>
<td>Valid</td>
<td>Move doubleword at (seg:offset) to EAX.</td>
</tr>
<tr>
<td>REX.W + A1</td>
<td>MOV RAX,moffs64*</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move quadword at (offset) to RAX.</td>
</tr>
<tr>
<td>A2</td>
<td>MOV moffs8,AL</td>
<td>Valid</td>
<td>Valid</td>
<td>Move AL to (seg:offset).</td>
</tr>
<tr>
<td>REX.W + A2</td>
<td>MOV moffs8***,AL</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move AL to (offset).</td>
</tr>
<tr>
<td>A3</td>
<td>MOV moffs16*,AX</td>
<td>Valid</td>
<td>Valid</td>
<td>Move AX to (seg:offset).</td>
</tr>
</tbody>
</table>
MOV—Move

Description

Copies the second operand (source operand) to the first operand (destination operand). The source operand can be an immediate value, general-purpose register, segment register, or memory location; the destination register can be a general-purpose register, segment register, or memory location. Both operands must be the same size, which can be a byte, a word, a doubleword, or a quadword.

The MOV instruction cannot be used to load the CS register. Attempting to do so results in an invalid opcode exception (#UD). To load the CS register, use the far JMP, CALL, or RET instruction.

If the destination operand is a segment register (DS, ES, FS, GS, or SS), the source operand must be a valid segment selector. In protected mode, moving a segment
selector into a segment register automatically causes the segment descriptor information associated with that segment selector to be loaded into the hidden (shadow) part of the segment register. While loading this information, the segment selector and segment descriptor information is validated (see the “Operation” algorithm below). The segment descriptor data is obtained from the GDT or LDT entry for the specified segment selector.

A NULL segment selector (values 0000-0003) can be loaded into the DS, ES, FS, and GS registers without causing a protection exception. However, any subsequent attempt to reference a segment whose corresponding segment register is loaded with a NULL value causes a general protection exception (#GP) and no memory reference occurs.

Loading the SS register with a MOV instruction inhibits all interrupts until after the execution of the next instruction. This operation allows a stack pointer to be loaded into the ESP register with the next instruction (MOV ESP, stack-pointer value) before an interrupt occurs. Be aware that the LSS instruction offers a more efficient method of loading the SS and ESP registers.

When operating in 32-bit mode and moving data between a segment register and a general-purpose register, the 32-bit IA-32 processors do not require the use of the 16-bit operand-size prefix (a byte with the value 66H) with this instruction, but most assemblers will insert it if the standard form of the instruction is used (for example, MOV DS, AX). The processor will execute this instruction correctly, but it will usually require an extra clock. With most assemblers, using the instruction form MOV DS, EAX will avoid this unneeded 66H prefix. When the processor executes the instruction with a 32-bit general-purpose register, it assumes that the 16 least-significant bits of the general-purpose register are the destination or source operand. If the register is a destination operand, the resulting value in the two high-order bytes of the register is implementation dependent. For the Pentium 4, Intel Xeon, and P6 family processors, the two high-order bytes are filled with zeros; for earlier 32-bit IA-32 processors, the two high order bytes are undefined.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

1. If a code instruction breakpoint (for debug) is placed on an instruction located immediately after a MOV SS instruction, the breakpoint may not be triggered. However, in a sequence of instructions that load the SS register, only the first instruction in the sequence is guaranteed to delay an interrupt.

In the following sequence, interrupts may be recognized before MOV ESP, EBP executes:

- MOV SS, EDX
- MOV SS, EAX
- MOV ESP, EBP

MOV—Move
Operation

DEST ← SRC;

Loading a segment register while in protected mode results in special checks and actions, as described in the following listing. These checks are performed on the segment selector and the segment descriptor to which it points.

IF SS is loaded
THEN
  IF segment selector is NULL
    THEN #GP(0); FI;
  IF segment selector index is outside descriptor table limits
    or segment selector's RPL ≠ CPL
    or segment is not a writable data segment
    or DPL ≠ CPL
    THEN #GP(selector); FI;
  IF segment not marked present
    THEN #SS(selector);
    ELSE
      SS ← segment selector;
      SS ← segment descriptor; FI;
  FI;

IF DS, ES, FS, or GS is loaded with non-NULL selector
THEN
  IF segment selector index is outside descriptor table limits
    or segment is not a data or readable code segment
    or ((segment is a data or nonconforming code segment)
      and (both RPL and CPL > DPL))
    THEN #GP(selector); FI;
  IF segment not marked present
    THEN #NP(selector);
    ELSE
      SegmentRegister ← segment selector;
      SegmentRegister ← segment descriptor; FI;
  FI;

IF DS, ES, FS, or GS is loaded with NULL selector
THEN
  SegmentRegister ← segment selector;
  SegmentRegister ← segment descriptor; FI;
Flags Affected
None.

Protected Mode Exceptions
#GP(0)  If attempt is made to load SS register with NULL segment selector.
If the destination operand is in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

#GP(selector)  If segment selector index is outside descriptor table limits.
If the SS register is being loaded and the segment selector's RPL and the segment descriptor's DPL are not equal to the CPL.
If the SS register is being loaded and the segment pointed to is a non-writable data segment.
If the DS, ES, FS, or GS register is being loaded and the segment pointed to is not a data or readable code segment.
If the DS, ES, FS, or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#SS(selector)  If the SS register is being loaded and the segment pointed to is marked not present.

#NP  If the DS, ES, FS, or GS register is being loaded and the segment pointed to is marked not present.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If attempt is made to load the CS register.
If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#UD  If attempt is made to load the CS register.
If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made.
- **#UD**: If attempt is made to load the CS register.
  - If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

- **#GP(0)**: If the memory address is in a non-canonical form.
  - If an attempt is made to load SS register with NULL segment selector when CPL = 3.
  - If an attempt is made to load SS register with NULL segment selector when CPL < 3 and CPL ≠ RPL.
- **#GP(selector)**: If segment selector index is outside descriptor table limits.
  - If the memory access to the descriptor table is non-canonical.
  - If the SS register is being loaded and the segment selector's RPL and the segment descriptor's DPL are not equal to the CPL.
  - If the SS register is being loaded and the segment pointed to is a non-writable data segment.
  - If the DS, ES, FS, or GS register is being loaded and the segment pointed to is not a data or readable code segment.
  - If the DS, ES, FS, or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.
- **#SS(0)**: If the stack address is in a non-canonical form.
- **#SS(selector)**: If the SS register is being loaded and the segment pointed to is marked not present.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If attempt is made to load the CS register.
  - If the LOCK prefix is used.
MOV—Move to/from Control Registers

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 20/r</td>
<td>MOV r32, CR0–CR7</td>
<td>N.E.</td>
<td>Valid</td>
<td>Move control register to r32</td>
</tr>
<tr>
<td>0F 20/r</td>
<td>MOV r64, CR0–CR7</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move extended control register to r64.</td>
</tr>
<tr>
<td>REX.R + 0F 20/0</td>
<td>MOV r64, CR8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move extended CR8 to r64.</td>
</tr>
<tr>
<td>0F 22/r</td>
<td>MOV CR0–CR7, r32</td>
<td>N.E.</td>
<td>Valid</td>
<td>Move r32 to control register</td>
</tr>
<tr>
<td>0F 22/r</td>
<td>MOV CR0–CR7, r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r64 to extended control register.</td>
</tr>
<tr>
<td>REX.R + 0F 22/0</td>
<td>MOV CR8, r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r64 to extended CR8.</td>
</tr>
</tbody>
</table>

NOTE:
1. MOV CR* instructions, except for MOV CR8, are serializing instructions. MOV CR8 is not architecturally defined as a serializing instruction. For more information, see Chapter 8 in Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A.

Description

Moves the contents of a control register (CR0, CR2, CR3, CR4, or CR8) to a general-purpose register or the contents of a general purpose register to a control register. The operand size for these instructions is always 32 bits in non-64-bit modes, regardless of the operand-size attribute. (See "Control Registers" in Chapter 2 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A, for a detailed description of the flags and fields in the control registers.) This instruction can be executed only when the current privilege level is 0.

At the opcode level, the reg field within the ModR/M byte specifies which of the control registers is loaded or read. The 2 bits in the mod field are ignored. The r/m field specifies the general-purpose register loaded or read. Attempts to reference CR1, CR5, CR6, CR7, and CR9–CR15 result in undefined opcode (#UD) exceptions.

When loading control registers, programs should not attempt to change the reserved bits; that is, always set reserved bits to the value previously read. An attempt to change CR4’s reserved bits will cause a general protection fault. Reserved bits in CR0 and CR3 remain clear after any load of those registers; attempts to set them have no impact. On Pentium 4, Intel Xeon and P6 family processors, CR0.ET remains set after any load of CR0; attempts to clear this bit have no impact.

These instructions have the following side effect:

- When writing to control register CR3, all non-global TLB entries are flushed (see "Caching Translation Information" in Chapter 4 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A).
The following side effects are implementation specific for the Pentium 4, Intel Xeon, and P6 processor family. Software should not depend on this functionality in all Intel 64 or IA-32 processors:

- When modifying any of the paging flags in the control registers (PE and PG in register CR0 and PGE, PSE, and PAE in register CR4), all TLB entries are flushed, including global entries.
- If the PG flag is set to 1 and control register CR4 is written to set the PAE flag to 1 (to enable the physical address extension mode), the pointers in the page-directory pointers table (PDPT) are loaded into the processor (into internal, non-architectural registers).
- If the PAE flag is set to 1 and the PG flag set to 1, writing to control register CR3 will cause the PDPTRs to be reloaded into the processor. If the PAE flag is set to 1 and control register CR0 is written to set the PG flag, the PDPTRs are reloaded into the processor.

In 64-bit mode, the instruction’s default operation size is 64 bits. The REX.R prefix must be used to access CR8. Use of REX.B permits access to additional registers (R8-R15). Use of the REX.W prefix or 66H prefix is ignored. Use of the REX.R prefix to specify a register other than CR8 causes an invalid-opcode exception. See the summary chart at the beginning of this section for encoding data and limits.

See "Changes to Instruction Behavior in VMX Non-Root Operation" in Chapter 22 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*, for more information about the behavior of this instruction in VMX non-root operation.

**Operation**

DEST ← SRC;

**Flags Affected**

The OF, SF, ZF, AF, PF, and CF flags are undefined.

**Protected Mode Exceptions**

- **#GP(0)** If the current privilege level is not 0. If an attempt is made to write invalid bit combinations in CR0 (such as setting the PG flag to 1 when the PE flag is set to 0, or setting the CD flag to 0 when the NW flag is set to 1). If an attempt is made to write a 1 to any reserved bit in CR4. If any of the reserved bits are set in the page-directory pointers table (PDPT) and the loading of a control register causes the PDPT to be loaded into the processor.
- **#UD** If the LOCK prefix is used. If an attempt is made to access CR1, CR5, CR6, or CR7.
Real-Address Mode Exceptions

#GP If an attempt is made to write a 1 to any reserved bit in CR4.
   If an attempt is made to write invalid bit combinations in CR0
      (such as setting the PG flag to 1 when the PE flag is set to 0).
#UD If the LOCK prefix is used.
   If an attempt is made to access CR1, CR5, CR6, or CR7.

Virtual-8086 Mode Exceptions

#GP(0) These instructions cannot be executed in virtual-8086 mode.

Compatibility Mode Exceptions

#GP(0) If the current privilege level is not 0.
   If an attempt is made to write invalid bit combinations in CR0
      (such as setting the PG flag to 1 when the PE flag is set to 0, or
      setting the CD flag to 0 when the NW flag is set to 1).
   If an attempt is made to write a 1 to any reserved bit in CR3.
   If an attempt is made to leave IA-32e mode by clearing
      CR4.PAE[bit 5].
#UD If the LOCK prefix is used.
   If an attempt is made to access CR1, CR5, CR6, or CR7.

64-Bit Mode Exceptions

#GP(0) If the current privilege level is not 0.
   If an attempt is made to write invalid bit combinations in CR0
      (such as setting the PG flag to 1 when the PE flag is set to 0, or
      setting the CD flag to 0 when the NW flag is set to 1).
   Attempting to clear CR0.PG[bit 31].
   If an attempt is made to write a 1 to any reserved bit in CR4.
   If an attempt is made to write a 1 to any reserved bit in CR8.
   If an attempt is made to write a 1 to any reserved bit in CR3.
   If an attempt is made to leave IA-32e mode by clearing
      CR4.PAE[bit 5].
#UD If the LOCK prefix is used.
   If an attempt is made to access CR1, CR5, CR6, or CR7.
   If the REX.R prefix is used to specify a register other than CR8.
MOV—Move to/from Debug Registers

### Description

Moves the contents of a debug register (DR0, DR1, DR2, DR3, DR4, DR5, DR6, or DR7) to a general-purpose register or vice versa. The operand size for these instructions is always 32 bits in non-64-bit modes, regardless of the operand-size attribute. (See Chapter 20, "Introduction to Virtual-Machine Extensions", of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, for a detailed description of the flags and fields in the debug registers.)

The instructions must be executed at privilege level 0 or in real-address mode.

When the debug extension (DE) flag in register CR4 is clear, these instructions operate on debug registers in a manner that is compatible with Intel386 and Intel486 processors. In this mode, references to DR4 and DR5 refer to DR6 and DR7, respectively. When the DE flag in CR4 is set, attempts to reference DR4 and DR5 result in an undefined opcode (#UD) exception. (The CR4 register was added to the IA-32 Architecture beginning with the Pentium processor.)

At the opcode level, the reg field within the ModR/M byte specifies which of the debug registers is loaded or read. The two bits in the mod field are ignored. The r/m field specifies the general-purpose register loaded or read.

In 64-bit mode, the instruction’s default operation size is 64 bits. Use of the REX.B prefix permits access to additional registers (R8–R15). Use of the REX.W or 66H prefix is ignored. Use of the REX.R prefix causes an invalid-opcode exception. See the summary chart at the beginning of this section for encoding data and limits.

### Operation

\[ \text{IF } ((\text{DE} = 1) \text{ and (SRC or DEST = DR4 or DR5})) \]  
\[ \text{THEN} \]  
\[ \text{#UD;} \]  
\[ \text{ELSE} \]  
\[ \text{DEST} \leftarrow \text{SRC;} \]  
\[ \text{FI}; \]
INSTRUCTION SET REFERENCE, A-M

Flags Affected
The OF, SF, ZF, AF, PF, and CF flags are undefined.

Protected Mode Exceptions
- **#GP(0)** If the current privilege level is not 0.
- **#UD** If CR4.DE[bit 3] = 1 (debug extensions) and a MOV instruction is executed involving DR4 or DR5.
  - If the LOCK prefix is used.
- **#DB** If any debug register is accessed while the DR7.GD[bit 13] = 1.

Real-Address Mode Exceptions
- **#UD** If CR4.DE[bit 3] = 1 (debug extensions) and a MOV instruction is executed involving DR4 or DR5.
  - If the LOCK prefix is used.
- **#DB** If any debug register is accessed while the DR7.GD[bit 13] = 1.

Virtual-8086 Mode Exceptions
- **#GP(0)** The debug registers cannot be loaded or read when in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
- **#GP(0)** If the current privilege level is not 0.
- **#UD** If CR4.DE[bit 3] = 1 (debug extensions) and a MOV instruction is executed involving DR4 or DR5.
  - If the LOCK prefix is used.
  - If the REX.R prefix is used.
- **#DB** If any debug register is accessed while the DR7.GD[bit 13] = 1.
MOVAPD—Move Aligned Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 28 /r</td>
<td>MOVAPD xmm1,</td>
<td>Valid</td>
<td>Valid</td>
<td>Move packed double-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td></td>
<td>xmm2/m128</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 29 /r</td>
<td>MOVAPD</td>
<td>Valid</td>
<td>Valid</td>
<td>Move packed double-precision floating-point values from xmm1 to xmm2/m128.</td>
</tr>
<tr>
<td></td>
<td>xmm2/m128, xmm1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Description
Moves a double quadword containing two packed double-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, to store the contents of an XMM register into a 128-bit memory location, or to move data between two XMM registers. When the source or destination operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

To move double-precision floating-point values to and from unaligned memory locations, use the MOVUPD instruction.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST ← SRC;
(* #GP if SRC or DEST unaligned memory operand *)

Intel C/C++ Compiler Intrinsic Equivalent

__m128 _mm_load_pd(double * p)
void _mm_store_pd(double *p, __m128 a)

SIMD Floating-Point Exceptions
None.
Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
INSTRUCTION SET REFERENCE, A-M

#UD

If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
MOVAPS—Move Aligned Packed Single-Precision Floating-Point Values

Description
Moves a double quadword containing four packed single-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, to store the contents of an XMM register into a 128-bit memory location, or to move data between two XMM registers. When the source or destination operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) is generated.

To move packed single-precision floating-point values to or from unaligned memory locations, use the MOVUPS instruction.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST ← SRC;
(* #GP if SRC or DEST unaligned memory operand *)

Intel C/C++ Compiler Intrinsic Equivalent

__m128 _mm_load_ps (float * p)
void _mm_store_ps (float *p, __m128 a)

SIMD Floating-Point Exceptions
None.
INSTRUCTION SET REFERENCE, A-M

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX:SSE[bit 25] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX:SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
MOVAPS—Move Aligned Packed Single-Precision Floating-Point Values

#UD

If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
MOVBE—Move Data After Swapping Bytes

**Description**

Performs a byte swap operation on the data copied from the second operand (source operand) and store the result in the first operand (destination operand). The source operand can be a general-purpose register, or memory location; the destination register can be a general-purpose register, or a memory location; however, both operands can not be registers, and only one operand can be a memory location. Both operands must be the same size, which can be a word, a doubleword or quadword.

The MOVBE instruction is provided for swapping the bytes on a read from memory or on a write to memory; thus providing support for converting little-endian values to big-endian format and vice versa.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\text{TEMP} \leftarrow \text{SRC}
\]

IF (OperandSize = 16)

\[
\text{THEN}
\]

\[
\begin{align*}
\text{DEST}[7:0] & \leftarrow \text{TEMP}[15:8]; \\
\text{DEST}[15:8] & \leftarrow \text{TEMP}[7:0]; \\
\text{ELSE IF} & \quad (\text{OperandSize} = 32) \\
\text{DEST}[7:0] & \leftarrow \text{TEMP}[31:24];
\end{align*}
\]

<table>
<thead>
<tr>
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<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 F0 /r</td>
<td>MOVBE r16, m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse byte order in m16 and move to r16</td>
</tr>
<tr>
<td>0F 38 F0 /r</td>
<td>MOVBE r32, m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse byte order in m32 and move to r32</td>
</tr>
<tr>
<td>REX.W + 0F 38 F0 /r</td>
<td>MOVBE r64, m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Reverse byte order in m64 and move to r64.</td>
</tr>
<tr>
<td>0F 38 F1 /r</td>
<td>MOVBE m16, r16</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse byte order in r16 and move to m16</td>
</tr>
<tr>
<td>0F 38 F1 /r</td>
<td>MOVBE m32, r32</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse byte order in r32 and move to m32</td>
</tr>
<tr>
<td>REX.W + 0F 38 F1 /r</td>
<td>MOVBE m64, r64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Reverse byte order in r64 and move to m64.</td>
</tr>
</tbody>
</table>
DEST[15:8] ← TEMP[23:16];
DEST[23:16] ← TEMP[15:8];
DEST[31:23] ← TEMP[7:0];
ELSE IF (OperandSize = 64)
DEST[7:0] ← TEMP[63:56];
DEST[15:8] ← TEMP[55:48];
DEST[23:16] ← TEMP[47:40];
DEST[39:32] ← TEMP[31:24];
DEST[47:40] ← TEMP[23:16];
DEST[55:48] ← TEMP[15:8];
DEST[63:56] ← TEMP[7:0];
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the destination operand is in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If CPUID.01H:ECX.MOVBE[bit 22] = 0.
If the LOCK prefix is used.
If REP (F3H) prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If CPUID.01H:ECX.MOVBE[bit 22] = 0.
If the LOCK prefix is used.
If REP (F3H) prefix is used.
Virtual-8086 Mode Exceptions

- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)**: If a page fault occurs.
- **#UD**: If CPUID.01H:ECX.MOVBE[bit 22] = 0.
  - If the LOCK prefix is used.
  - If REP (F3H) prefix is used.
  - If REPNE (F2H) prefix is used and CPUID.01H:ECX.SSE4.2[bit 20] = 0.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

- **#GP(0)**: If the memory address is in a non-canonical form.
- **#SS(0)**: If the stack address is in a non-canonical form.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If CPUID.01H:ECX.MOVBE[bit 22] = 0.
  - If the LOCK prefix is used.
  - If REP (F3H) prefix is used.
MOVD/MOVQ—Move Doubleword/Move Quadword

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 6E /r</td>
<td>MOVD mm, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move doubleword from r/m32 to mm.</td>
</tr>
<tr>
<td>REX.W + 0F 6E /r</td>
<td>MOVQ mm, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move quadword from r/m64 to mm.</td>
</tr>
<tr>
<td>0F 7E /r</td>
<td>MOVQ r/m32, mm</td>
<td>Valid</td>
<td></td>
<td>Move doubleword from mm to r/m32.</td>
</tr>
<tr>
<td>REX.W + 0F 7E /r</td>
<td>MOVQ r/m64, mm</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move quadword from mm to r/m64.</td>
</tr>
<tr>
<td>66 0F 6E /r</td>
<td>MOVD xmm, r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Move doubleword from r/m32 to xmm.</td>
</tr>
<tr>
<td>66 REX.W 0F 6E /r</td>
<td>MOVQ xmm, r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move quadword from r/m64 to xmm.</td>
</tr>
<tr>
<td>66 0F 7E /r</td>
<td>MOVQ r/m32, xmm</td>
<td>Valid</td>
<td>Valid</td>
<td>Move doubleword from xmm register to r/m32.</td>
</tr>
<tr>
<td>66 REX.W 0F 7E /r</td>
<td>MOVQ r/m64, xmm</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move quadword from xmm register to r/m64.</td>
</tr>
</tbody>
</table>

**Description**

Copies a doubleword from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be general-purpose registers, MMX technology registers, XMM registers, or 32-bit memory locations. This instruction can be used to move a doubleword to and from the low doubleword of an MMX technology register and a general-purpose register or a 32-bit memory location, or to and from the low doubleword of an XMM register and a general-purpose register or a 32-bit memory location. The instruction cannot be used to transfer data between MMX technology registers, between XMM registers, between general-purpose registers, or between memory locations.

When the destination operand is an MMX technology register, the source operand is written to the low doubleword of the register, and the register is zero-extended to 64 bits. When the destination operand is an XMM register, the source operand is written to the low doubleword of the register, and the register is zero-extended to 128 bits.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.
INSTRUCTION SET REFERENCE, A-M

Operation

MOVD instruction when destination operand is MMX technology register:

\[ \text{DEST}[31:0] \leftarrow \text{SRC}; \]
\[ \text{DEST}[63:32] \leftarrow 00000000H; \]

MOVD instruction when destination operand is XMM register:

\[ \text{DEST}[31:0] \leftarrow \text{SRC}; \]
\[ \text{DEST}[127:32] \leftarrow 000000000000000000000000H; \]

MOVD instruction when source operand is MMX technology or XMM register:

\[ \text{DEST} \leftarrow \text{SRC}[31:0]; \]

MOVQ instruction when destination operand is XMM register:

\[ \text{DEST}[63:0] \leftarrow \text{SRC}[63:0]; \]
\[ \text{DEST}[127:64] \leftarrow 0000000000000000H; \]

MOVQ instruction when destination operand is r/m64:

\[ \text{DEST}[63:0] \leftarrow \text{SRC}[63:0]; \]

MOVQ instruction when source operand is XMM register or r/m64:

\[ \text{DEST} \leftarrow \text{SRC}[63:0]; \]

Intel C/C++ Compiler Intrinsic Equivalent

\[
\begin{align*}
\text{MOVD} & \quad \text{__m64 } \_\text{mm_cvtsi32}_\text{si64}(\text{int } i) \\
\text{MOVD} & \quad \text{int } \_\text{mm Cvtsi64}_\text{si32}(\_\text{m64} m) \\
\text{MOVD} & \quad \text{__m128i } \_\text{mm Cvtsi32}_\text{si128}(\text{int } a) \\
\text{MOVD} & \quad \text{int } \_\text{mm Cvtsi128}_\text{si32}(\_\text{m128i } a)
\end{align*}
\]

Flags Affected

None.

SIMD Floating-Point Exceptions

None.

Protected Mode Exceptions

#GP(0) If the destination operand is in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD  If CR0.EM[bit 2] = 1.

128-bit operations will generate #UD only if CR4.OSFXSR[bit 9] = 0. Execution of 128-bit instructions on a non-SSE2 capable processor (one that is MMX technology capable) will result in the instruction operating on the mm registers, not #UD.
If the LOCK prefix is used.

#NM  If CR0.TS[bit 3] = 1.

#MF  (MMX register operations only) If there is a pending FPU exception.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP  If any part of the operand lies outside of the effective address space from 0 to FFFFH.

#UD  If CR0.EM[bit 2] = 1.

128-bit operations will generate #UD only if CR4.OSFXSR[bit 9] = 0. Execution of 128-bit instructions on a non-SSE2 capable processor (one that is MMX technology capable) will result in the instruction operating on the mm registers, not #UD.
If the LOCK prefix is used.

#NM  If CR0.TS[bit 3] = 1.

#MF  (MMX register operations only) If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.
MOVQ—Move Quadword

If CR0.E[bit 2] = 1.
(XMM register operations only) if CR4.OSFXSR[bit 9] = 0.
(XMM register operations only) if CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#NM If CR0.TS[bit 3] = 1.

#MF (MMX register operations only) If there is a pending FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MOVDDUP—Move One Double-FP and Duplicate

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 12 /r</td>
<td>MOVDDUP xmm1, xmm2/m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Move one double-precision floating-point value from the lower 64-bit operand in xmm2/m64 to xmm1 and duplicate.</td>
</tr>
</tbody>
</table>

**Description**

The linear address corresponds to the address of the least-significant byte of the referenced memory data. When a memory address is indicated, the 8 bytes of data at memory location m64 are loaded. When the register-register form of this operation is used, the lower half of the 128-bit source register is duplicated and copied into the 128-bit destination register. See Figure 3-15.

**Figure 3-15. MOVDDUP—Move One Double-FP and Duplicate**

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

IF (Source == m64)
THEN
  (* Load instruction *)
  xmm1[63:0] = m64;

MOVDDUP—Move One Double-FP and Duplicate  Vol. 2A  3-665
INSTRUCTION SET REFERENCE, A-M

xmm1[127:64] = m64;
ELSE
  (* Move instruction *)
  xmm1[63:0] = xmm2[63:0];
  xmm1[127:64] = xmm2[63:0];
FI;

Intel C/C++ Compiler Intrinsic Equivalent

MOVDDUP __m128d __mm_movedup_pd(__m128d a)
__m128d __mm_loadup_pd(double const * dp)

Exceptions
None

Numeric Exceptions
None

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
**Virtual 8086 Mode Exceptions**

- **GP(0)**: If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:ECX.SSE3[bit 0] = 0.
  - If the LOCK prefix is used.
- **#PF(fault-code)**: For a page fault.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

- **#SS(0)**: If a memory address referencing the SS segment is in a non-canonical form.
- **#GP(0)**: If the memory address is in a non-canonical form.
- **#PF(fault-code)**: For a page fault.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.SSE3(ECX, bit 0) is 0.
  - If the LOCK prefix is used.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MOVDQA—Move Aligned Double Quadword

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 6F/r</td>
<td>MOVDQA xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Move aligned double quadword from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>66 0F 7F/r</td>
<td>MOVDQA xmm2/m128, xmm1</td>
<td>Valid</td>
<td>Valid</td>
<td>Move aligned double quadword from xmm1 to xmm2/m128.</td>
</tr>
</tbody>
</table>

Description

Moves a double quadword from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, to store the contents of an XMM register into a 128-bit memory location, or to move data between two XMM registers. When the source or destination operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

To move a double quadword to or from unaligned memory locations, use the MOVDQU instruction.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

DEST ← SRC;
(* #GP if SRC or DEST unaligned memory operand *)

Intel C/C++ Compiler Intrinsic Equivalent

MOVDQA __m128i _mm_load_si128 (__m128i *p)
MOVDQA void _mm_store_si128 (__m128i *p, __m128i a)

SIMD Floating-Point Exceptions

None.

Protected Mode Exceptions

#PF(fault-code) If a page fault occurs.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
MOVDQA—Move Aligned Double Quadword

INSTRUCTION SET REFERENCE, A-M

#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
MOVDQU—Move Unaligned Double Quadword

Description

Moves a double quadword from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, to store the contents of an XMM register into a 128-bit memory location, or to move data between two XMM registers. When the source or destination operand is a memory operand, the operand may be unaligned on a 16-byte boundary without causing a general-protection exception (#GP) to be generated.

To move a double quadword to or from memory locations that are known to be aligned on 16-byte boundaries, use the MOVDQA instruction.

While executing in 16-bit addressing mode, a linear address for a 128-bit data access that overlaps the end of a 16-bit segment is not allowed and is defined as reserved behavior. A specific processor implementation may or may not generate a general-protection exception (#GP) in this situation, and the address that spans the end of the segment may or may not wrap around to the beginning of the segment.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

DEST ← SRC;

Intel C/C++ Compiler Intrinsic Equivalent

MOVDQU void _mm_storeu_si128 (__m128i *p, __m128i a)
MOVDQU __m128i _mm_loadu_si128 (__m128i *p)

SIMD Floating-Point Exceptions

None.
Protected Mode Exceptions

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
#PF(fault-code) If a page fault occurs.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
INSTRUCTION SET REFERENCE, A-M

#UD  If CR0.EM[bit 2] = 1.
     If CR4.OSFXSR[bit 9] = 0.
     If CPUID.01H:EDX.SSE2[bit 26] = 0.
     If the LOCK prefix is used.
MOVDQ2Q—Move Quadword from XMM to MMX Technology Register

**Description**

Moves the low quadword from the source operand (second operand) to the destination operand (first operand). The source operand is an XMM register and the destination operand is an MMX technology register.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the MOVDQ2Q instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\text{DEST} \leftarrow \text{SRC}[63:0];
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVDQ2Q _m64 _mm_movepi64_pi64 ( _m128i a)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

<table>
<thead>
<tr>
<th>Exception Type</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>#NM</td>
<td>If CR0.TS[bit 3] = 1.</td>
</tr>
<tr>
<td>#UD</td>
<td>If CR0.EM[bit 2] = 1.</td>
</tr>
<tr>
<td></td>
<td>If CR4.OSFXSR[bit 9] = 0.</td>
</tr>
<tr>
<td></td>
<td>If CPUID.01H:EDX.SSE2[bit 26] = 0.</td>
</tr>
<tr>
<td></td>
<td>If the LOCK prefix is used.</td>
</tr>
<tr>
<td>#MF</td>
<td>If there is a pending x87 FPU exception.</td>
</tr>
</tbody>
</table>

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.
Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**MOVHLPS— Move Packed Single-Precision Floating-Point Values High to Low**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 12 /r</td>
<td>MOVHLPS xmm1, xmm2</td>
<td>Valid</td>
<td>Valid</td>
<td>Move two packed single-precision floating-point values from high quadword of xmm2 to low quadword of xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Moves two packed single-precision floating-point values from the high quadword of the source operand (second operand) to the low quadword of the destination operand (first operand). The high quadword of the destination operand is left unchanged.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[63:0] ← SRC[127:64];
(* DEST[127:64] unchanged *)

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVHLPS _m128 _mm_movehl_ps(_m128 a, _m128 b)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- #NM: If CR0.TS[bit 3] = 1.
- #UD: If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.

**Real Address Mode Exceptions**

Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-M

Virtual 8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
MOVHPD—Move High Packed Double-Precision Floating-Point Value

**Description**

Moves a double-precision floating-point value from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be an XMM register or a 64-bit memory location. This instruction allows a double-precision floating-point value to be moved to and from the high quadword of an XMM register and memory. It cannot be used for register to register or memory to memory moves. When the destination operand is an XMM register, the low quadword of the register remains unchanged.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

MOVHPD instruction for memory to XMM move:

DEST[127:64] ← SRC;

(* DEST[63:0] unchanged *)

MOVHPD instruction for XMM to memory move:

DEST ← SRC[127:64];

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVHPD __m128d _mm_loadh_pd (__m128d a, double *p)

MOVHPD void _mm_storeh_pd (double *p, __m128d a)

**SIMD Floating-Point Exceptions**

None.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 16 /r MOVHPD xmm, m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Move double-precision floating-point value from m64 to high quadword of xmm.</td>
<td></td>
</tr>
<tr>
<td>66 0F 17 /r MOVHPD m64, xmm</td>
<td>Valid</td>
<td>Valid</td>
<td>Move double-precision floating-point value from high quadword of xmm to m64.</td>
<td></td>
</tr>
</tbody>
</table>
Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE2[bit 26] = 0.

If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE2[bit 26] = 0.

If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.
MOVHPD—Move High Packed Double-Precision Floating-Point Value

If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
### MOVHPS—Move High Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 16 /r</td>
<td>MOVHPS xmm, m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Move two packed single-precision floating-point values from m64 to high quadword of xmm.</td>
</tr>
<tr>
<td>0F 17 /r</td>
<td>MOVHPS m64, xmm</td>
<td>Valid</td>
<td>Valid</td>
<td>Move two packed single-precision floating-point values from high quadword of xmm to m64.</td>
</tr>
</tbody>
</table>

**Description**

Moves two packed single-precision floating-point values from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be an XMM register or a 64-bit memory location. This instruction allows two single-precision floating-point values to be moved to and from the high quadword of an XMM register and memory. It cannot be used for register to register or memory to memory moves. When the destination operand is an XMM register, the low quadword of the register remains unchanged.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

MOVHPS instruction for memory to XMM move:

```
DEST[127:64] ← SRC;
(* DEST[63:0] unchanged *)
```

MOVHPS instruction for XMM to memory move:

```
DEST ← SRC[127:64];
```

**Intel C/C++ Compiler Intrinsic Equivalent**

```
MOVHPS _m128d_mm_loadh_pi (_m128d a, _m64 *p)
MOVHPS void _mm_storeh_pi (_m64 *p, _m128d a)
```

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
MOVHPS—Move High Packed Single-Precision Floating-Point Values

### INSTRUCTION SET REFERENCE, A-M

- **#SS(0)**: For an illegal address in the SS segment.
- **#PF(fault-code)**: For a page fault.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

### Real-Address Mode Exceptions

- **GP**: If any part of the operand lies outside the effective address space from 0 to FFFFH.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.

### Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

- **#PF(fault-code)**: For a page fault.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made.

### Compatibility Mode Exceptions

Same exceptions as in protected mode.

### 64-Bit Mode Exceptions

- **#SS(0)**: If a memory address referencing the SS segment is in a non-canonical form.
- **#GP(0)**: If the memory address is in a non-canonical form.
- **#PF(fault-code)**: For a page fault.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, A-M

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MOVLHPS—Move Packed Single-Precision Floating-Point Values Low to High

Description

Moves two packed single-precision floating-point values from the low quadword of the source operand (second operand) to the high quadword of the destination operand (first operand). The low quadword of the destination operand is left unchanged.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

DEST[127:64] ← SRC[63:0];
(* DEST[63:0] unchanged *)

Intel C/C++ Compiler Intrinsic Equivalent

MOVHLPS _m128 _mm_movelh_ps(_m128 a, _m128 b)

SIMD Floating-Point Exceptions

None.

Protected Mode Exceptions

#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Real Address Mode Exceptions

Same exceptions as in protected mode.

Virtual 8086 Mode Exceptions

Same exceptions as in protected mode.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
MOVLDP—Move Low Packed Double-Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 12</td>
<td>MOVLPD xmm, m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Move double-precision floating-point value from m64 to low quadword of xmm register.</td>
</tr>
<tr>
<td>66 0F 13</td>
<td>MOVLPD m64, xmm</td>
<td>Valid</td>
<td>Valid</td>
<td>Move double-precision floating-point value from low quadword of xmm register to m64.</td>
</tr>
</tbody>
</table>

**Description**

Moves a double-precision floating-point value from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be an XMM register or a 64-bit memory location. This instruction allows a double-precision floating-point value to be moved to and from the low quadword of an XMM register and memory. It cannot be used for register to register or memory to memory moves. When the destination operand is an XMM register, the high quadword of the register remains unchanged.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

MOVLDP instruction for memory to XMM move:

DEST[63:0] ← SRC;

(*) DEST[127:64] unchanged *)

MOVLDP instruction for XMM to memory move:

DEST ← SRC[63:0];

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVLDP _m128d _mm_loadl_pd ( _m128d a, double *p)
MOVLDP void _mm_storel_pd (double *p, _m128d a)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
INSTRUCTION SET REFERENCE, A-M

#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MOVLPS—Move Low Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 12 /r</td>
<td>MOVLPS xmm, m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Move two packed single-precision floating-point values from m64 to low quadword of xmm.</td>
</tr>
<tr>
<td>0F 13 /r</td>
<td>MOVLPS m64, xmm</td>
<td>Valid</td>
<td>Valid</td>
<td>Move two packed single-precision floating-point values from low quadword of xmm to m64.</td>
</tr>
</tbody>
</table>

**Description**

Moves two packed single-precision floating-point values from the source operand (second operand) and the destination operand (first operand). The source and destination operands can be an XMM register or a 64-bit memory location. This instruction allows two single-precision floating-point values to be moved to and from the low quadword of an XMM register and memory. It cannot be used for register to register or memory to memory moves. When the destination operand is an XMM register, the high quadword of the register remains unchanged.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

MOVLPS instruction for memory to XMM move:

```
DEST[63:0] ← SRC;
(* DEST[127:64] unchanged *)
```

MOVLPS instruction for XMM to memory move:

```
DEST ← SRC[63:0];
```

**Intel C/C++ Compiler Intrinsic Equivalent**

```
MOVLPS __m128 _mm_loadl_pi (__m128 a, __m64 *p)
MOVLPS void _mm_storel_pi (__m64 *p, __m128 a)
```

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
INSTRUCTION SET REFERENCE, A-M

#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MOVMSKPDP—Extract Packed Double-Precision Floating-Point Sign Mask

**Description**

Extracts the sign bits from the packed double-precision floating-point values in the source operand (second operand), formats them into a 2-bit mask, and stores the mask in the destination operand (first operand). The source operand is an XMM register, and the destination operand is a general-purpose register. The mask is stored in the 2 low-order bits of the destination operand. Zero-extend the upper bits of the destination.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. The default operand size is 64-bit in 64-bit mode.

**Operation**

\[
\begin{align*}
\text{DEST}[0] & \leftarrow \text{SRC}[63]; \\
\text{DEST}[1] & \leftarrow \text{SRC}[127]; \\
\text{IF} \ DEST = r32 \\
& \quad \text{THEN} \ DEST[31:2] \leftarrow \text{ZeroExtend}; \\
& \quad \text{ELSE} \ DEST[63:2] \leftarrow \text{ZeroExtend}; \\
\text{FI};
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVMSKPDP int _mm_movemask_pd (__m128d a)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- #NM If CR0.TS[bit 3] = 1.
- #UD If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.

**Opcode Instruction 64-Bit Mode**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 50 /r</td>
<td>MOVMSKPDP reg, xmm</td>
<td>Valid</td>
<td>Valid</td>
<td>Extract 2-bit sign mask from xmm and store in reg. The upper bits of r32 or r64 are filled with zeros.</td>
</tr>
</tbody>
</table>
MOVMSKPD—Extract Packed Double-Precision Floating-Point Sign Mask

If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

**Real-Address Mode Exceptions**
Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**
Same exceptions as in protected mode.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
Same exceptions as in protected mode.
MOVMSKPS—Extract Packed Single-Precision Floating-Point Sign Mask

Description
Extracts the sign bits from the packed single-precision floating-point values in the source operand (second operand), formats them into a 4-bit mask, and stores the mask in the destination operand (first operand). The source operand is an XMM register, and the destination operand is a general-purpose register. The mask is stored in the 4 low-order bits of the destination operand. Zero-extend the upper bits of the destination operand.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. The default operand size is 64-bit in 64-bit mode.

Operation
\[
\begin{align*}
\text{DEST}[0] & \leftarrow \text{SRC}[31]; \\
\text{DEST}[1] & \leftarrow \text{SRC}[63]; \\
\text{DEST}[2] & \leftarrow \text{SRC}[95]; \\
\text{DEST}[3] & \leftarrow \text{SRC}[127]; \\
\text{IF } \text{DEST} = r32 & \text{ THEN } \text{DEST}[31:4] \leftarrow \text{ZeroExtend}; \\
& \text{ ELSE } \text{DEST}[63:4] \leftarrow \text{ZeroExtend};
\end{align*}
\]

Intel C/C++ Compiler Intrinsic Equivalent
\[
\text{int } \_\text{mm} \_\text{movemask} \_\text{ps}(\_\text{m}128 \text{ a})
\]

SIMD Floating-Point Exceptions
None.

Protected Mode Exceptions
- #NM If CR0.TS[bit 3] = 1.
- #UD If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual 8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
MOVNTDQA — Load Double Quadword Non-Temporal Aligned Hint

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 2A /r</td>
<td>MOVNTDQA xmm1, m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Move double quadword from m128 to xmm using non-temporal hint if WC memory type.</td>
</tr>
</tbody>
</table>

Description

MOVNTDQA loads a double quadword from the source operand (second operand) to the destination operand (first operand) using a non-temporal hint. A processor implementation may make use of the non-temporal hint associated with this instruction if the memory source is WC (write combining) memory type. An implementation may also make use of the non-temporal hint associated with this instruction if the memory source is WB (write back) memory type.

A processor’s implementation of the non-temporal hint does not override the effective memory type semantics, but the implementation of the hint is processor dependent. For example, a processor implementation may choose to ignore the hint and process the instruction as a normal MOVDQA for any memory type. Another implementation of the hint for WC memory type may optimize data transfer throughput of WC reads. A third implementation may optimize cache reads generated by MOVNTDQA on WB memory type to reduce cache evictions.

WC Streaming Load Hint

For WC memory type in particular, the processor never appears to read the data into the cache hierarchy. Instead, the non-temporal hint may be implemented by loading a temporary internal buffer with the equivalent of an aligned cache line without filling this data to the cache. Any memory-type aliased lines in the cache will be snooped and flushed. Subsequent MOVNTDQA reads to unread portions of the WC cache line will receive data from the temporary internal buffer if data is available. The temporary internal buffer may be flushed by the processor at any time for any reason, for example:

- A load operation other than a MOVNTDQA which references memory already resident in a temporary internal buffer.
- A non-WC reference to memory already resident in a temporary internal buffer.
- Interleaving of reads and writes to memory currently residing in a single temporary internal buffer.
- Repeated MOVNTDQA loads of a particular 16-byte item in a streaming line.
- Certain micro-architectural conditions including resource shortages, detection of a mis-speculation condition, and various fault conditions

The memory type of the region being read can override the non-temporal hint, if the memory address specified for the non-temporal read is not a WC memory region.
Information on non-temporal reads and writes can be found in Chapter 11, "Memory Cache Control" of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*.

Because the WC protocol uses a weakly-ordered memory consistency model, an MFENCE or locked instruction should be used in conjunction with MOVNTDQA instructions if multiple processors might reference the same WC memory locations or in order to synchronize reads of a processor with writes by other agents in the system. Because of the speculative nature of fetching due to MOVNTDQA, Streaming loads must not be used to reference memory addresses that are mapped to I/O devices having side effects or when reads to these devices are destructive. For additional information on MOVNTDQA usages, see Section 12.10.3 in Chapter 12, "Programming with SSE3, SSSE3 and SSE4" of *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*.

**Operation**

DST ← SRC;

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVNTDQA __m128i _mm_stream_load_si128 (__m128i *p);

**Flags Affected**

None

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
  - If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
- **#SS(0)** For an illegal address in the SS segment.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
  - If LOCK prefix is used.
  - Either the prefix REP (F3h) or REPN (F2H) is used.

**Real Mode Exceptions**

- **#GP(0)** if any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

**#NM** If CR0.TS[bit 3] = 1.

**#UD** If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
   If LOCK prefix is used.
   Either the prefix REP (F3h) or REPN (F2H) is used.

**Virtual 8086 Mode Exceptions**
Same exceptions as in Real Address Mode.

**#PF(fault-code)** For a page fault.

**Compatibility Mode Exceptions**
Same exceptions as in Protected Mode.

**64-Bit Mode Exceptions**

**#GP(0)** If the memory address is in a non-canonical form.
   If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

**#SS(0)** If a memory address referencing the SS segment is in a non-canonical form.

**#PF(fault-code)** For a page fault.

**#NM** If TS in CR0 is set.

**#UD** If EM in CR0 is set.
   If OSFXSR in CR4 is 0.
   If CPUID feature flag ECX.SSE4_1 is 0.
   If LOCK prefix is used.
   Either the prefix REP (F3h) or REPN (F2H) is used.
MOVNTDQ—Store Double Quadword Using Non-Temporal Hint

**Description**

Moves the double quadword in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to prevent caching of the data during the write to memory. The source operand is an XMM register, which is assumed to contain integer data (packed bytes, words, doublewords, or quadwords). The destination operand is a 128-bit memory location.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTDQ instructions if multiple processors might use different memory types to read/write the destination memory locations.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST ← SRC;

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVNTDQ void _mm_stream_pd( double* p, __m128d a)

**SIMD Floating-Point Exceptions**

None.
Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real-address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
MOVNTDQ—Store Double Quadword Using Non-Temporal Hint

#UD

If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
MOVNTI—Store Doubleword Using Non-Temporal Hint

**Description**

Moves the doubleword integer in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to minimize cache pollution during the write to memory. The source operand is a general-purpose register. The destination operand is a 32-bit memory location.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTI instructions if multiple processors might use different memory types to read/write the destination memory locations.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[ \text{DEST} \leftarrow \text{SRC}; \]

**Intel C/C++ Compiler Intrinsic Equivalent**

`MOVNTI void _mm_stream_si32 (int *p, int a)`

**SIMD Floating-Point Exceptions**

None.
MOVNTI—Store Doubleword Using Non-Temporal Hint

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#UD If CPUID.01H:EDX.SSE2[bit 26] = 0.
          If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
          If any part of the operand lies outside the effective address space from 0 to FFFFH.
#UD If CPUID.01H:EDX.SSE2[bit 26] = 0.
          If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#UD If CPUID.01H:EDX.SSE2[bit 26] = 0.
          If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MOVNTPD—Store Packed Double-Precision Floating-Point Values Using Non-Temporal Hint

Description

Moves the double quadword in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to minimize cache pollution during the write to memory. The source operand is an XMM register, which is assumed to contain two packed double-precision floating-point values. The destination operand is a 128-bit memory location.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see "Caching of Temporal vs. Non-Temporal Data" in Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTPD instructions if multiple processors might use different memory types to read/write the destination memory locations.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

DEST ← SRC;

Intel C/C++ Compiler Intrinsic Equivalent

MOVNTPD  void _mm_stream_pd(double *p, __m128d a)

SIMD Floating-Point Exceptions

None.
Protected Mode Exceptions

#GP(0)  For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

   If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0)  For an illegal address in the SS segment.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.

#UD  If CR0.EM[bit 2] = 1.
       If CR4.OSFXSR[bit 9] = 0.
       If CPUID.01H:EDX.SSE2[bit 26] = 0.
       If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP  If a memory operand is not aligned on a 16-byte boundary, regardless of segment.

   If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM  If CR0.TS[bit 3] = 1.

#UD  If CR0.EM[bit 2] = 1.
       If CR4.OSFXSR[bit 9] = 0.
       If CPUID.01H:EDX.SSE2[bit 26] = 0.
       If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code)  For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.

   If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.
#UD

- If CR0.EM[bit 2] = 1.
- If CR4.OSFXSR[bit 9] = 0.
- If CPUID.01H:EDX.SSE2[bit 26] = 0.
- If the LOCK prefix is used.
MOVNTPS—Store Packed Single-Precision Floating-Point Values Using Non-Temporal Hint

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 2B /r</td>
<td>MOVNTPS m128, xmm</td>
<td>Valid</td>
<td>Valid</td>
<td>Move packed single-precision floating-point values from xmm to m128 using non-temporal hint.</td>
</tr>
</tbody>
</table>

**Description**

Moves the double quadword in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to minimize cache pollution during the write to memory. The source operand is an XMM register, which is assumed to contain four packed single-precision floating-point values. The destination operand is a 128-bit memory location.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see "Caching of Temporal vs. Non-Temporal Data" in Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTPS instructions if multiple processors might use different memory types to read/write the destination memory locations.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST ← SRC;

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVNTDQ void_mm_stream_ps(float * p, __m128 a)

**SIMD Floating-Point Exceptions**

None.
Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS,
ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary,
regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary,
regardless of segment.
If any part of the operand lies outside the effective address
space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-
canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary,
regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
MOVNTPS—Store Packed Single-Precision Floating-Point Values Using Non-Temporal Hint

#UD
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
MOVNTQ—Store of Quadword Using Non-Temporal Hint

Description

Moves the quadword in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to minimize cache pollution during the write to memory. The source operand is an MMX technology register, which is assumed to contain packed integer data (packed bytes, words, or doublewords). The destination operand is a 64-bit memory location.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTQ instructions if multiple processors might use different memory types to read/write the destination memory locations.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

\[
\text{DEST} \leftarrow \text{SRC};
\]

Intel C/C++ Compiler Intrinsic Equivalent

MOVNTQ void _mm_stream_pi(__m64 * p, __m64 a)

SIMD Floating-Point Exceptions

None.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
MOVNTQ—Store of Quadword Using Non-Temporal Hint

INSTRUCTION SET REFERENCE, A-M

#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If CR0.EM[bit 2] = 1.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory
reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 16-byte boundary,
regardless of segment.
If any part of the operand lies outside the effective address
space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If CR0.EM[bit 2] = 1.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory
reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-
canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If CR0.EM[bit 2] = 1.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MOVQ—Move Quadword

Description
Copies a quadword from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be MMX technology registers, XMM registers, or 64-bit memory locations. This instruction can be used to move a quadword between two MMX technology registers or between an MMX technology register and a 64-bit memory location, or to move data between two XMM registers or between an XMM register and a 64-bit memory location. The instruction cannot be used to transfer data between memory locations.

When the source operand is an XMM register, the low quadword is moved; when the destination operand is an XMM register, the quadword is stored to the low quadword of the register, and the high quadword is cleared to all 0s.

In 64-bit mode, use of the REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

Operation
MOVQ instruction when operating on MMX technology registers and memory locations:
   DEST ← SRC;

MOVQ instruction when source and destination operands are XMM registers:
   DEST[63:0] ← SRC[63:0];
   DEST[127:64] ← 0000000000000000H;

MOVQ instruction when source operand is XMM register and destination operand is memory location:
   DEST ← SRC[63:0];
MOVQ—Move Quadword

MOVQ instruction when source operand is memory location and destination
operand is XMM register:

\[
\begin{align*}
\text{DEST}[63:0] & \leftarrow \text{SRC}; \\
\text{DEST}[127:64] & \leftarrow 0000000000000000H;
\end{align*}
\]

**Flags Affected**

None.

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVQ m128i _mm_mov_epi64(__m128i a)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- **#GP(0)** If the destination operand is in a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#UD** If CR0.EM[bit 2] = 1.

128-bit operations will generate #UD only if CR4.OSFXSR[bit 9] = 0. Execution of 128-bit instructions on a non-SSE2 capable processor (one that is MMX technology capable) will result in the instruction operating on the mm registers, not #UD.

If the LOCK prefix is used.

- **#NM** If CR0.TS[bit 3] = 1.
- **#MF** (MMX register operations only) If there is a pending FPU exception.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- **#GP** If any part of the operand lies outside of the effective address space from 0 to FFFFH.
- **#UD** If CR0.EM[bit 2] = 1.

128-bit operations will generate #UD only if CR4.OSFXSR[bit 9] = 0. Execution of 128-bit instructions on a non-SSE2 capable
processor (one that is MMX technology capable) will result in the instruction operating on the mm registers, not #UD.

If the LOCK prefix is used.

#NM If CR0.TS[bit 3] = 1.

#MF (MMX register operations only) If there is a pending FPU exception.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#UD If CR0.EM[bit 2] = 1.

(XMM register operations only) If CR4.OSFXSR[bit 9] = 0.

(XMM register operations only) If CPUID.01H:EDX.SSE2[bit 26] = 0.

If the LOCK prefix is used.

#NM If CR0.TS[bit 3] = 1.

#MF (MMX register operations only) If there is a pending FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MOVQ2DQ—Move Quadword from MMX Technology to XMM Register

**Description**

Moves the quadword from the source operand (second operand) to the low quadword of the destination operand (first operand). The source operand is an MMX technology register and the destination operand is an XMM register.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the MOVQ2DQ instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[ \text{DEST}[63:0] \leftarrow \text{SRC}[63:0]; \]
\[ \text{DEST}[127:64] \leftarrow 0000000000000000000H; \]

**Intel C/C++ Compiler Intrinsic Equivalent**

`MOVQ2DQ __128i _mm_movpi64_pi64 (__m64 a)`

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
  - If the LOCK prefix is used.
- **#MF** If there is a pending x87 FPU exception.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.
Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**MOVNS/MOVSB/MOVSW/MOVSD/MOVSQ—Move Data from String to String**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A4</td>
<td>MOVS m8, m8</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Move byte from address DS:(E)SI to ES:(E)DI. For 64-bit mode move byte from address (R</td>
</tr>
<tr>
<td>A5</td>
<td>MOVS m16, m16</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, move word from address DS:(E)SI to ES:(E)DI. For 64-bit mode move word at address (R</td>
</tr>
<tr>
<td>A5</td>
<td>MOVS m32, m32</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, move dword from address DS:(E)SI to ES:(E)DI. For 64-bit mode move dword from address (R</td>
</tr>
<tr>
<td>REX.w + A5</td>
<td>MOVS m64, m64</td>
<td>Valid N.E.</td>
<td>Move qword from address (R</td>
<td>E)SI to (R</td>
</tr>
<tr>
<td>A4</td>
<td>MOVSB</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Move byte from address DS:(E)SI to ES:(E)DI. For 64-bit mode move byte from address (R</td>
</tr>
<tr>
<td>A5</td>
<td>MOVSW</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, move word from address DS:(E)SI to ES:(E)DI. For 64-bit mode move word at address (R</td>
</tr>
<tr>
<td>A5</td>
<td>MOVSD</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, move dword from address DS:(E)SI to ES:(E)DI. For 64-bit mode move dword from address (R</td>
</tr>
<tr>
<td>REX.w + A5</td>
<td>MOVSQ</td>
<td>Valid N.E.</td>
<td>Move qword from address (R</td>
<td>E)SI to (R</td>
</tr>
</tbody>
</table>

**Description**

Moves the byte, word, or doubleword specified with the second operand (source operand) to the location specified with the first operand (destination operand). Both the source and destination operands are located in memory. The address of the source operand is read from the DS:ESI or the DS:SI registers (depending on the address-size attribute of the instruction, 32 or 16, respectively). The address of the destination operand is read from the ES:EDI or the ES:DI registers (again depending on the address-size attribute of the instruction). The DS segment may be overridden with a segment override prefix, but the ES segment cannot be overridden.
At the assembly-code level, two forms of this instruction are allowed: the “explicit-operands” form and the “no-operands” form. The explicit-operands form (specified with the MOVS mnemonic) allows the source and destination operands to be specified explicitly. Here, the source and destination operands should be symbols that indicate the size and location of the source value and the destination, respectively. This explicit-operands form is provided to allow documentation; however, note that the documentation provided by this form can be misleading. That is, the source and destination operand symbols must specify the correct type (size) of the operands (bytes, words, or doublewords), but they do not have to specify the correct location. The locations of the source and destination operands are always specified by the DS:(E)SI and ES:(E)DI registers, which must be loaded correctly before the move string instruction is executed.

The no-operands form provides "short forms" of the byte, word, and doubleword versions of the MOVS instructions. Here also DS:(E)SI and ES:(E)DI are assumed to be the source and destination operands, respectively. The size of the source and destination operands is selected with the mnemonic: MOVSB (byte move), MOVSW (word move), or MOVSD (doubleword move).

After the move operation, the (E)SI and (E)DI registers are incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the (E)SI and (E)DI register are incremented; if the DF flag is 1, the (E)SI and (E)DI registers are decremented.) The registers are incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The MOVS, MOVSB, MOVSW, and MOVSD instructions can be preceded by the REP prefix (see "RDTSCP—Read Time-Stamp Counter and Processor ID” in Chapter 4, Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B) for block moves of ECX bytes, words, or doublewords.

In 64-bit mode, the instruction's default address size is 64 bits; 32-bit address size is supported using the prefix 67H. The 64-bit addresses are specified by RSI and RDI; 32-bit address are specified by ESI and EDI. Use of the REX.W prefix promotes doubleword operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\text{DEST} \leftarrow \text{SRC};
\]

Non-64-bit Mode:

IF (Byte move)

\[
\text{THEN IF } \text{DF} = 0
\]

\[
\text{THEN}
\]

\[
\text{(E)SI} \leftarrow (\text{E})\text{SI} + 1;
\]

\[
\text{(E)DI} \leftarrow (\text{E})\text{DI} + 1;
\]

ELSE

\[
\text{MOVXS/MOVX/EXPAND—Move Words from String }
\]

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(E)SI ← (E)SI – 1;
(E)DI ← (E)DI – 1;
FI;
ELSE IF (Word move)
    THEN IF DF = 0
        (E)SI ← (E)SI + 2;
        (E)DI ← (E)DI + 2;
    FI;
    ELSE
        (E)SI ← (E)SI – 2;
        (E)DI ← (E)DI – 2;
    FI;
ELSE IF (Doubleword move)
    THEN IF DF = 0
        (E)SI ← (E)SI + 4;
        (E)DI ← (E)DI + 4;
    FI;
    ELSE
        (E)SI ← (E)SI – 4;
        (E)DI ← (E)DI – 4;
    FI;
FI;
64-bit Mode:
IF (Byte move)
    THEN IF DF = 0
        THEN
            (R|E)SI ← (R|E)SI + 1;
            (R|E)DI ← (R|E)DI + 1;
        ELSE
            (R|E)SI ← (R|E)SI – 1;
            (R|E)DI ← (R|E)DI – 1;
        FI;
ELSE IF (Word move)
    THEN IF DF = 0
        THEN
            (R|E)SI ← (R|E)SI + 2;
            (R|E)DI ← (R|E)DI + 2;
        FI;
    ELSE
        (R|E)SI ← (R|E)SI – 2;
        (R|E)DI ← (R|E)DI – 2;
    FI;
ELSE IF (Doubleword move)
    THEN IF DF = 0

MOVS/MOVSB/MOVSW/MOVSD/MOVSQ—Move Data from String to String
MOVS/MOVSB/MOVSW/MOVSD/MOVSDQ—Move Data from String to String

(R|E)SI ← (R|E)SI + 4;
(R|E)DI ← (R|E)DI + 4;
FI;
ELSE
(R|E)SI ← (R|E)SI – 4;
(R|E)DI ← (R|E)DI – 4;
FI;
ELSE IF (Quadword move)
THEN IF DF = 0
(R|E)SI ← (R|E)SI + 8;
(R|E)DI ← (R|E)DI + 8;
FI;
ELSE
(R|E)SI ← (R|E)SI – 8;
(R|E)DI ← (R|E)DI – 8;
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
MOVSD—Move Scalar Double-Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 10 /r</td>
<td>MOVSD xmm1, xmm2/m64</td>
<td>Valid</td>
<td>Valid</td>
<td>Move scalar double-precision floating-point value from xmm2/m64 to xmm1 register.</td>
</tr>
<tr>
<td>F2 0F 11 /r</td>
<td>MOVSD xmm2/m64, xmm1</td>
<td>Valid</td>
<td>Valid</td>
<td>Move scalar double-precision floating-point value from xmm1 register to xmm2/m64.</td>
</tr>
</tbody>
</table>

**Description**

Moves a scalar double-precision floating-point value from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be XMM registers or 64-bit memory locations. This instruction can be used to move a double-precision floating-point value to and from the low quadword of an XMM register and a 64-bit memory location, or to move a double-precision floating-point value between the low quadwords of two XMM registers. The instruction cannot be used to transfer data between memory locations.

When the source and destination operands are XMM registers, the high quadword of the destination operand remains unchanged. When the source operand is a memory location and destination operand is an XMM registers, the high quadword of the destination operand is cleared to all 0s.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

MOVSD instruction when source and destination operands are XMM registers:

`DEST[63:0] ← SRC[63:0];`

(`* DEST[127:64] unchanged *`)

MOVSD instruction when source operand is XMM register and destination operand is memory location:

`DEST ← SRC[63:0];`

MOVSD instruction when source operand is memory location and destination operand is XMM register:

`DEST[63:0] ← SRC;`

`DEST[127:64] ← 0000000000000000H;`

**Intel C/C++ Compiler Intrinsic Equivalent**

`MOVSD __m128d _mm_load_sd (double *p)`
MOVSD  void _mm_store_sd (double *p, __m128d a)
MOVSD __m128d _mm_store_sd (__m128d a, __m128d b)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- **#SS(0)** For an illegal address in the SS segment.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If CR4.OSFXSR[bit 9] = 0.
- If CPUID.01H:EDX.SSE2[bit 26] = 0.
- If the LOCK prefix is used.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- **GP** If any part of the operand lies outside the effective address space from 0 to FFFFH.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If CR4.OSFXSR[bit 9] = 0.
- If CPUID.01H:EDX.SSE2[bit 26] = 0.
- If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

Same exceptions as in real address mode.

- **#PF(fault-code)** For a page fault.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE2[bit 26] = 0.
   If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MOVSHDUP—Move Packed Single-FP High and Duplicate

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 16 /r</td>
<td>MOVSHDUP xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Move two single-precision floating-point values from the higher 32-bit operand of each qword in xmm2/m128 to xmm1 and duplicate each 32-bit operand to the lower 32-bits of each qword.</td>
</tr>
</tbody>
</table>

**Description**

The linear address corresponds to the address of the least-significant byte of the referenced memory data. When a memory address is indicated, the 16 bytes of data at memory location m128 are loaded and the single-precision elements in positions 1 and 3 are duplicated. When the register-register form of this operation is used, the same operation is performed but with data coming from the 128-bit source register. See Figure 3-16.

![Figure 3-16. MOVSHDUP—Move Packed Single-FP High and Duplicate](image)

In 64-bit mode, use of the REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).
Operation

IF (Source == m128)
    THEN (* Load instruction *)
        xmm1[31:0] = m128[63:32];
        xmm1[63:32] = m128[63:32];
        xmm1[95:64] = m128[127:96];
        xmm1[127:96] = m128[127:96];
    ELSE (* Move instruction *)
        xmm1[31:0] = xmm2[63:32];
        xmm1[63:32] = xmm2[63:32];
        xmm1[95:64] = xmm2[127:96];
        xmm1[127:96] = xmm2[127:96];
FI;

Intel C/C++ Compiler Intrinsic Equivalent

MOVSHDUP __m128 _mm_movehdup_ps(__m128 a)

Exceptions

General protection exception if not aligned on 16-byte boundary, regardless of segment.

Numeric Exceptions

None

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.
#UD
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
**Real Address Mode Exceptions**

GP(0)  If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM  If CR0.TS[bit 3] = 1.
#UD  If CR0.EM[bit 2] = 1.
      If CR4.OSFXSR[bit 9] = 0.
      If CPUID.01H:ECX.SSE3[bit 0] = 0.
      If the LOCK prefix is used.

**Virtual 8086 Mode Exceptions**

GP(0)  If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM  If CR0.TS[bit 3] = 1.
#UD  If CR0.EM[bit 2] = 1.
      If CR4.OSFXSR[bit 9] = 0.
      If CPUID.01H:ECX.SSE3[bit 0] = 0.
      If the LOCK prefix is used.

#PF(fault-code)  For a page fault.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0)  If a memory address referencing the SS segment is not non-canonical.

#GP(0)  If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.
#UD  If CR0.EM[bit 2] = 1.
      If CR4.OSFXSR[bit 9] = 0.
      If CPUID.SSE3(ECX, bit 0) is 0.
      If the LOCK prefix is used.
MOVSLDUP—Move Packed Single-FP Low and Duplicate

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 12 /r</td>
<td>MOVSLDUP xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Move two single-precision floating-point values from the lower 32-bit operand of each qword in xmm2/m128 to xmm1 and duplicate each 32-bit operand to the higher 32-bits of each qword.</td>
</tr>
</tbody>
</table>

**Description**

The linear address corresponds to the address of the least-significant byte of the referenced memory data. When a memory address is indicated, the 16 bytes of data at memory location m128 are loaded and the single-precision elements in positions 0 and 2 are duplicated. When the register-register form of this operation is used, the same operation is performed but with data coming from the 128-bit source register. See Figure 3-17.

![Figure 3-17. MOVSLDUP—Move Packed Single-FP Low and Duplicate](image)

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
Operation

IF (Source == m128)
THEN (* Load instruction *)
  xmm1[31:0] = m128[31:0];
  xmm1[63:32] = m128[31:0];
  xmm1[95:64] = m128[95:64];
  xmm1[127:96] = m128[95:64];
ELSE (* Move instruction *)
  xmm1[31:0] = xmm2[31:0];
  xmm1[63:32] = xmm2[31:0];
  xmm1[95:64] = xmm2[95:64];
  xmm1[127:96] = xmm2[95:64];
FI;

Intel C/C++ Compiler Intrinsic Equivalent

MOVSLDUP __m128 _mm_moveldup_ps(__m128 a)

Exceptions

General protection exception if not aligned on 16-byte boundary, regardless of segment.

Numeric Exceptions

None.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
Real Address Mode Exceptions

GP(0)  If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM  If CR0.TS[bit 3] = 1.
#UD  If CR0.EM[bit 2] = 1.

Virtual 8086 Mode Exceptions

GP(0)  If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#NM  If CR0.TS[bit 3] = 1.
#UD  If CR0.EM[bit 2] = 1.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.
If memory operand is not aligned on a 16-byte boundary, regardless of segment.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.
#UD  If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.  
If CPUID.01H:ECX.SSE3[bit 0] = 0.
If the LOCK prefix is used.
MOVSS—Move Scalar Single-Precision Floating-Point Values

**Description**

Moves a scalar single-precision floating-point value from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be XMM registers or 32-bit memory locations. This instruction can be used to move a single-precision floating-point value to and from the low doubleword of an XMM register and a 32-bit memory location, or to move a single-precision floating-point value between the low doublewords of two XMM registers. The instruction cannot be used to transfer data between memory locations.

When the source and destination operands are XMM registers, the three high-order doublewords of the destination operand remain unchanged. When the source operand is a memory location and destination operand is an XMM register, the three high-order doublewords of the destination operand are cleared to all 0s.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

MOVSS instruction when source and destination operands are XMM registers:

```
DEST[31:0] ← SRC[31:0];
(* DEST[127:32] remains unchanged *)
```

MOVSS instruction when source operand is XMM register and destination operand is memory location:

```
DEST ← SRC[31:0];
```

MOVSS instruction when source operand is memory location and destination operand is XMM register:

```
DEST[31:0] ← SRC;
DEST[127:32] ← 00000000000000000000000000000000H;
```

**Intel C/C++ Compiler Intrinsic Equivalent**

`MOVSS __m128 _mm_load_ss(float * p)`
MOVSS  void _mm_store_ss(float * p, __m128 a)
MOVSS  __m128 _mm_move_ss(__m128 a, __m128 b)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- **#SS(0)** For an illegal address in the SS segment.
- **#PF(fault-code)** For a page fault.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- **GP** If any part of the operand lies outside the effective address space from 0 to FFFFH.
- **#NM** If CR0.TS[bit 3] = 1.
- **#UD** If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE[bit 25] = 0.
  - If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

Same exceptions as in real address mode.

- **#PF(fault-code)** For a page fault.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.

#PF(fault-code)  For a page fault.

#NM  If CR0.TS[bit 3] = 1.

#UD  If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
**MOVSX/MOVSXD—Move with Sign-Extension**

### Description
Copies the contents of the source operand (register or memory location) to the destination operand (register) and sign extends the value to 16 or 32 bits (see Figure 7-6 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). The size of the converted value depends on the operand-size attribute.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

### Operation

\[ \text{DEST} \leftarrow \text{SignExtend} (\text{SRC}) ; \]

### Flags Affected

None.

---

### Opcode Table

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F BE /r</td>
<td>MOV r16, r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Move byte to word with sign-extension.</td>
</tr>
<tr>
<td>0F BE /r</td>
<td>MOV r32, r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Move byte to doubleword with sign-extension.</td>
</tr>
<tr>
<td>REX + 0F BE /r</td>
<td>MOV r64, r/m8*</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move byte to quadword with sign-extension.</td>
</tr>
<tr>
<td>0F BF /r</td>
<td>MOV r32, r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Move word to doubleword, with sign-extension.</td>
</tr>
<tr>
<td>REX.W + 0F BF /r</td>
<td>MOV r64, r/m16</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move word to quadword with sign-extension.</td>
</tr>
<tr>
<td>REX.W** + 63 /r</td>
<td>MOV r64, r/m32</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move doubleword to quadword with sign-extension.</td>
</tr>
</tbody>
</table>

### Notes:

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

** The use of MOVSXD without REX.W in 64-bit mode is discouraged, Regular MOV should be used instead of using MOVSXD without REX.W.
Protected Mode Exceptions

- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If the LOCK prefix is used.

Real-Address Mode Exceptions

- **#GP**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS**: If a memory operand effective address is outside the SS segment limit.
- **#UD**: If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)**: If a page fault occurs.
- **#UD**: If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

- **#SS(0)**: If a memory address referencing the SS segment is in a non-canonical form.
- **#GP(0)**: If the memory address is in a non-canonical form.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If the LOCK prefix is used.
MOVUPD—Move Unaligned Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 10 /r</td>
<td>MOVUPD xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Move packed double-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>66 0F 11 /r</td>
<td>MOVUPD xmm2/m128, xmm</td>
<td>Valid</td>
<td>Valid</td>
<td>Move packed double-precision floating-point values from xmm1 to xmm2/m128.</td>
</tr>
</tbody>
</table>

**Description**

Moves a double quadword containing two packed double-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, store the contents of an XMM register into a 128-bit memory location, or move data between two XMM registers. When the source or destination operand is a memory operand, the operand may be unaligned on a 16-byte boundary without causing a general-protection exception (#GP) to be generated.

To move double-precision floating-point values to and from memory locations that are known to be aligned on 16-byte boundaries, use the MOVAPD instruction.

While executing in 16-bit addressing mode, a linear address for a 128-bit data access that overlaps the end of a 16-bit segment is not allowed and is defined as reserved behavior. A specific processor implementation may or may not generate a general-protection exception (#GP) in this situation, and the address that spans the end of the segment may or may not wrap around to the beginning of the segment.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST ← SRC;

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVUPD __m128 _mm_loadu_pd(double * p)
MOVUPD void _mm_storeu_pd(double *p, __m128 a)

**SIMD Floating-Point Exceptions**

None.
Protected Mode Exceptions

- #AC(0) If alignment checking is enabled and an unaligned memory reference is made.
- #GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- #SS(0) For an illegal address in the SS segment.
- #PF(fault-code) For a page fault.
- #NM If CR0.TS[bit 3] = 1.
- #UD If CR0.EM[bit 2] = 1.
- If CR4.OSFXSR[bit 9] = 0.
- If CPUID.01H:EDX:SSE2[bit 26] = 0.
- If the LOCK prefix is used.

Real-Address Mode Exceptions

- GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
- #NM If CR0.TS[bit 3] = 1.
- #UD If CR0.EM[bit 2] = 1.
- If CR4.OSFXSR[bit 9] = 0.
- If CPUID.01H:EDX:SSE2[bit 26] = 0.
- If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

- #AC(0) If alignment checking is enabled and an unaligned memory reference is made.
- #PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

- #AC(0) If alignment checking is enabled and an unaligned memory reference is made.
- #SS(0) If a memory address referencing the SS segment is in a non-canonical form.
- #GP(0) If the memory address is in a non-canonical form.
- #PF(fault-code) For a page fault.
- #NM If CR0.TS[bit 3] = 1.
MOVUPD—Move Unaligned Packed Double-Precision Floating-Point Values

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#UD

If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
MOVUPS—Move Unaligned Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/LEG Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 10 1r</td>
<td>MOVUPS xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Move packed single-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>0F 11 1r</td>
<td>MOVUPS xmm2/m128, xmm1</td>
<td>Valid</td>
<td>Valid</td>
<td>Move packed single-precision floating-point values from xmm1 to xmm2/m128.</td>
</tr>
</tbody>
</table>

**Description**

Moves a double quadword containing four packed single-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, store the contents of an XMM register into a 128-bit memory location, or move data between two XMM registers. When the source or destination operand is a memory operand, the operand may be unaligned on a 16-byte boundary without causing a general-protection exception (#GP) to be generated.

To move packed single-precision floating-point values to and from memory locations that are known to be aligned on 16-byte boundaries, use the MOVAPS instruction.

While executing in 16-bit addressing mode, a linear address for a 128-bit data access that overlaps the end of a 16-bit segment is not allowed and is defined as reserved behavior. A specific processor implementation may or may not generate a general-protection exception (#GP) in this situation, and the address that spans the end of the segment may or may not wrap around to the beginning of the segment.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST ← SRC;

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVUPS _m128_mm_loadu_ps(double * p)
MOVUPS void _mm_storeu_ps(double *p, __m128 a)

**SIMD Floating-Point Exceptions**

None.
Protected Mode Exceptions

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#GP(0) For an illegal memory operand effective address in the CS, DS,
      ES, FS or GS segments.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
      If CR4.OSFXSR[bit 9] = 0.
      If CPUID.01H:EDX.SSE[bit 25] = 0.
      If the LOCK prefix is used.

Real-Address Mode Exceptions

GP If any part of the operand lies outside the effective address space from 0 to FFFFH.

#NM If CR0.TS[bit 3] = 1.

#UD If CR0.EM[bit 2] = 1.
      If CR4.OSFXSR[bit 9] = 0.
      If CPUID.01H:EDX.SSE[bit 25] = 0.
      If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.
#UD       If CR0.EM[bit 2] = 1.
        If CR4.OSFXSR[bit 9] = 0.
        If CPUID.01H:EDX.SSE[bit 25] = 0.
        If the LOCK prefix is used.
MOVZX—Move with Zero-Extend

Description
Copies the contents of the source operand (register or memory location) to the destination operand (register) and zero extends the value. The size of the converted value depends on the operand-size attribute.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bit operands. See the summary chart at the beginning of this section for encoding data and limits.

Operation
DEST ← ZeroExtend(SRC);

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

NOTES:
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if the REX prefix is used: AH, BH, CH, DH.
INSTRUCTION SET REFERENCE, A-M

#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
MPSADBW — Compute Multiple Packed Sums of Absolute Difference

Description

MPSADBW sums the absolute difference (SAD) of a pair of unsigned bytes for a group of 4 byte pairs, and produces 8 SAD results (one for each 4 byte-pairs) stored as 8 word integers in the destination operand (first operand). Each 4 byte pairs are selected from the source operand (first operand) and the destination according to the bit fields specified in the immediate byte (third operand).

The immediate byte provides two bit fields:

SRC_OFFSET: the value of Imm8[1:0]*32 specifies the offset of the 4 sequential source bytes in the source operand.
DEST_OFFSET: the value of Imm8[2]*32 specifies the offset of the first of 8 groups of 4 sequential destination bytes in the destination operand. The next four destination bytes starts at DEST_OFFSET + 8, etc.

The SAD operation is repeated 8 times, each time using the same 4 source bytes but selecting the next group of 4 destination bytes starting at the next higher byte in the destination. Each 16-bit sum is written to destination.

Operation

SRC_OFFSET ← imm8[1:0]*32
DEST_OFFSET ← imm8[2]*32
DEST_BYTE0 ← DEST[DEST_OFFSET+7:DEST_OFFSET]
DEST_BYTE1 ← DEST[DEST_OFFSET+15:DEST_OFFSET+8]
DEST_BYTE2 ← DEST[DEST_OFFSET+23:DEST_OFFSET+16]
DEST_BYTE3 ← DEST[DEST_OFFSET+31:DEST_OFFSET+24]
DEST_BYTE4 ← DEST[DEST_OFFSET+39:DEST_OFFSET+32]
DEST_BYTE5 ← DEST[DEST_OFFSET+47:DEST_OFFSET+40]
DEST_BYTE6 ← DEST[DEST_OFFSET+55:DEST_OFFSET+48]
DEST_BYTE7 ← DEST[DEST_OFFSET+63:DEST_OFFSET+56]
DEST_BYTE8 ← DEST[DEST_OFFSET+71:DEST_OFFSET+64]
DEST_BYTE9 ← DEST[DEST_OFFSET+79:DEST_OFFSET+72]

Sums absolute 8-bit integer difference of adjacent groups of 4 byte integers in xmm1 and xmm2/m128 and writes the results in xmm1. Starting offsets within xmm1 and xmm2/m128 are determined by imm8.
DEST_BYTEN ← DEST[DEST_OFFSET+87:DEST_OFFSET+80]

SRC_BYTE0 ← SRC[SRC_OFFSET+7:SRC_OFFSET]
SRC_BYTE1 ← SRC[SRC_OFFSET+15:SRC_OFFSET+8]
SRC_BYTE2 ← SRC[SRC_OFFSET+23:SRC_OFFSET+16]
SRC_BYTE3 ← SRC[SRC_OFFSET+31:SRC_OFFSET+24]

TEMP0 ← ABS(DEST_BYTE0 - SRC_BYTE0)
TEMP1 ← ABS(DEST_BYTE1 - SRC_BYTE1)
TEMP2 ← ABS(DEST_BYTE2 - SRC_BYTE2)
TEMP3 ← ABS(DEST_BYTE3 - SRC_BYTE3)
DEST[15:0] ← TEMP0 + TEMP1 + TEMP2 + TEMP3

TEMP0 ← ABS(DEST_BYTE1 - SRC_BYTE0)
TEMP1 ← ABS(DEST_BYTE2 - SRC_BYTE1)
TEMP2 ← ABS(DEST_BYTE3 - SRC_BYTE2)
TEMP3 ← ABS(DEST_BYTE4 - SRC_BYTE3)
DEST[31:16] ← TEMP0 + TEMP1 + TEMP2 + TEMP3

TEMP0 ← ABS(DEST_BYTE2 - SRC_BYTE0)
TEMP1 ← ABS(DEST_BYTE3 - SRC_BYTE1)
TEMP2 ← ABS(DEST_BYTE4 - SRC_BYTE2)
TEMP3 ← ABS(DEST_BYTE5 - SRC_BYTE3)
DEST[47:32] ← TEMP0 + TEMP1 + TEMP2 + TEMP3

TEMP0 ← ABS(DEST_BYTE3 - SRC_BYTE0)
TEMP1 ← ABS(DEST_BYTE4 - SRC_BYTE1)
TEMP2 ← ABS(DEST_BYTE5 - SRC_BYTE2)
TEMP3 ← ABS(DEST_BYTE6 - SRC_BYTE3)
DEST[63:48] ← TEMP0 + TEMP1 + TEMP2 + TEMP3

TEMP0 ← ABS(DEST_BYTE4 - SRC_BYTE0)
TEMP1 ← ABS(DEST_BYTE5 - SRC_BYTE1)
TEMP2 ← ABS(DEST_BYTE6 - SRC_BYTE2)
TEMP3 ← ABS(DEST_BYTE7 - SRC_BYTE3)
DEST[79:64] ← TEMP0 + TEMP1 + TEMP2 + TEMP3

TEMP0 ← ABS(DEST_BYTE5 - SRC_BYTE0)
TEMP1 ← ABS(DEST_BYTE6 - SRC_BYTE1)
TEMP2 ← ABS(DEST_BYTE7 - SRC_BYTE2)
TEMP3 ← ABS(DEST_BYTE8 - SRC_BYTE3)
DEST[95:80] ← TEMP0 + TEMP1 + TEMP2 + TEMP3
MPSADBW — Compute Multiple Packed Sums of Absolute Difference

TEMPO ← \text{ABS}(\text{DEST}_{\text{BYTE}6} - \text{SRC}_{\text{BYTE}0})
TEMP1 ← \text{ABS}(\text{DEST}_{\text{BYTE}7} - \text{SRC}_{\text{BYTE}1})
TEMP2 ← \text{ABS}(\text{DEST}_{\text{BYTE}8} - \text{SRC}_{\text{BYTE}2})
TEMP3 ← \text{ABS}(\text{DEST}_{\text{BYTE}9} - \text{SRC}_{\text{BYTE}3})
\text{DEST}_{[111:96]} ← \text{TEMPO} + \text{TEMP1} + \text{TEMP2} + \text{TEMP3}

TEMPO ← \text{ABS}(\text{DEST}_{\text{BYTE}7} - \text{SRC}_{\text{BYTE}0})
TEMP1 ← \text{ABS}(\text{DEST}_{\text{BYTE}8} - \text{SRC}_{\text{BYTE}1})
TEMP2 ← \text{ABS}(\text{DEST}_{\text{BYTE}9} - \text{SRC}_{\text{BYTE}2})
TEMP3 ← \text{ABS}(\text{DEST}_{\text{BYTE}10} - \text{SRC}_{\text{BYTE}3})
\text{DEST}_{[127:112]} ← \text{TEMPO} + \text{TEMP1} + \text{TEMP2} + \text{TEMP3}

\textbf{Intel C/C++ Compiler Intrinsic Equivalent}

MPSADBW \_m128i \_mm_mpsadbw_epu8 (\_m128i s1, \_m128i s2, const int mask);

\textbf{Flags Affected}

None

\textbf{Protected Mode Exceptions}

\#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS, or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
\#SS(0) For an illegal address in the SS segment.
\#PF(fault-code) For a page fault.
\#NM If CR0.TS[bit 3] = 1.
\#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

\textbf{Real Mode Exceptions}

\#GP(0) if any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
\#NM If CR0.TS[bit 3] = 1.
\#UD If CR0.EM[bit 2] = 1.
INSTRUCTION SET REFERENCE, A-M

If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:ECX.SSE4_1[bit 19] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Virtual 8086 Mode Exceptions
Same exceptions as in Real Address Mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions
Same exceptions as in Protected Mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If TS in CR0 is set.
#UD If EM in CR0 is set.
If OSFXSR in CR4 is 0.
If CPUID feature flag ECX.SSE4_1 is 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.
MUL—Unsigned Multiply

### Opcode Table

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /4</td>
<td>MUL r/m8</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned multiply (AX ← AL * r/m8).</td>
</tr>
<tr>
<td>REX + F6 /4</td>
<td>MUL r/m8</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned multiply (AX ← AL * r/m8).</td>
</tr>
<tr>
<td>F7 /4</td>
<td>MUL r/m16</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned multiply (DX:AX ← AX * r/m16).</td>
</tr>
<tr>
<td>F7 /4</td>
<td>MUL r/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned multiply (EDX:EAX ← EAX * r/m32).</td>
</tr>
<tr>
<td>REX.W + F7 /4</td>
<td>MUL r/m64</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned multiply (RDX:RAX ← RAX * r/m64).</td>
</tr>
</tbody>
</table>

### Description

Performs an unsigned multiplication of the first operand (destination operand) and the second operand (source operand) and stores the result in the destination operand. The destination operand is an implied operand located in register AL, AX or EAX (depending on the size of the operand); the source operand is located in a general-purpose register or a memory location. The action of this instruction and the location of the result depends on the opcode and the operand size as shown in Table 3-69.

The result is stored in register AX, register pair DX:AX, or register pair EDX:EAX (depending on the operand size), with the high-order bits of the product contained in register AH, DX, or EDX, respectively. If the high-order bits of the product are 0, the CF and OF flags are cleared; otherwise, the flags are set.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits.

See the summary chart at the beginning of this section for encoding data and limits.

### Table 3-69. MUL Results

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Source 1</th>
<th>Source 2</th>
<th>Destination</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
<td>AL</td>
<td>r/m8</td>
<td>AX</td>
</tr>
<tr>
<td>Word</td>
<td>AX</td>
<td>r/m16</td>
<td>DX:AX</td>
</tr>
<tr>
<td>Doubleword</td>
<td>EAX</td>
<td>r/m32</td>
<td>EDX:EAX</td>
</tr>
<tr>
<td>Quadword</td>
<td>RAX</td>
<td>r/m64</td>
<td>RDX:RAX</td>
</tr>
</tbody>
</table>

NOTES:

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
Operation

IF (Byte operation)
    THEN
        AX ← AL * SRC;
    ELSE (* Word or doubleword operation *)
        IF OperandSize = 16
            THEN
                DX:AX ← AX * SRC;
            ELSE IF OperandSize = 32
                THEN EDX:EAX ← EAX * SRC; FI;
            ELSE (* OperandSize = 64 *)
                RDX:RAX ← RAX * SRC;
        FI;
    FI;

Flags Affected

The OF and CF flags are set to 0 if the upper half of the result is 0; otherwise, they are set to 1. The SF, ZF, AF, and PF flags are undefined.

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
MUL—Unsigned Multiply

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MULPD—Multiply Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 59 /r</td>
<td>MULPD xmm1, xmm2/m128</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply packed double-precision floating-point values in xmm2/m128 by xmm1.</td>
</tr>
</tbody>
</table>

Description
Performs a SIMD multiply of the two packed double-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the packed double-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Figure 11-3 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a SIMD double-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST[63:0] ← DEST[63:0] * SRC[63:0];
DEST[127:64] ← DEST[127:64] * SRC[127:64];

Intel C/C++ Compiler Intrinsic Equivalent
MULPD _mm128d _mm_mul_pd (m128d a, m128d b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
   If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE2[bit 26] = 0.
    If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP  If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
    If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM  If CR0.TS[bit 3] = 1.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
    If CR0.EM[bit 2] = 1.
    If CR4.OSFXSR[bit 9] = 0.
    If CPUID.01H:EDX.SSE2[bit 26] = 0.
    If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.
#PF(fault-code)  For a page fault.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
        If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code)  For a page fault.
#NM  If CR0.TS[bit 3] = 1.
#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD

If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.

If CR0.EM[bit 2] = 1.

If CR4.OSFXSR[bit 9] = 0.

If CPUID.01H:EDX.SSE2[bit 26] = 0.

If the LOCK prefix is used.
MULPS—Multiply Packed Single-Precision Floating-Point Values

Description
Performs a SIMD multiply of the four packed single-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the packed single-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Figure 10-5 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a SIMD single-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST[31:0] ← DEST[31:0] * SRC[31:0];
DEST[95:64] ← DEST[95:64] * SRC[95:64];

Intel C/C++ Compiler Intrinsic Equivalent
MULPS __m128 _mm_mul_ps(__m128 a, __m128 b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
INSTRUCTION SET REFERENCE, A-M

#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
   If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
   If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
MULPS—Multiply Packed Single-Precision Floating-Point Values

INSTRUCTION SET REFERENCE, A-M

#XM  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.

#UD  If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
   If CR0.EM[bit 2] = 1.
   If CR4.OSFXSR[bit 9] = 0.
   If CPUID.01H:EDX.SSE[bit 25] = 0.
   If the LOCK prefix is used.
MULSD—Multiply Scalar Double-Precision Floating-Point Values

Description
Multiplies the low double-precision floating-point value in the source operand (second operand) by the low double-precision floating-point value in the destination operand (first operand), and stores the double-precision floating-point result in the destination operand. The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. The high quadword of the destination operand remains unchanged. See Figure 11-4 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a scalar double-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation
DEST[63:0] ← DEST[63:0] * xmm2/m64[63:0];
(* DEST[127:64] unchanged *)

Intel C/C++ Compiler Intrinsic Equivalent
MULSD __m128d _mm_mul_sd (m128d a, m128d b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions
#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 1.
MULSD—Multiply Scalar Double-Precision Floating-Point Values

#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE2[bit 26] = 0.
  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.
#AC For unaligned memory reference.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD
If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

#AC(0)
If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MULSS—Multiply Scalar Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 59</td>
<td>MULSS xmm1, xmm2/m32</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply the low single-precision floating-point value in xmm2/mem by the low single-precision floating-point value in xmm1.</td>
</tr>
</tbody>
</table>

Description

Multiplies the low single-precision floating-point value from the source operand (second operand) by the low single-precision floating-point value in the destination operand (first operand), and stores the single-precision floating-point result in the destination operand. The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. The three high-order double-words of the destination operand remain unchanged. See Figure 10-6 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an illustration of a scalar single-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

DEST[31:0] ← DEST[31:0] * SRC[31:0];
(* DEST[127:32] unchanged *)

Intel C/C++ Compiler Intrinsic Equivalent

MULSS __m128 __mm_mul_ss(__m128 a, __m128 b)

SIMD Floating-Point Exceptions

Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE[bit 25] = 0.
  If the LOCK prefix is used.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
#UD If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 0.
  If CR0.EM[bit 2] = 1.
  If CR4.OSFXSR[bit 9] = 0.
  If CPUID.01H:EDX.SSE[bit 25] = 0.
  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.
#AC For unaligned memory reference.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
#XM If an unmasked SIMD floating-point exception and CR4.OSXM-MEXCPT[bit 10] = 1.
MULSS—Multiply Scalar Single-Precision Floating-Point Values

#UD
If an unmasked SIMD floating-point exception and CR4.OSXMEXCPT[bit 10] = 0.
If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE[bit 25] = 0.
If the LOCK prefix is used.

#AC(0)
If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MWAIT—Monitor Wait

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 C9</td>
<td>MWAIT</td>
<td>Valid</td>
<td>Valid</td>
<td>A hint that allow the processor to stop instruction execution and enter an implementation-dependent optimized state until occurrence of a class of events.</td>
</tr>
</tbody>
</table>

**Description**

MWAIT instruction provides hints to allow the processor to enter an implementation-dependent optimized state. There are two principal targeted usages: address-range monitor and advanced power management. Both usages of MWAIT require the use of the MONITOR instruction.

A CPUID feature flag (ECX bit 3; CPUID executed EAX = 1) indicates the availability of MONITOR and MWAIT in the processor. When set, MWAIT may be executed only at privilege level 0 (use at any other privilege level results in an invalid-opcode exception). The operating system or system BIOS may disable this instruction by using the IA32_MISC_ENABLES MSR; disabling MWAIT clears the CPUID feature flag and causes execution to generate an illegal opcode exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**MWAIT for Address Range Monitoring**

For address-range monitoring, the MWAIT instruction operates with the MONITOR instruction. The two instructions allow the definition of an address at which to wait (MONITOR) and a implementation-dependent-optimized operation to commence at the wait address (MWAIT). The execution of MWAIT is a hint to the processor that it can enter an implementation-dependent-optimized state while waiting for an event or a store operation to the address range armed by MONITOR.

ECX specifies optional extensions for the MWAIT instruction. EAX may contain hints such as the preferred optimized state the processor should enter.

For Pentium 4 processors (CPUID signature family 15 and model 3), non-zero values for EAX and ECX are reserved. Later processors defined ECX=1 as a valid extension (see below).

A store to the address range armed by the MONITOR instruction, an interrupt, an NMI or SMI, a debug exception, a machine check exception, the BINIT# signal, the INIT# signal, or the RESET# signal will exit the implementation-dependent-optimized state. An interrupt will cause the processor to exit only if the state was entered with interrupts enabled or if ECX=1.

If a store to the address range causes the processor to exit, execution will resume at the instruction following the MWAIT instruction. If an interrupt (including NMI) caused the processor to exit the implementation-dependent-optimized state, the
processor will exit the state and handle the interrupt. If an SMI caused the processor

to exit the implementation-dependent-optimized state, execution will resume at the

instruction following MWAIT after handling of the SMI. Unlike the HLT instruction, the

MWAIT instruction does not support a restart at the MWAIT instruction. There may

also be other implementation-dependent events or time-outs that may take the

processor out of the implementation-dependent-optimized state and resume execu-

tion at the instruction following the MWAIT.

If the preceding MONITOR instruction did not successfully arm an address range or if

the MONITOR instruction has not been executed prior to executing MWAIT, then the

processor will not enter the implementation-dependent-optimized state. Execution

will resume at the instruction following the MWAIT.

MWAIT for Power Management

MWAIT accepts a hint and optional extension to the processor that it can enter a

specified target C state while waiting for an event or a store operation to the address

range armed by MONITOR. Support for MWAIT extensions for power management is

indicated by CPUID.05H.ECX[0] reporting 1. EAX and ECX will be used to communicate the additional information to the MWAIT

instruction, such as the kind of optimized state the processor should enter. ECX spec-

ifies optional extensions for the MWAIT instruction. EAX may contain hints such as

the preferred optimized state the processor should enter. A given processor imple-

mentation may choose to ignore the hint and continue executing the next instruction.

Future processor implementations may implement several optimized "waiting" states

and will select among those states based on the hint argument.

Table 3-70 describes the meaning of ECX and EAX registers for MWAIT extensions.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Treat Interrupt as break-event, even when interrupts are disabled (EFLAGS.IF=0). May be set only if CPUID.01H:ECX.MONITOR[bit 3] = 1.</td>
</tr>
<tr>
<td>31: 1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Note that if MWAIT is used to enter any of the C-states that are numerically higher than C1, a store to the address range armed by the MONITOR instruction will cause the processor to exit MWAIT only if the store was originated by other processor agents. A store from non-processor agent may not cause the processor to exit MWAIT in such cases.

For additional details of MWAIT extensions, see Chapter 14, “Power and Thermal Management,” of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*.

**Operation**

(* MWAIT takes the argument in EAX as a hint extension and is architected to take the argument in ECX as an instruction extension MWAIT EAX, ECX *)

```c
{ 
    WHILE ("Monitor Hardware is in armed state") {
        implementation_dependent_optimized_state(EAX, ECX); 
    } 
    Set the state of Monitor Hardware as triggered; 
}
```

**Intel C/C++ Compiler Intrinsic Equivalent**

```c
MWAIT  void _mm_mwait(unsigned extensions, unsigned hints)
```

**Example**

MONITOR/MWAIT instruction pair must be coded in the same loop because execution of the MWAIT instruction will trigger the monitor hardware. It is not a proper usage to execute MONITOR once and then execute MWAIT in a loop. Setting up MONITOR without executing MWAIT has no adverse effects.

 Typically the MONITOR/MWAIT pair is used in a sequence, such as:

EAX = Logical Address(Trigger)
ECX = 0 (*Hints * )

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 : 0</td>
<td>Sub C-state within a C-state, indicated by bits [7:4]</td>
</tr>
<tr>
<td>7 : 4</td>
<td>Target C-state*</td>
</tr>
<tr>
<td></td>
<td>Value of 0 means C1; 1 means C2 and so on</td>
</tr>
<tr>
<td></td>
<td>Value of 01111B means C0</td>
</tr>
<tr>
<td></td>
<td>Note: Target C states for MWAIT extensions are processor-specific C-states, not ACPI C-states</td>
</tr>
<tr>
<td>31: 8</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
EDX = 0 (* Hints *)

IF (!trigger_store_happened)
    MONITOR EAX, ECX, EDX
    IF (!trigger_store_happened)
        MWAIT EAX, ECX

The above code sequence makes sure that a triggering store does not happen between the first check of the trigger and the execution of the monitor instruction. Without the second check that triggering store would go un-noticed. Typical usage of MONITOR and MWAIT would have the above code sequence within a loop.

**Numeric Exceptions**

None

**Protected Mode Exceptions**

- **#GP(0)**
  - If ECX[31:1] ≠ 0.
  - If ECX[0] = 1 and CPUID.05H:ECX[bit 3] = 0.
- **#UD**
  - If CPUID.01H:ECX.MONITOR[bit 3] = 0.
  - If current privilege level is not 0.

**Real Address Mode Exceptions**

- **#GP**
  - If ECX[31:1] ≠ 0.
  - If ECX[0] = 1 and CPUID.05H:ECX[bit 3] = 0.
- **#UD**
  - If CPUID.01H:ECX.MONITOR[bit 3] = 0.

**Virtual 8086 Mode Exceptions**

- **#UD**
  - The MWAIT instruction is not recognized in virtual-8086 mode (even if CPUID.01H:ECX.MONITOR[bit 3] = 1).

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

- **#GP(0)**
  - If RCX[63:1] ≠ 0.
  - If RCX[0] = 1 and CPUID.05H:ECX[bit 3] = 0.
- **#UD**
  - If the current privilege level is not 0.
  - If CPUID.01H:ECX.MONITOR[bit 3] = 0.